TECH TIPS

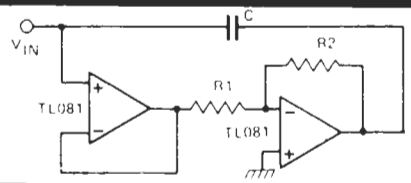
Capacitance multiplier

When an audio circuit calls for a large value capacitor — such as in a filter — then this circuit can substitute for those very difficult to get, expensive high-value capacitors. The circuit only synthesises the required impedance, it will not store energy.

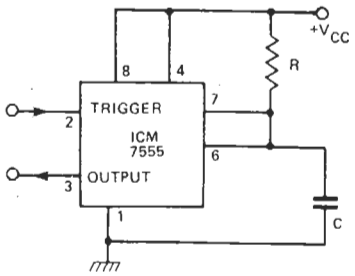
its value from:

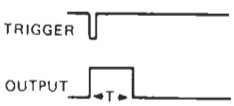
$C_{IN} = C(R1 + R2)/R1$

Note that TL071 or NE5534 op-amps could be substituted for the TL081 specified.

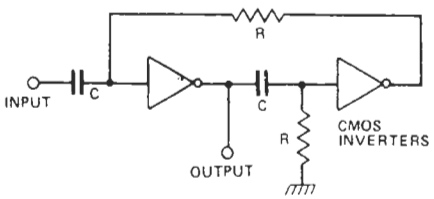


Monostables





CMOS 555
T = 1.1RC



CMOS inverters
T = 1.38RC
Keep R greater than 47k

A commonly-used circuit block is the monostable. There are several convenient ways to realise one and these two general circuits show how. Suitable CMOS inverters for the upper circuit would be 74C04, 4009, 4049 and 4069. Inverters can be made by typing the input of NAND gates together, don't forget. 'Rule of thumb' timing equations are given.

The ICM7555 is a CMOS version of the ever-popular 555. In this application the input is pin 2, output is pin 3.

The input, at V_{IN}, looks like a capacitor (C_{IN}) and you can calculate

BY CLEMENT S. PEPPER

A MONOSTABLE CATALOG for Experimenters

A guide to today's IC monostable multivibrators emphasizes their usefulness in practical applications

MONOSTABLE multivibrators, sometimes called "one-shots," are electronic circuits that, when triggered, deliver an output pulse of a predetermined width.

Although today's IC monostables still provide the one-shot function, their usefulness has been greatly extended. These modern devices feature multiple inputs with both positive- and negative-edge triggering, complementary outputs, retriggerability and resetability. They are also very easy to use, lower in cost, and available in conventional and low-power TTL and CMOS.

The key features of a number of popular monostables are summarized in the "Catalog." The information is sufficient to enable using the mono without recourse to a data sheet. Summaries of the 555 and 558/559 timers (which can function as a one-shot) are included separately in Figs. 3 and 5.

Triggering. All of the monos in the catalog will trigger from a high-to-low or from a low-to-high transition. For triggering to actually occur on the transition, all inputs must conform to defined logic states. These states are shown in the "Input Table" for each device.

The logic tables in the manufacturers data sheets include inhibit as well as trigger conditions. Only trigger conditions are shown in the Catalog. Any other state is an inhibit.

Each line of the table defines a trigger mode for a "one-shot" output. "A" and "B" designators are used in the Input Tables. Several monos have multiple A and/or B inputs though not all manufacturers use this notation. An "A" input is defined as a high-to-low transition (shown as a down arrow), while a "B" input is defined as a low-to-high transition (shown as an up arrow). The CMOS 4098B/4528/14528 are exceptions—the A and B transitions being reversed.

The A and B inputs have a defined logical relationship to each other, but these are not consistent between devices. You should go by the Input Table for the mono being used. Triggering occurs at a voltage level independent of the transition time, while rise and fall times are consistent with the type of logic family.

The 74121 and the 74LS221 feature Schmitt circuitry at their B input. They trigger with a 1-volt/s rise time, and provide 1.2 volts of noise immunity.

All of the monos shown provide complementary outputs. The Q output is normally low and goes high for the pulse duration. The not-Q output is normally high and goes low. Pulse width is identical for both outputs.

The minimum pulse widths and delay times listed are subject to some conditions. They are included to provide a generalized picture of limiting conditions. If nanosecond timing is critical to your application, consult the manufacturer's data sheet.

(Continued on page 74)

(Continued from page 69)

Pulse Timing. A typical timing equation has the form tw=k*RC* where tw is the pulse width in nanoseconds, k is a constant, *R* is the timing resistance in kilohms, and *C* is the timing capacitance in picofarads.

For example, the pulse width for the 74121 is given as tw=.693*RC*. Assume that *R* is 10,000 ohms, and *C* is 100 pF. Then the equation is tw=.693(10)(100) =693 ns or .693 μs.

Retriggering. Some monos are retriggerable. That is, if a second trigger arrives while the output is still high from the first pulse, the output will respond to the latest trigger and remain high. The extension is for one complete cycle and a train of input triggers will result in a sustained output pulse that will have a very long duration.

Retriggering may be accomplished from either the A or B inputs, simply or intermixed. This makes for some intriguing timing possibilities.

However, there is a time restriction on retriggering some monos. As shown in the Catalog, the required delay is the number in parenthesis following "re-triggerable." Thus, the 74123 cannot be retriggered before 0.22 ns after the previous input.

Retriggering is useful when you want it, but on the other hand, what do you do if you don't want it? Suppose, for example, you are using a 74123 dual mono because you need retrigger for one circuit, but you cannot live with it in the other. In this case, connect the B input to the not-Q output and trigger with the A input (or vice versa). When the mono triggers, B is pulled low thus inhibiting further triggering until the circuit times out. Be sure, however, that the A input(s) are in the inhibit mode at the time out, or you will have an oscillator instead of a mono.

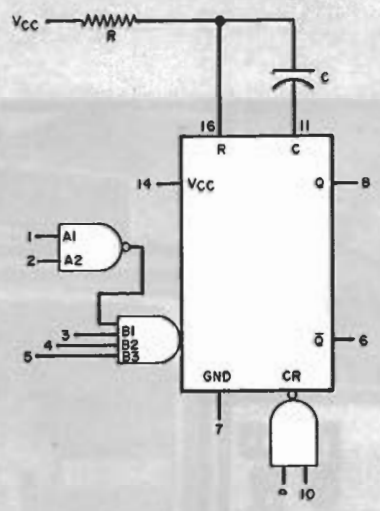
Reset. Some monos, but not all, provide for reset. This is implemented by applying a reset pulse to the CR (clear) input. The leading edge of this pulse resets the outputs to the initial state, and another trigger is required to obtain an output.

If the CR input is held in the reset state, the mono is inhibited and will not respond to an input trigger. This feature adds flexibility to the controlling logic for the mono.

R and C Limits. All monos have upper and lower limits for the range of resistance (R), while some have limits on

MONOSTABLE CATALOG-1

9600 SINGLE TTL



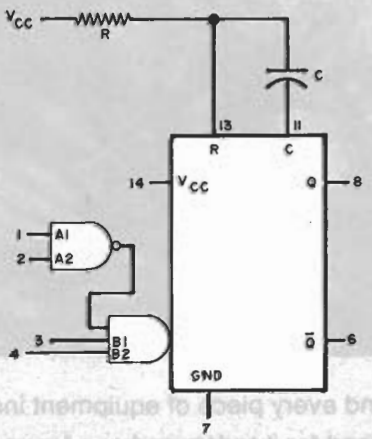
A_1	A_2	B_1	B_2	B_3
↓	1	1	1	1
1	↓	1	1	1
0	X	↑	1	1
X	0	↑	1	1
0	X	1	↑	1
X	0	1	↑	1
0	X	1	1	↑
X	0	1	1	↑

INPUT TABLE

t_w=0.32RC (1+0.7/R)

FEATURES
RETRIGGERABLE (0.3Cns)
RESET ON LOW TO EITHER "CR" INPUT
t_{min}= 74 ns
t_{pd}=29 ns
LIMIT ON R=
5k ≤ R ≤50k
(0 ≤ T°C ≤75)
LIMITS ON C:
NONE

9601 SINGLE TTL



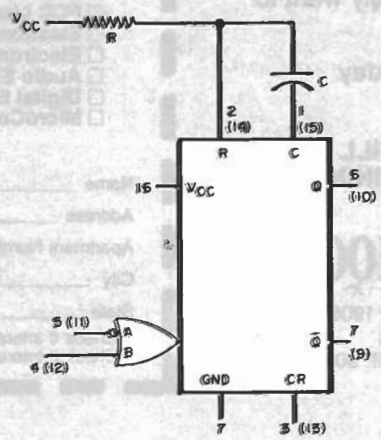
A_1	A_2	B_1	B_2
↓	1	1	1
1	↓	1	1
0	X	↑	1
X	0	↑	1
0	X	1	↑
X	0	1	↑

INPUT TABLE

t_w=0.32RC (1+0.7/R)

FEATURES
RETRIGGERABLE (0.3Cns)
NOT RESETTABLE.
t_{min}=45 ns.
t_{ps}=25ns.
LIMITS ON R:
5k ≤ R ≤50k
(0 ≤ T°C ≤75)
LIMITS ON C:
NONE

9602 DUAL TTL



A	B
↓	D
1	↑

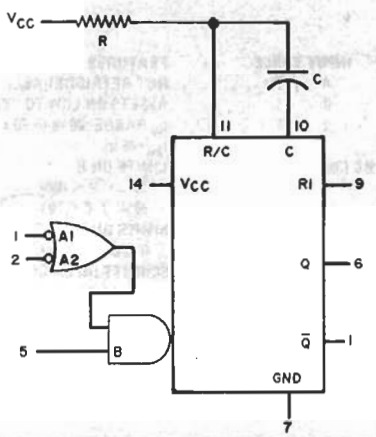
INPUT TABLE

t_w=0.31RC (1+1/R)

FEATURES
RETRIGGERABLE (0.3Cns)
RESET ON LOW TO "CR"
t_{min}=72 ns
t_{pd}=25 ns
LIMITS ON R:
5k ≤ R ≤50k
(0 ≤ T°C ≤75)
LIMITS ON C:
NONE

MONOSTABLE CATALOG-2

74121 SINGLE TTL



INPUT TABLE		
A_1	A_2	B
0	X	↑
X	0	↑
↓	X	1
X	↓	1

t_w=0.693 RC
TO USE THE INTERNAL TIMING RESISTOR, CONNECT PIN 9 TO V_{cc}.
FOR C=0, t_w=30 ns.

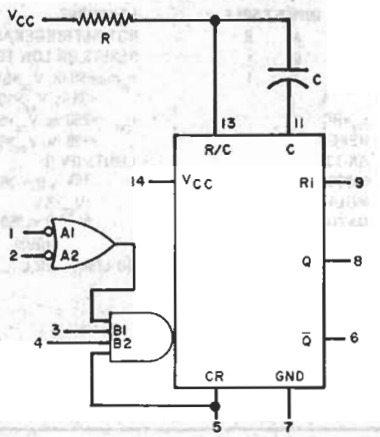
FEATURES
NOT RETRIGGERABLE
NOT RESETTABLE
"B" IS A SCHMITT INPUT
t_{min}=30 ns
t_{pd}=45 ns
R_{int}=12 kΩ
LIMITS ON R:
1.4k ≤ R ≤ 40k
(0 ≤ T°C ≤ 70)
LIMIT ON C:
0 ≤ C ≤ 1000 μF

74122 SINGLE TTL

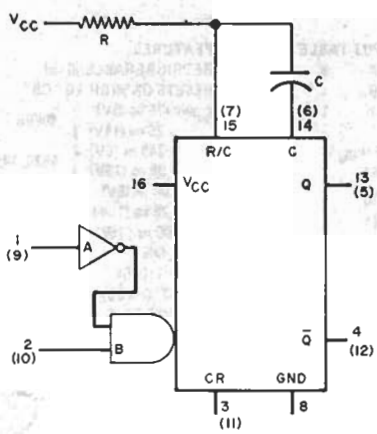
INPUT TABLE			
A_1	A_2	B_1	B_2
0	X	↑	1
0	X	1	↑
X	0	↑	1
X	0	1	↑
1	↓	1	1
↓	↓	1	1
↓	1	1	1

t_w=0.32 RC (1+0.7/R)
TO USE THE INTERNAL TIMING RESISTOR CONNECT PIN 9 TO V_{cc}.

FEATURES
RETRIGGERABLE (0.22 ns)
RESET ON LOW TO "CR"
t_{min}=40 ns
t_{pd}=21 ns
LIMITS ON R:
5k ≤ R ≤ 50k
(0 ≤ T°C ≤ 70)
LIMITS ON C:
NONE



74123 DUAL TTL



INPUT TABLE	
A	B
0	↑
↓	1

t_w=0.32 RC (1+0.7/R)

FEATURES
RETRIGGERABLE (0.22 ns)
RESETS ON LOW TO "CR"
t_{min}=40 ns
t_{pd}=21 ns
LIMITS ON R:
5k ≤ R ≤ 50k
(0 ≤ T°C ≤ 70)
LIMITS ON C:
NONE

capacitance (C). Typical limits for industrial devices are shown in the Catalog.

In general, try to stay away from maximum values of *R*, especially when using electrolytic capacitors for *C*.

Conventional electrolytics and aluminum electrolytics can be a problem. Most high-quality tantalums perform well. Inserting a silicon diode between the *R/C* terminal and the *RC* junction as shown in Fig, 1, will eliminate any leakage problem that may occur with reverse voltage across the capacitor. However, if you use this diode, the value of *R* must be reduced to less than 60% of its maximum value. Some circuits do use tantalums without the diode, but with reduced values of *R*. If your circuit has to operate at elevated temperature, be cautious.

Avoiding Problems. The greatest single source of problems is false triggering, and the second is no triggering at all.

IC monostables are very fast, and according to "Murphy's Law" if the inputs can couple to form a "glitch" generator, they will. Therefore, input lines should be kept short and isolated from neighboring lines to avoid the unwanted stray coupling.

A 0.1-μF or larger capacitor should be connected between the V_{CC} and ground right at the IC. The upper trace of Fig. 2 shows large "spikes" riding on the leading edge of each waveform. After installing the bypass capacitor, the signal cleared up as shown in the lower trace.

Using a scope whose ground lead is connected to the power supply ground, take a look at the signal ground line to make sure that it really is ground. It shouldn't be riding a half a volt or so above ground, or displaying a lush growth of grass (noise).

Always make the foil traces for Vcc and ground heavier than pin interconnections. This keeps their resistance low and current pulses passing through them do not develop voltage drops that can appear as signals to other devices connected to the lines.

If possible, test your mono outside the circuit, using the timing values you require. Don't forget the minimum retriggering time.

The 555. This timer IC, as well as the 558/559, do not conform to the standard monostable format and were not included in the Catalog. However, these timer ICs can be used as one-shots or as free-running or gated oscillators.

They do have limitations, though: they are slow when compared to the other monos, and pulses narrower than 10 μs are best obtained with a TTL device. Also, they're not retriggerable; and in the free-running mode, they have a duty-cycle limitation.

They do, however, have a single output, can operate with a wide range of supply voltages, and can sink or source 200 mA (which can save a driver transistor).

The use of a 555 as a one-shot or free-running oscillator is shown in Fig. 3. The capacitor connected to CV (pin 5) is essential to reduce noise.

In the mono mode, calculations are based on $t_W = 1.1RC$. For these timers, *R* is shown in ohms, *C* in farads and t is in seconds.

For any timing circuit, it is best to use a standard value of capacitance for *C*, then calculate the required resistance. It's always possible to combine different standard resistances in series, parallel or combinations, but it is difficult to locate an odd value of capacitance.

For the free-running mode, there are four defining equations:

D = *Rb*/(*Ra* + 2*Rb*) = t2/t1 = duty cycle
t1 = 0.693(*Ra* + *Rb*)*C* = output high time
t2 = 0.693*RbC* = output low time
T = 0.693(*Ra*+2*Rb*)*C* = t1 + t2

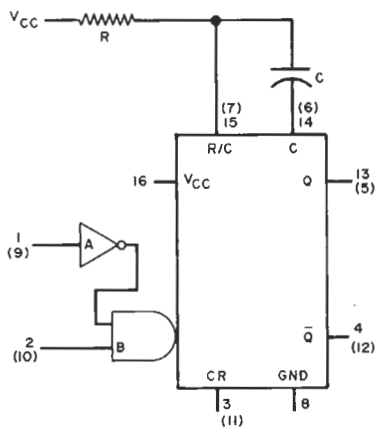
In the equation for D, note that if *Ra* is zero, then D becomes 0.5. This tells you not to try to get a square-wave output as you have to tie DS (pin 7) directly to Vcc. There is no internal current-limiting resistor within the chip, so do not try this. Select D as 0.25 or 0.3 for most cases.

It's usually best to start by selecting a value of C appropriate to the frequency and duty cycle. *Rb* is then computed using the equation for t2, and this is plugged into the D equation to solve for *Ra*. Then solve for T as a check on the values.

There are several ways to generate a square wave. The circuit shown in Fig. 3E allows a wide selection of both frequency and duty cycle from a single capacitor. This is illustrated by the composite scope traces shown in Fig. 4. In the circuit, *R1* was 2200 ohms, *R2* was a 10,000-ohm potentiometer and *C* was a 0.01-μF capacitor. The three traces represent three settings of *R2*. Overall frequency range was from 5 to 80 kHz. If trimmer potentiometers were used for both *R1* and *R2*, the frequency and duty cycle could be trimmed to the exact requirements.

MONOSTABLE CATALOG-3

74LS221 DUAL LSTTL

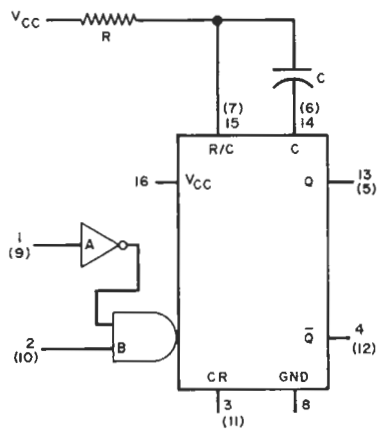


INPUT TABLE	
A	B
0	↑
↓	1

$t_W = RC\ (3.03\ RC)$

FEATURES
NOT RETRIGGERABLE
RESETS ON LOW TO "CR"
t_W RANGE=30 ns to 70 s
t_{pd}=45 ns
LIMITS ON R
1.4k ≤ R ≤ 100k
(0 ≤ T°C ≤ 70)
LIMITS ON C
0 ≤ C ≤ 1000 μf
SCHMITT INPUT ON "B"

74C221 DUAL CMOS

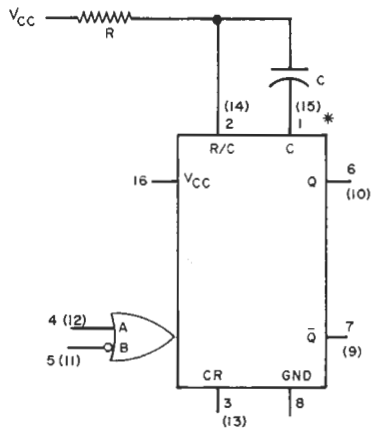


INPUT TABLE	
A	B
0	↑
↓	1

$t_W = RC$
REFERENCE:
AN-138 "USING THE CMOS DUAL MONO. MULTIVIBRATOR" NATIONAL SEMICONDUCTOR

FEATURES
NOT RETRIGGERABLE
RESETS ON LOW TO "CR"
$t_w$min=50 ns, V_{cc}=5V
=30 ns, V_{cc}=10V
t_{pd} =250 ns, V_{cc}=5V
=120 ns, V_{cc}=10V
LIMITS ON R:
10k ≤ R ≤ 350k
(V_{cc}=5V
5k ≤ R ≤ 350k
(V_{cc}=10V)
NO LIMITS ON C.

4098B/4528B/MC14528CP DUAL CMOS



* WITH 4528, MC14528CP CONNECT PINS 1 AND 15 TO PIN 8.

INPUT TABLE	
A	B
0	↓
↑	1

$t_W = 0.2\ RC\ (\log_e V_{cc})$
$\log_e 5 = 1.61$
10=2.30
15=2.71

FEATURES
RETRIGGERABLE (0 ns)
RESETS ON HIGH TO "CR"
$t_w$min=75 ns (5V) } 4098B
25 ns (15V) }
240 ns (5V) } 4528, 14528
90 ns (15V) }
t_{pd}=300 ns (5V)
125 ns (10V)
100 ns (15V)
LIMIT ON R
5k ≤ R ≤ 1000k
(-40 ≤ T°C ≤ 85)
NO LIMIT ON C

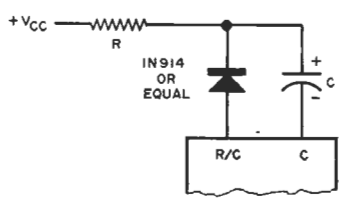


Fig. 1. Use of a diode prevents high inverse leakage currents through the timing capacitor.

The period is linear with respect to *C*. A substitution of a 0.1-μF capacitor reduced the frequency by a factor of 10 while preserving the duty cycle. This circuit allows for a low-cost pulse generator with lots of flexibility.

The 558/559 Timers. These are quad timers having a range of a few microseconds to a few hours. Each of the four monos are independent, but they share a common reset. They are edge-triggered, and several sections can be coupled in tandem to produce an output several hours long.

A function diagram and important features of these timers are shown in Fig. 5. The 558 has an open collector output (Fig. 5D) while the 559 has a Darlington follower output (Fig. 5E). In all other respects, the two are identical.

The output pulse width is the *RC* product of the timing components. Two devices may be cross-coupled to operate in the free running mode as shown in Fig. 5C. The potentiometer connected to the CV line allows adjustment of the output pulse width and duty cycle. The CV voltage range is from 0.5 V to V_{CC} minus 1 volt.

Applications. A simple pulse can be created by *RC* coupling between gates or flip-flops. Although this approach will work, it is marginal at best. For example, take a look at the circuit shown in Fig. 6A. Operation depends on the overshoot at the trailing edge. The system malfunctioned because the overshoot was marginal. Also, 750 ohms is too small a pulldown for TTL, and the circuit is susceptible to noise because there can be a volt or more of dc offset at the input.

If a 74123 dual mono had been used, as in the circuit shown in Fig. 6B, the time delay could have been achieved at

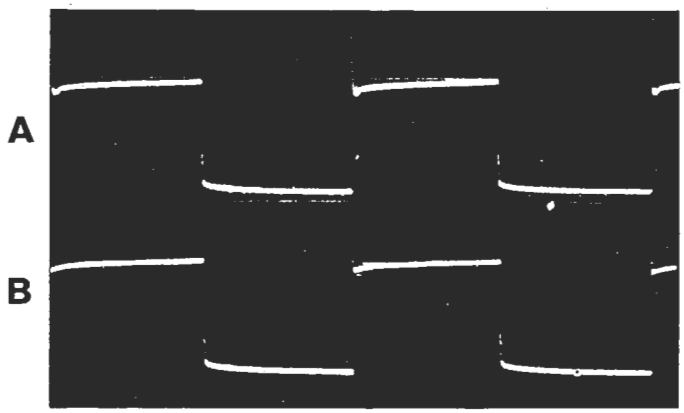
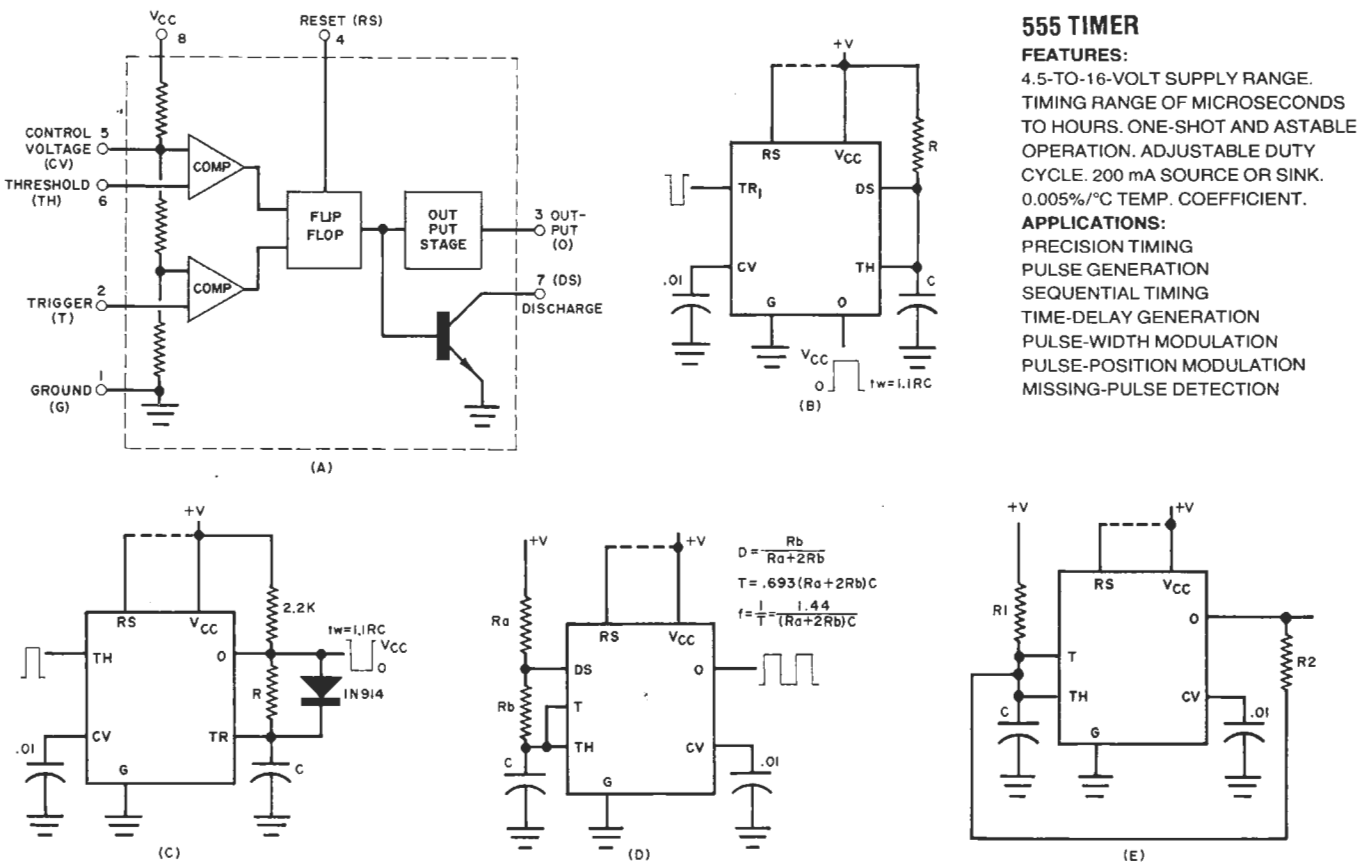


Fig. 2. A 2-volt spike on leading edge of waveform (A) is removed (B) by using a bypass capacitor from V_{cc} to ground.



555 TIMER

FEATURES:
4.5-TO-16-VOLT SUPPLY RANGE. TIMING RANGE OF MICROSECONDS TO HOURS. ONE-SHOT AND ASTABLE OPERATION. ADJUSTABLE DUTY CYCLE. 200 mA SOURCE OR SINK. 0.005%/°C TEMP. COEFFICIENT.

APPLICATIONS:
PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME-DELAY GENERATION
PULSE-WIDTH MODULATION
PULSE-POSITION MODULATION
MISSING-PULSE DETECTION

Fig. 3. The 555 timer function diagram (A), positive output with negative trigger (B), negative output for positive trigger (C), astable operation (D), and astable operation for a 50% duty cycle (E).

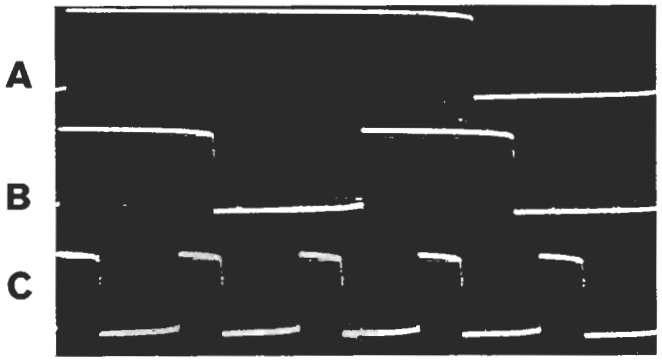
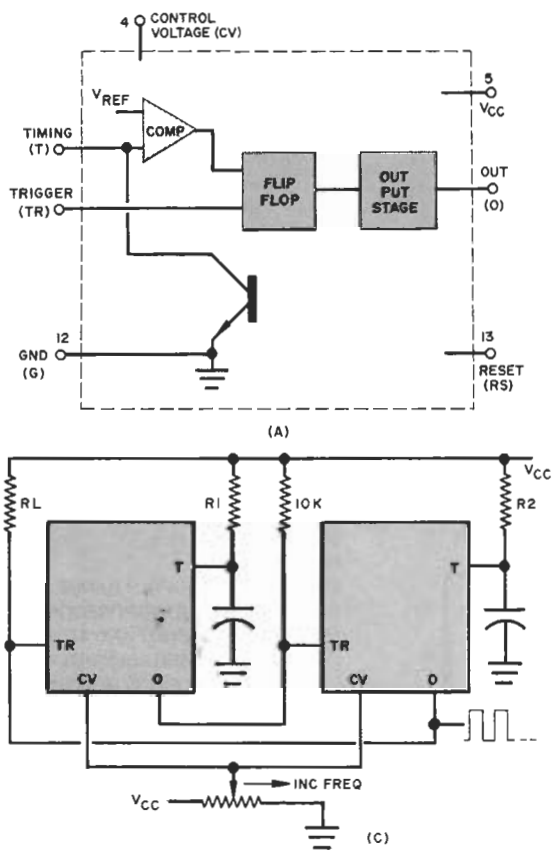


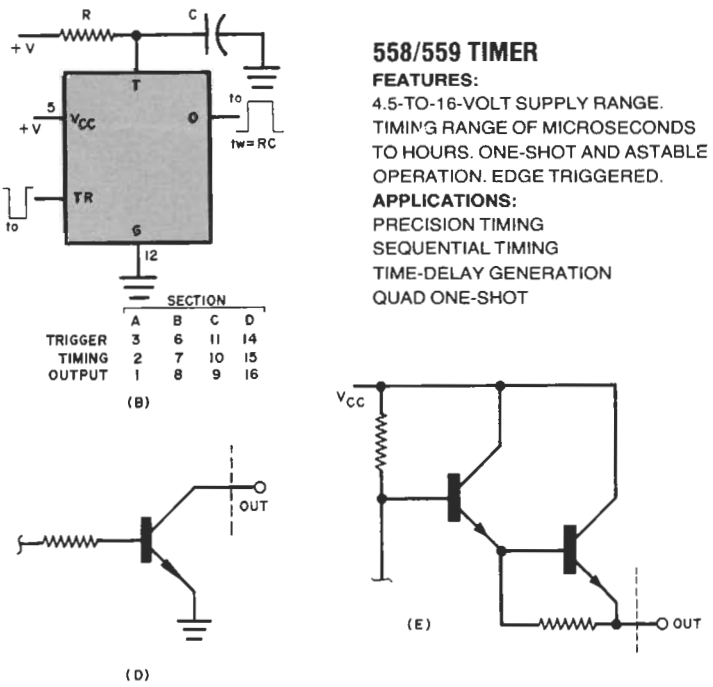
Fig. 4. Waveforms for various values or R2 in Fig. 3E. (A) is 10 kHz; (B) is 20 kHz; and (C) is 50 kHz.

no real increase in cost, but with greatly improved reliability. The output pulse would have defined and controlled width.

Occasions may arise when you need an oscillator having independent control of frequency and duty cycle. The 74123 (TTL) or the 74C221 (CMOS) dual monos perform this task very well using the circuit shown in Fig. 7.

If you use potentiometers for *R1* and *R2*, you can construct a low-cost, wide-





558/559 TIMER

FEATURES:
4.5-TO-16-VOLT SUPPLY RANGE. TIMING RANGE OF MICROSECONDS TO HOURS. ONE-SHOT AND ASTABLE OPERATION. EDGE TRIGGERED.

APPLICATIONS:
PRECISION TIMING
SEQUENTIAL TIMING
TIME-DELAY GENERATION
QUAD ONE-SHOT

Fig. 5. Function diagram (A) of 558/559 timer; monostable connection (B); 558 as a variable-frequency oscillator with fixed duty cycle (C); 558 open-collector output structure (D) and 559 Darlington follower output structure (E).

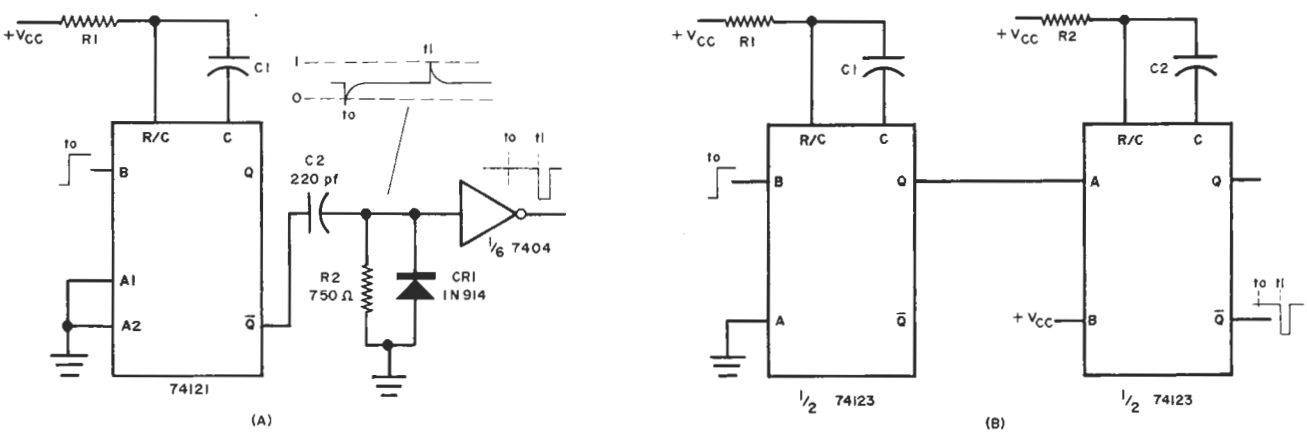


Fig. 6. RC coupling (A) used for leading edge delay for the 7404. Using a 74123 (B) provides precisely timed pulse with improved reliability.

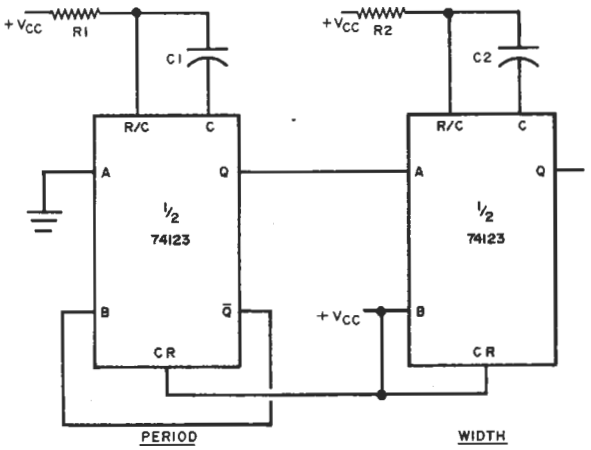


Fig. 7. A dual monostable can create an oscillator having independently adjustable period and pulse width.

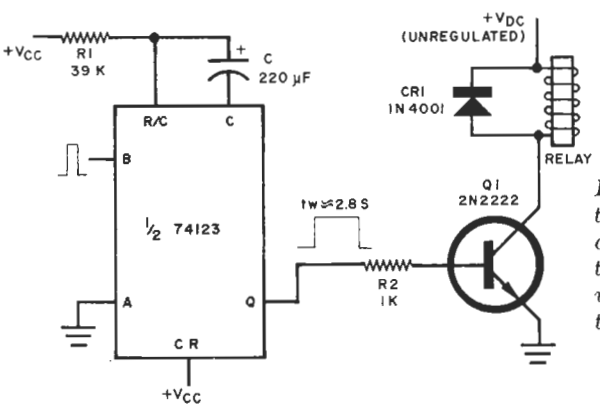


Fig. 8. A switching transistor provides relay driving power and isolates the mono from higher voltage required by the relay.

range pulse generator with lots of versatility. The capacitors may be switched to change the timing parameters.

Retriggering. This is a feature that should not be overlooked. A retriggerable mono will respond to inputs that arrive while the output is still high from the preceeding trigger. It then becomes possible to have a train of inputs that will hold the output high until the train stops.

A telephone toll restrictor was created using this effect. The problem was that there was only one signal to tell the circuit that the phone was lifted off the cradle, that the dial was being used, that dialing was completed, and that the phone was replaced on the cradle. The retriggering capability of the 74123 enabled the digits counter for the pulses from the dialer; and when the train stopped, there was a short delay, then a reset of the counter for the next digit.

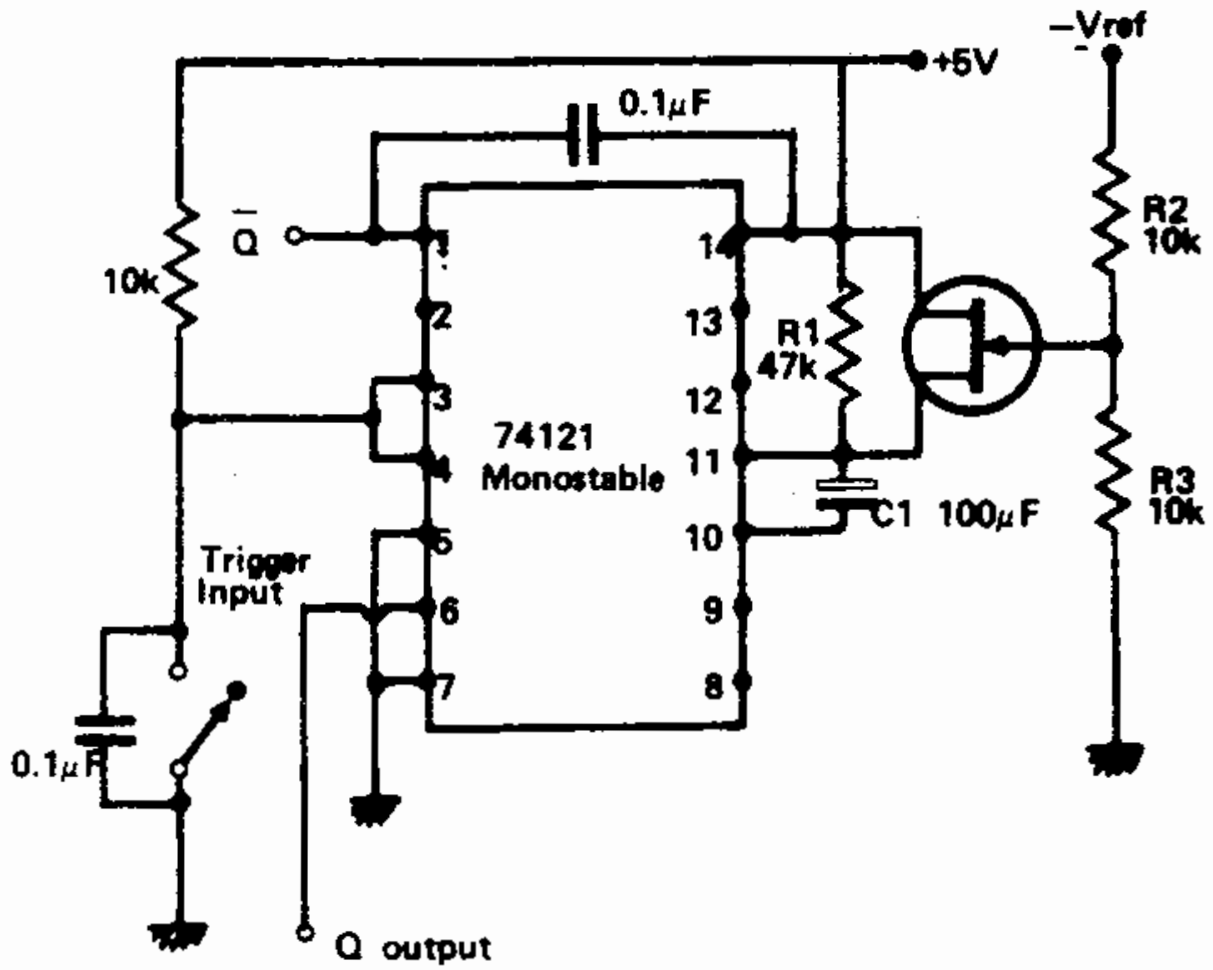
Multiple Inputs. Several monos, such as the 9600,9602 and 74121 have multiple trigger inputs. These may be used as digital summing elements when you wish to form a single pulse train as a summation of triggers from several sources. Be careful here because the logic can be tricky.

Pulse Stretching. A mono can be used to stretch a brief pulse so that it can be used to drive a relay, among other applications. The basic circuit is shown in Fig. 8. The 555, 558 and 559 are well suited to this use because of their drive capabilities.

An advantage of this circuit is that the load can be powered from a higher voltage than the logic. In Fig. 8, the relay is powered from the unregulated dc supply, saving the power supply regulator. Isolating resistor *R2* is important to protect *Q1*. If heavy load current is required, the emitter of *Q1* should be returned to the power supply ground.

Summary. Because of the edge triggering features of each of the devices discussed here, many mono's can be interconnected to create complex digital waveforms that can be duplicated only with expensive commercial generators. Also, edge triggering greatly reduces the need for logic gates. ◇

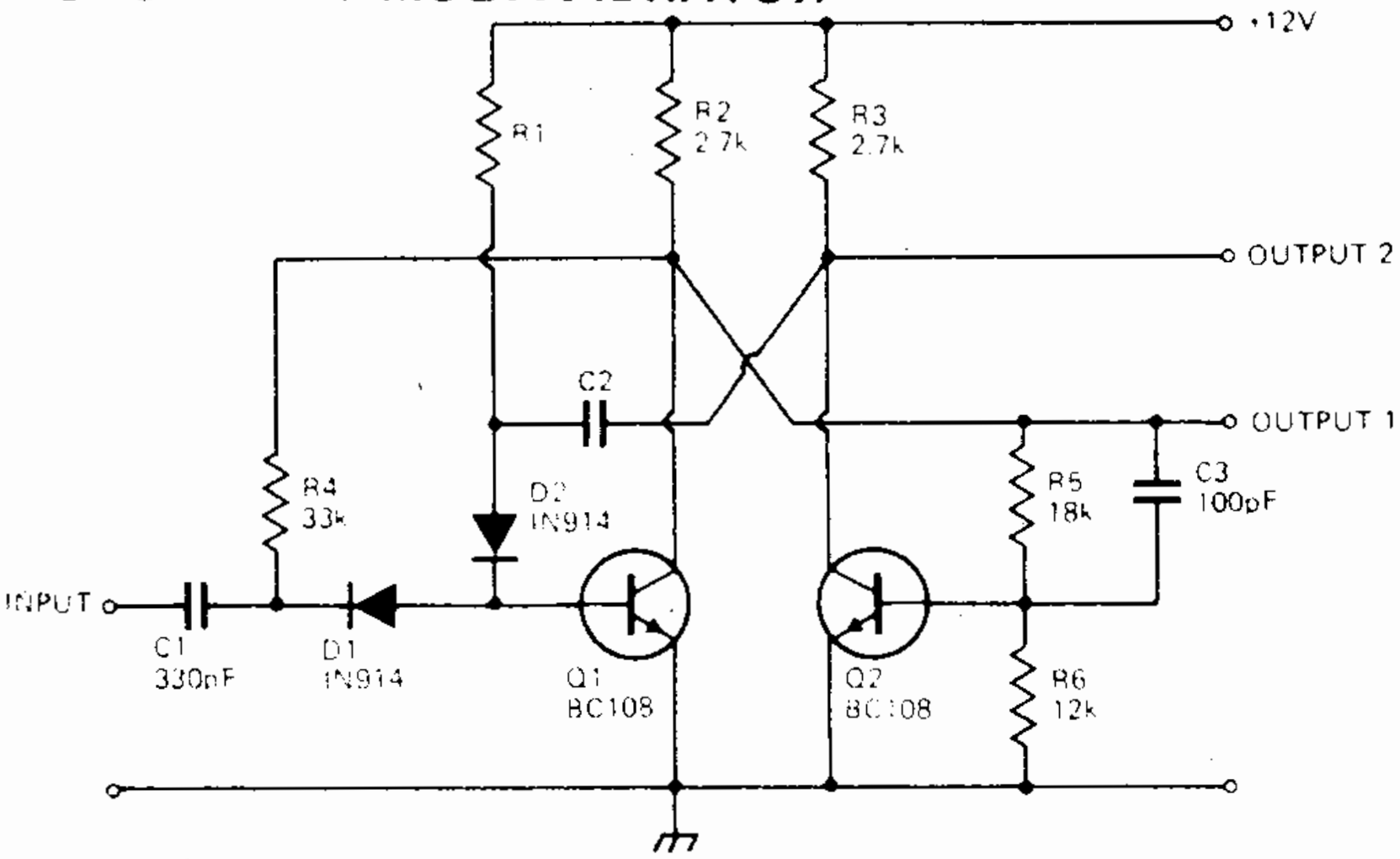
VOLTAGE CONTROLLED MONOSTABLE



This circuit was used to switch a motor on for a variable period as part of a position control system. Using the components shown a range of 20mS to 2 seconds may be obtained, when V_{ref}, is varied between 0 and –5V. The maximum period is governed by the value of R1 (=0.7R1C1). The minimum by the drain-source resistance of the FET with no gate voltage applied. The FET acts as a voltage controlled resistor in the charging circuit of a 74121 monostable. The FET used was an N-channel 2N3819. If a P-channel device is used, R2 must be taken to + V_{ref}.

stock.

MONOSTABLE MULTIVIBRATOR



The time constant T of this circuit is equal to 0.7 R_1C_2. Where T is in seconds, R_1 in ohms and C_2 in farads. For example when R_1 = 10 k and C_2 = 100 microfarads the time constant will be one second.

Capacitor C_2 may be selected over wide a range and R_1 may be a potentiometer 100 k maximum. Outputs 1 and 2 provide pulses of opposite polarity but the rise time of output 2 is long due to the charging current of C_2.

82

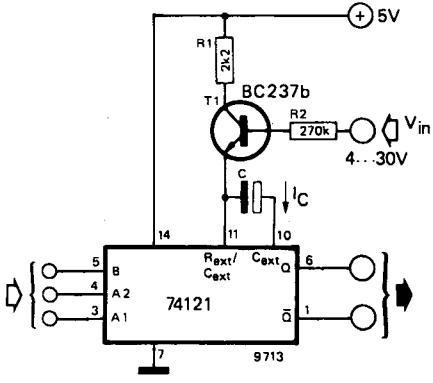
voltage controlled monostable

The 74121 IC is a monostable multivibrator, the pulse length of which may be varied from 40 ns to 40 s. An external RC-network determines the duration of the pulse and if the fixed resistor in this network is replaced by a potentiometer (from pin 11 to supply voltage) then the pulse length of the output may be adjusted accordingly. However the diagram shows how it may be used as a voltage-controlled monostable. The external resistor is replaced by transistor T1. This transistor functions as a variable resistor, which, depending on the base-bias voltage (4-30 V), determines the charging current of the external capacitor C. The pulse length is therefore controlled by the bias voltage V_{in}. Using the following formula it is possible to approximately calculate the duration of the pulse:

$$t \approx \frac{C \cdot V_{tr} \cdot R_2}{(V_{in} - 3.6) \cdot B}$$

C = external capacitor (max. 100 μ)
V_{tr} = trigger voltage (c. 3 V)
V_{in} = base-bias voltage
B = DC gain of the transistor

It should be noted that the pulse length does not vary linearly with the bias voltage.
The triggering occurs as in normal MMVs at the inputs A1, A2, and B.



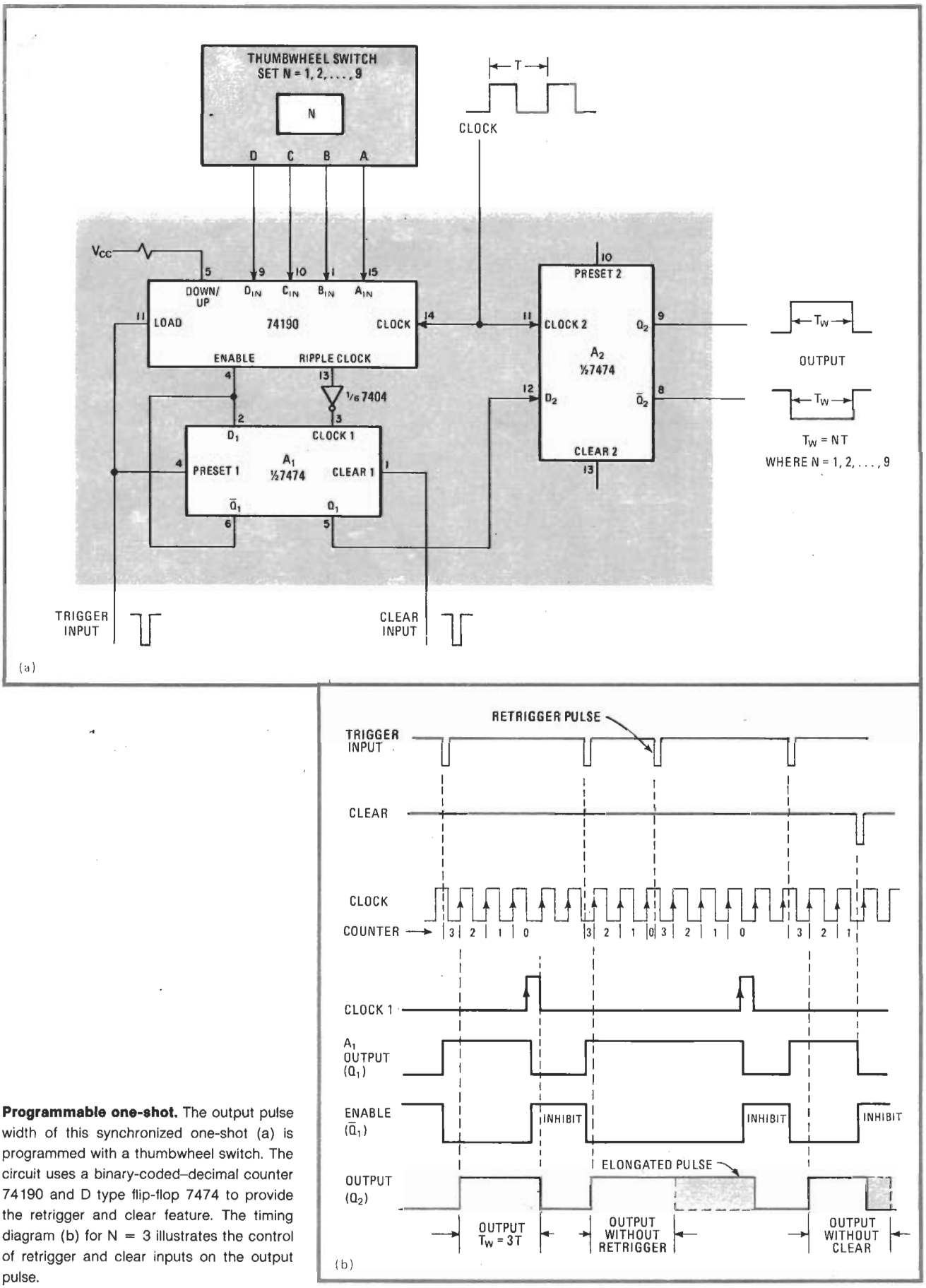
Thumbwheel switch programs retriggerable one-shot

by Dil Sukh Jain
National Remote Sensing Agency, Hyderabad, India

This programmable synchronous one-shot is a few jumps ahead of the rest by being able to generate a synchronized output pulse whose width can be varied through an externally controlled clock period or a programmable thumbwheel switch. In addition, the circuit is retriggerable with a provision for a clear input.

A narrow negative pulse applied at the trigger input loads the synchronous binary-coded–decimal down-up counter 74190 with the number (N) set on the thumbwheel switch and simultaneously sets Q_1 of flip-flop A_1 high. This loading in turn sets Q_2 of flip-flop A_2 high. The low level at $\overline{Q}_1$ enables the counter to count down from N on successive positive edges of the clock.

When the counter reaches zero, a negative pulse is produced at the ripple clock output of the counter 74190, which corresponds to the negative edge of the clock. This negative pulse, inverted by the 7404 chip, triggers A_1 to make Q_1 low and the enable ($\overline{Q}_1$) input high, which in turn disables the counter and inhibits the circuit. The



Programmable one-shot. The output pulse width of this synchronized one-shot (a) is programmed with a thumbwheel switch. The circuit uses a binary-coded–decimal counter 74190 and D type flip-flop 7474 to provide the retrigger and clear feature. The timing diagram (b) for N = 3 illustrates the control of retrigger and clear inputs on the output pulse.

low input level at D_2 terminates the output pulse whose width is given by $T_w = NT$, where T is the clock's period. The one-shot output pulse width when $N = 3$ is 3T(b).

A retrigger pulse applied while the counter is counting down reloads the circuit with set number N and begins a new countdown, resulting in a single stretched pulse at output Q_2. A negative pulse applied at the clear input (while the counter is counting down) terminates the output pulse at the clock's following positive edge. □

NEW IDEAS

Frequency-boundary detector

I'M SURE THAT EVERY ELECTRONICS EXperimenter or hobbyist, at one time or another, has needed a device that would indicate whether or not a signal was within a certain frequency range—I know I did when I was working with a switch-mode power supply. I got what I needed by building the frequency-boundary detector whose circuit is shown in Fig. 1. (The IC's supply and ground connections are shown in Fig. 2.)

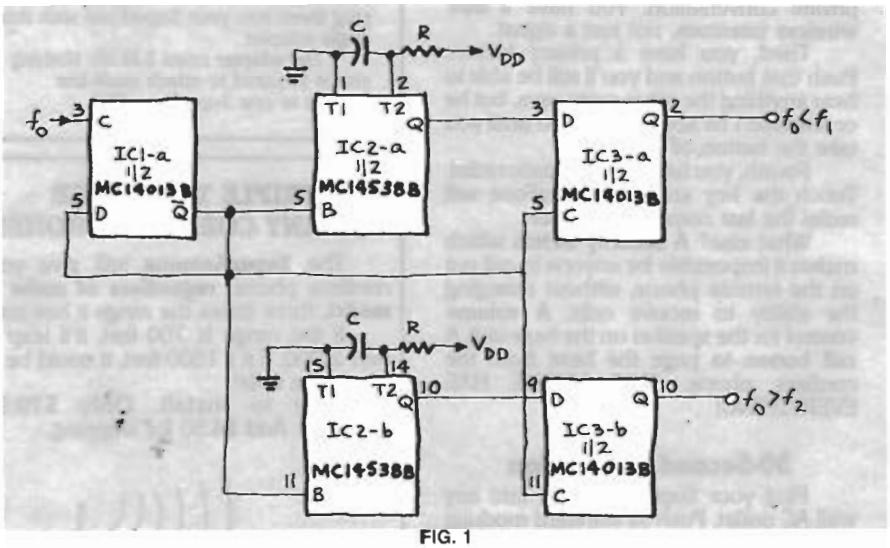


FIG. 1

IC	PINS TIED TO V_{DD}	PINS TIED TO GROUND
IC1	14	4, 6, 7, 8, 9, 10, 11
IC2	3, 13, 16	1, 4, 8, 12, 15
IC3	14	4, 6, 7, 8, 10

FIG. 2

The circuit can be used (with LED's or other indicators) to tell you whether or not an input signal is within a certain frequency range. Because you may be hard-pressed to come up with applications for the circuit, I should point out that voltage-to-frequency converters can be used to make the number of applications almost limitless.

The device itself is rather easy to build. It consists of three IC's—a dual monostable multivibrator and two dual D-type flip flops. The signal whose frequency is in question is fed to the clock input of one of the flip-flops. The $\overline{Q}$ output of that flip-flop (IC1-a) is cross-coupled to its data input so that it acts like a divide-by-two counter. (See the timing diagram in Fig. 3.) The trailing edge of the $\overline{Q}$ output is used to trigger the one-shots formed by IC2.

The upper- and lower-frequency boundaries are determined by the two sections of IC2—the dual precision monostable multivibrator—and their external

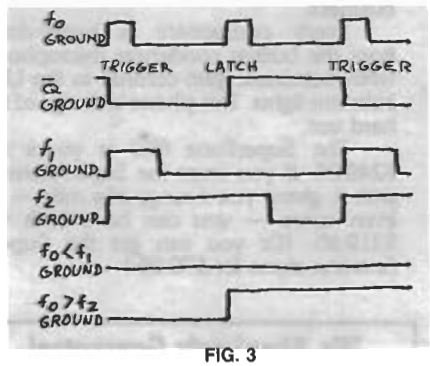


FIG. 3

resistor-capacitor networks. The upper-frequency boundary ($f1$) is set by the output of IC2-a, and the lower-frequency boundary ($f2$) is set by the output of IC2-b. The relationship that describes the periods of the outputs of IC2 is: $T = \frac{1}{2}RC$, where T is measured in seconds, R in ohms, and C in farads. However, because IC1-a is used as a divide-by-two counter, the formula used to determine the period of the upper- and lower-frequency boundaries becomes: $T = RC$.

The frequency of the input to the circuit can be anywhere from DC to 100 kHz. However, you can use the "extra" half of IC1 as another divide-by-two counter and increase the circuit's range to 200 kHz. Then the period of the outputs of IC2 would be represented by: $T = 2RC$.

The states of the outputs of IC2, which determine the upper- and lower-frequency boundaries, are latched by IC3-a and IC3-b respectively. As shown in the timing diagram of Fig. 3, the output of IC3-a (which is clocked by the output of IC1-a) will be high only when the input frequency is less than that of the output of IC2-a ($f1$). The output of IC3-b will be high only when the frequency of the input is greater than that of the output of IC2-b ($f2$). You can use appropriate logic gates to give an "in-bounds" or an "out-of-bounds" indication.—*Jim N. Kitchen*

NEW IDEAS

This column is devoted to new ideas, circuits, device applications, construction techniques, helpful hints, etc.

All published entries, upon publication, will earn $25. In addition, Panavise will donate their *model 333*—The Rapid Assembly Circuit Board Holder, having a retail price of $39.95. It features an eight-position rotating adjustment, indexing at 45-degree increments, and six positive lock positions in the vertical plane, giving you a full ten-inch height adjustment for comfortable working.

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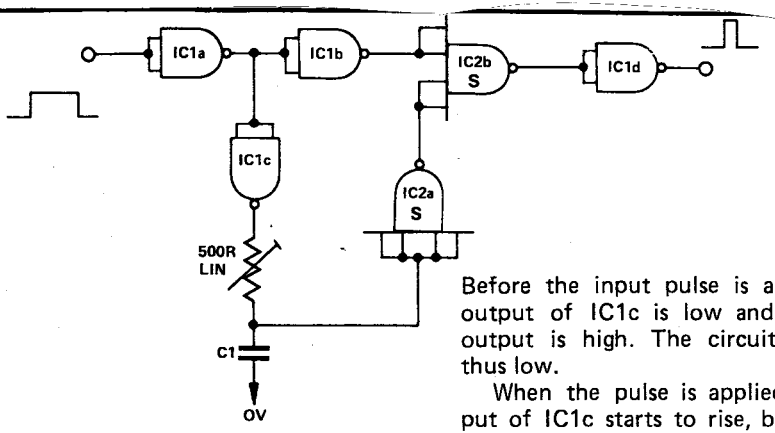


Pulse Compressor

This circuit will prove useful in any application where it is required to reduce the width of a digital pulse by a pre-set amount.

Using only two ICs, it can achieve pulse width reductions up to about 10 milliseconds. The following table gives some examples of the width reduction achieved by using different capacitor values:

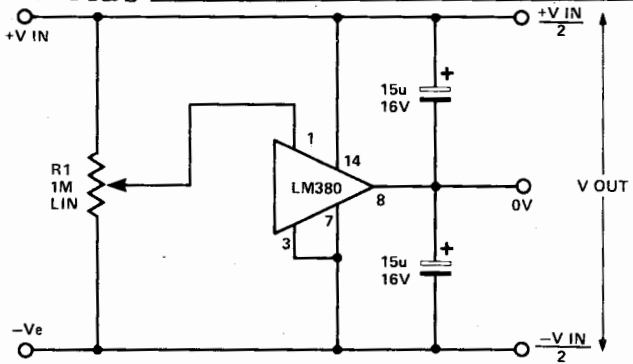
Width reduction	C1
3 ms	8 u
5 ms	4 u
9 ms	1 u
9.5 ms	470 n
9.9 ms	100 n

Before the input pulse is applied, the output of IC1c is low and so IC2b's output is high. The circuit output is thus low.

When the pulse is applied, the output of IC1c starts to rise, but the output of the circuit remains low because of the high on the output of IC2a. When C1 charges the threshold voltage of IC2a, the output of IC2a will go low and the output of IC2b will go low while the input to the circuit is still high. Thus the start of the pulse is delayed by the amount of time taken for C1 to charge.

Tech-Tips is an ideas forum and is not aimed at the beginner; we regret that we cannot answer queries on these items. We do not build up these circuits prior to publication.

ETI is happy to consider circuits or ideas submitted by readers; all items used will be paid for. Drawings should be as clear as possible and the text should be preferrably typed. Anything submitted should not be subject to copyright. Items for consideration should be sent to the Editor.



Simple Dual Power Supply

L Swann

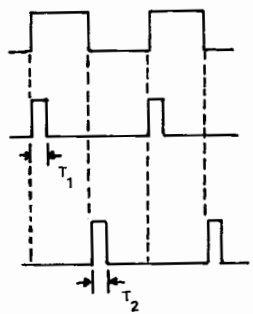
This circuit offers a cheap and simple way of obtaining a split power supply (for Op-amps etc.), utilising the quasi-complementary output stage of the popular LM380 audio power IC.

The device is internally biased so that with no input the output is held mid-way between the supply rails.

R1, which should be initially set to mid-travel, is used to nullify any inbalance in the output. Regulation of V_{OUT} depends upon the circuit feeding the LM380, but the positive and negative outputs will track accurately irrespective of input regulation and unbalanced loads.

The free-air dissipation is a little over 1 watt, and so extra cooling may be required. The device is fully protected and will go into thermal shutdown if its rated dissipation is exceeded, current limiting occurs if the output current exceeds 1A3.

The input voltage should not exceed 20 V.

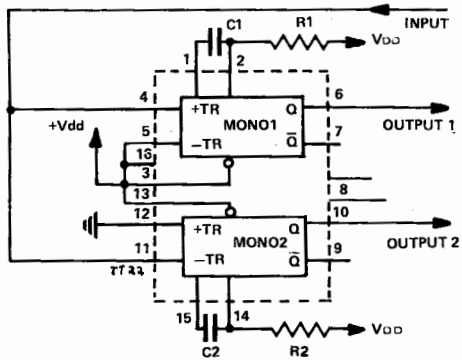


Dual One - Shot Discriminates trailing and Falling Edges Of Data Signals

Noel Boutin, Sherbrooke University

Many circuits have been published in the past which can be classified as transition detectors. They produce an output pulse each time a state change occurs at their input. The proposed circuit have two output ports. On the first one, a short pulse, the duration of which being adjustable by an external RC network, is produced each time a transition from a logical "0" to a logical "1" is detected at its input. In fact, the circuit is a monostable triggered by trailing edge of data input. On the second output port, a short pulse, also adjustable, is produced each time a transition from a logical "1" to a logical "0" is detected at its input. This second part of the discriminator is another monostable triggered, this time, by the falling edge of the input signal.

As shown in figure, the only components need is an IC dual monostable multivibrator such as the CD4098 or MC14538 and two RC networks.



WORKING WITH MONOSTABLE MULTIVIBRATORS

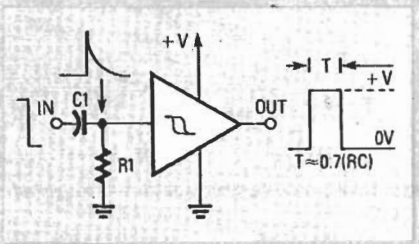


FIG. 1—THIS LEADING-EDGE DETECTOR circuit has a positive output pulse.

RAY MARSTON

Learn how to design and build pulse generators and monostable multivibrators, and how to use them in your projects.

CIRCUIT DESIGNERS often need to come up with a circuit to generate a pulse when triggered by the leading or trailing edge of a waveform. When the pulse width is not critical, they usually turn to a circuit element that's known as a *half-monostable* or *edge-detector*. When the pulse width is critical, they usually use a circuit element known as a *full-monostable multivibrator*.

There are two types of monostables, standard and retriggerable. In a standard monostable circuit, the arrival of the trigger signal initiates an internal timing cycle that causes the output of the monostable to change state at the start of the timing cycle, and then revert back to the original state on completion of the cycle. Note that once a timing cycle has been initiated, the standard monostable is immune to the effects of subsequent trigger signals until the timing period ends. That type of circuit can be modified by adding a RESET control, so that the output pulse can be terminated or aborted at any time.

In a retriggerable monostable circuit, the trigger signal actually resets the monostable and initiates a new timing cycle even if the trigger signal arrives in the midst of an existing cycle. Thus, the retriggerable monostable's output will stay in its active state as long as new trigger pulses are introduced before the timing cycle ends.

The choice of an IC to implement a pulse generator is usually dictated by economics and convenience, rather than by the actual design requirements. So, if the designer needs a standard CMOS monostable of only modest precision, he can build it very inexpensively using IC's such as a 4001B or 4011B. Otherwise, it can be done at a greater expense using a 555 timer or a dedicated monostable IC such as 4047B.

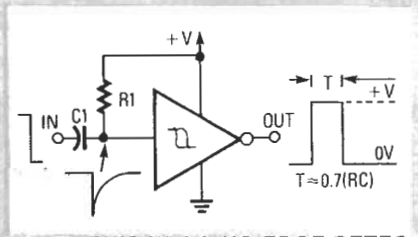


FIG. 2—THIS TRAILING-EDGE DETECtor circuit also has a positive output pulse.

Edge-detector circuits

Edge-detector circuits are used to generate an output pulse on the arrival of either the leading or trailing edge of a rectangular input waveform. In most applications, the precise width of the output pulse is not critical. The basic method of making an edge-detector is to feed the input waveform to a short-time-constant RC network, which produces an output waveform with a sharp leading edge and an exponential trailing edge upon the arrival of each input edge. The unwanted edge waveform is then eliminated with a discriminator diode, and the remaining spike or sawtooth waveform is then converted into a clean pulse by feeding it through a Schmitt-trigger.

CMOS Schmitt IC's incorporate built-in protection diodes on all input terminals, which can be used as discriminator diodes as was previously described. The 4093B quad 2-input NOR Schmitt can be used as a normal Schmitt inverter by wiring one input terminal to the positive supply and using the other terminal as the input. Also, a non-inverting Schmitt trigger can be made by wiring two inverting Schmitts in series.

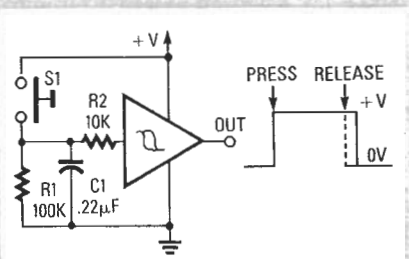


FIG. 3—IF YOU NEED A NOISELESS push-button switch, this circuit can be used to de-bounce a switch.

Figure 1 shows a leading-edge detector circuit. The input of the Schmitt is tied to ground via R1, and the RC time constant is relatively short compared to the period of the input waveform. As shown, the leading edge of the input signal is converted to the spike waveform, and the spike is then converted into a pulse waveform by the Schmitt. The circuit will generate a positive-going output pulse if a non-inverting Schmitt is

used, or a negative-going output pulse with an inverting Schmitt. In either case, the output has a period (T) of roughly 0.7(RC). Figure 2 is a similar circuit that is set up as a trailing-edge detector.

An edge-detector circuit can be used to make a "noiseless" push-button switch as shown in Fig. 3. The input of the non-inverting Schmitt is tied to ground via timing-resistor R1 and by input-protection-resistor R2, so the output of the circuit is normally low. When S1 is closed, C1 charges almost immediately to the positive supply voltage, and the Schmitt output goes high. When S1 is released, C1 discharges relatively slowly via R1, and the Schmitt output does not return low until roughly 20 ms later. Therefore, the circuit provides a clean output waveform.

The reset-pulse generator circuit in Fig. 4 generates a reset pulse when power is first applied to the circuit. The circuit produces a 700-ms output pulse for resetting external circuitry. When power is first applied, C1 is discharged, pulling the Schmitt input low and driving the output high. Capacitor C1 then charges via R1 until, after about 700 ms, the C1 voltage rises to such a level that the Schmitt output switches low.

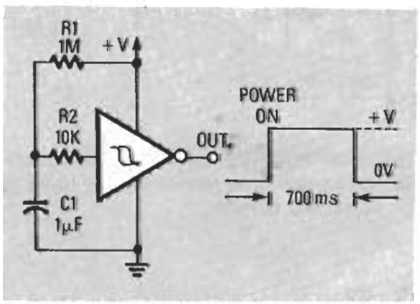


FIG. 4—A RESET-PULSE generator circuit will generate a reset pulse upon power up.

Monostable IC's

The cheapest possible way of building a standard or resettable monostable circuit is to use a 4001B quad 2-input NOR gate or a 4011B quad 2-input NAND gate; circuits using those IC's are shown in Figs. 5–8. Note, however, that the output pulse widths of those circuits are subject to variations between individual IC's and variations in the supply voltage, so they are not suitable for use in high-precision applications.

Figures 5 and 6 show two versions of the standard monostable circuit,

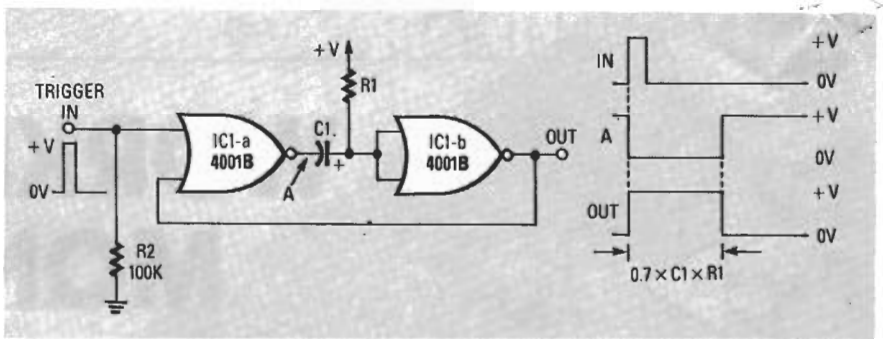


FIG. 5—THIS 2-GATE NOR monostable is triggered by a positive-going signal and generates a positive-going output pulse.

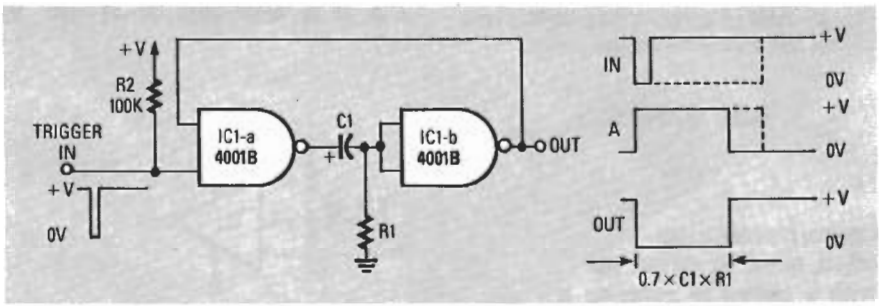


FIG. 6—THIS 2-GATE NAND monostable is triggered by a negative-going signal and generates a negative-going output pulse.

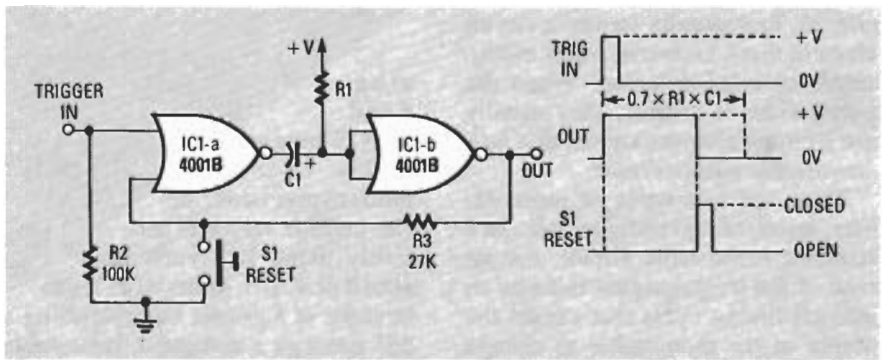


FIG. 7—A RESETTABLE NOR monostable can be reset by pressing S1. It is triggered by a positive-going signal and produces a positive-going pulse.

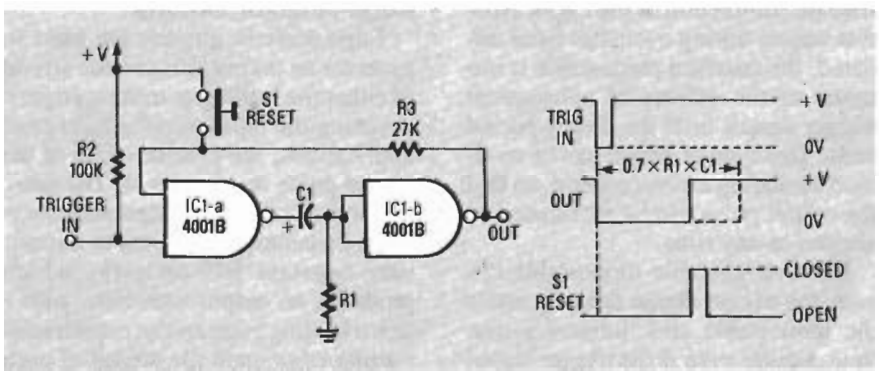


FIG. 8—THE CIRCUIT SHOWN HERE is a NAND monostable. Unlike the NOR-type, it is triggered by a negative-going signal and produces a negative-going pulse.

each using only two of the four gates that are available in the CMOS package. The duration of the output pulse is determined by the values of R1 and C1, and is approximately 0.7 × C1 × R1. When R1 has a value of 1.5 megohms, the period of the pulse is approximately one-second-per-μF of C1's value. In practice, C1 can have any value from about 100 pF up to a few thousand μF, and R1 can have any value from 4.7K to 10 megohms. The NOR version of the circuit (Fig. 5) has a normally-low output, and is trig-

gered by the edge of a positive-going input signal, while the NAND version (Fig. 6) has a normally-high output and is triggered by the edge of a negative-going input signal.

One good feature of those circuits is that the input trigger pulse can be direct coupled, and the duration of the trigger pulse has little effect on the length of the generated output pulse. Another useful feature is that the signal appearing at point A has a period equal to that of either the output pulse or the input trigger pulse, whichever is greater. That feature is valuable when making pulse-length comparators and over-speed alarms.

The operating principles of those two circuits are fairly simple. Let's look first at the circuit in Fig. 5, where IC1-a is wired as a NOR gate and IC1-b is wired as an inverter. When the circuit is in the quiescent stage, the trigger-input terminal is held low by R2, and the output of IC1-b is also low. Both inputs of IC1-a are low, so the output of IC1-a is forced high and C1 is discharged. When a positive trigger signal is applied to the circuit, the output of IC1-a is immediately forced low and, since C1 is now discharged, it pulls the input of IC1-b low and drives its output high. The output of IC1-b is coupled back to the input of IC1-a, and forces the output of IC1-a to remain low, irrespective of the prevailing state of the input trigger signal. As soon as the output of IC1-a switches low, C1 starts to charge up via R1, and after a delay determined by the values of those components, C1's voltage rises to such a level that the output of IC1-b starts to swing low, terminating the output pulse. The circuit will not return to its quiescent state if the trigger signal is high when the output pulse is terminated.

The circuit in Fig. 6 operates like the one in Fig. 5, except that IC1-a is wired as a NAND gate, with its trigger input tied to the positive supply via R2, and the timing-resistor R1 is connected to ground.

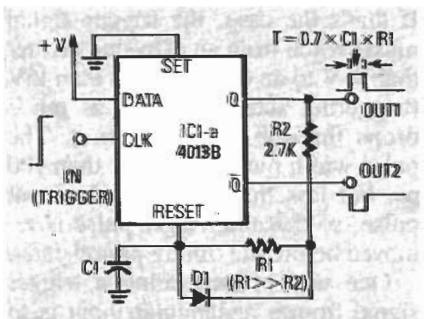


FIG. 9—A D-TYPE FLIP-FLOP can be used as a monostable. It produces both negative- and positive-going pulses.

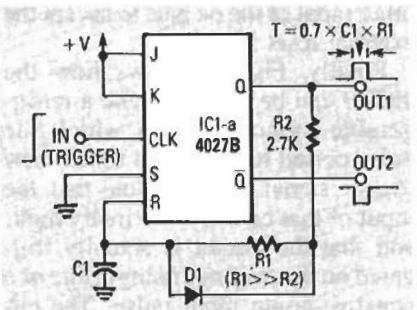


FIG. 10—A JK-TYPE FLIP-FLOP can also be used as a monostable. Its operation is similar to the D-type in Fig. 9.

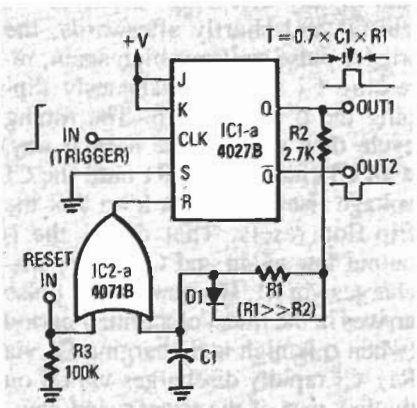


FIG. 11—THIS JK-TYPE monostable is electronically resettable.

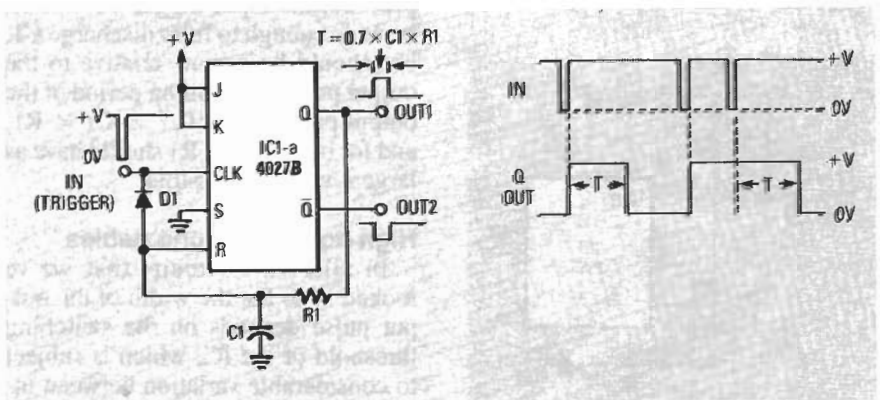


FIG. 12—A RETRIGGERABLE JK-type monostable has an output pulse that can be prolonged by an additional trigger pulse before the timing cycle ends.

The circuits in Figs. 5 and 6 have their outputs coupled directly to one input of IC1-a to effectively maintain a trigger input once the original trigger signal is removed, thereby providing semi-latching operation.

The circuits in Figs. 5 and 6 can be made resettable by providing them with a means of breaking the feedback path, as shown in Figs. 7 and 8. The feedback connection from the output of IC1-b to the input of IC1-a is made via R3. Consequently, once the circuit has been triggered, and the original trigger signal has been removed, the circuit can be reset by forcing the feedback input of IC1-a to its normal quiescent state by pressing S1. In practice, S1 can be replaced with a transistor, enabling the circuit to be reset electronically.

Flip-flop monostables

Medium-accuracy monostable circuits can be built using standard edge-triggered CMOS flip-flop IC's, such as the 4013B dual D-type or the 4027B dual JK-type, in the configurations shown in Figs. 9 and 10. Both circuits operate in the same basic manner, with the IC wired in the divider mode by proper connection of their control terminals (DATA and SET in the 4013B, and J, K and SET in the 4027B), but with the Q terminal connected to RESET by an RC time-delay network. The operating sequence of both circuits is as follows:

When the circuit is in its quiescent state, the Q output terminal is low and discharges timing capacitor C1 via R2 and the parallel combination of R1 and D1. Upon the arrival of a sharply rising leading edge on the CLK terminal, the Q output flips high, and C1 starts to charge up via the series combination of R1 and R2. Eventually, after a delay determined mainly by values of C1 and R1, the C1 voltage rises to such a value that the flip-flop is forced to reset, driving the Q terminal low again. Capacitor C1 then discharges rapidly via R2 and the D1/R1 network, and the circuit is ready to generate another output pulse when the next trigger signal arrives.

The timing period of the circuits in Figs. 9 and 10 is roughly equal to 0.7 × C1 × R1, and the reset period (the

time for C1 to discharge after each pulse) is roughly equal to C1 × R2. In practice, R2 is used mainly to prevent degradation of the trailing edge of the pulse waveform as C1 discharges; R2 can be replaced by a jumper if degradation is acceptable. Note that the circuit generates a positive-going output pulse at Q, and a negative-going pulse at $\overline{Q}$.

The circuit in Fig. 10 can be made resettable as shown in Fig. 11. That is done by connecting capacitor C1 to the RESET terminal of the circuit via one input of an OR gate, and using the other input of the OR gate to accept the external reset signal.

Finally, Fig. 12 shows how the 4027B can be used to make a retriggerable monostable, in which the pulse period restarts each time a new trigger signal arrives. Note that the input of that circuit is normally high, and that the circuit is actually triggered on the trailing (rising) edge of a negative-going input pulse. The circuit operates as follows:

At the start of each timing cycle, the input trigger pulse switches low and rapidly discharges capacitor C1 via D1 and shortly afterwards, the trigger pulse switches high again, releasing C1 and simultaneously flipping the Q output high. The timing cycle then starts in the normal way, with C1 charging via R1 until the C1 voltage rises to such a level that the flip-flop resets. That drives the Q output low again and C1 slowly discharges via R1. If a new trigger pulse arrives in the midst of a timing period (when Q is high and charging C1 via R1), C1 rapidly discharges via D1 on the low part of the trigger, and commences a new timing cycle as the input waveform switches high again. In practice, the input trigger pulse must be wide enough to fully discharge C1, but should be narrow relative to the output pulse. The timing period of the output pulse equals 0.7 × C1 × R1, and for best results, R1 should have as large a value as possible.

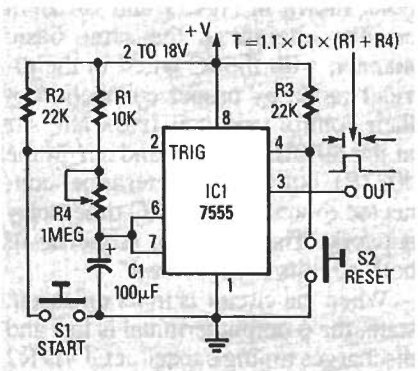


FIG. 13—THIS MONOSTABLE can be manually-triggered and has a variable pulse width from 1.1 to 100 seconds.

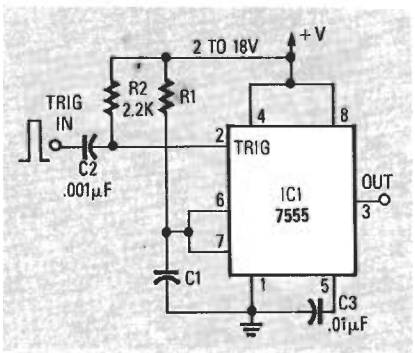


FIG. 14—THIS 7555 MONOSTABLE is similar to the one in Fig. 13, with the exception that it can be electronically triggered.

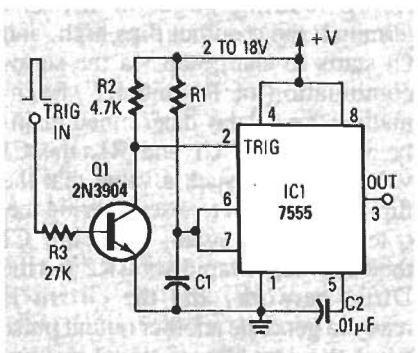


FIG. 15—A PULSE-TRIGGERED 7555 monostable can produce an accurate output pulse from a medium-accuracy input signal.

High accuracy monostables

In all of the circuits that we've looked at so far, the width of the output pulse depends on the switching threshold of the IC, which is subject to considerable variation between individual IC's, and variations in supply voltage and temperature. Therefore, the circuits have only moderate accuracy. If precise pulse widths are needed, the best way of generating them it is to use a 7555 IC, which is the CMOS version of the ubiquitous 555 timer. It has a built-in precision voltage comparator that activates internal flip-flops and precisely controls the output pulse width, irrespective of wide variations in supply voltage and temperature. The 7555 can operate from supplies that range from 2 volts to 18 volts.

Figure 13 shows the basic way of using the 7555 as a manually triggered variable-pulse generator. The IC is triggered by briefly pulling pin 2

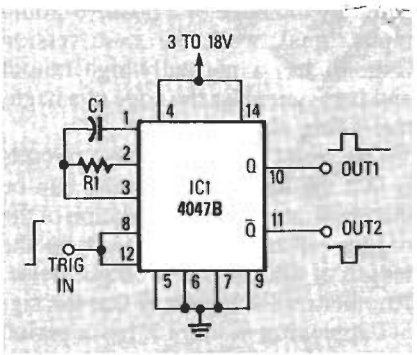


FIG. 16—THE 4047B can be used as a retriggerable monostable, with positive-edge triggering.

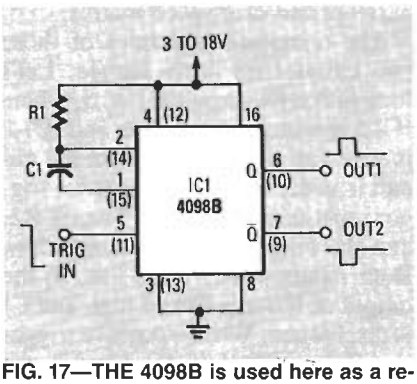


FIG. 17—THE 4098B is used here as a retriggerable monostable with negative-edge-triggering.

low (less than ⅓V) via S1. At that time, the output (pin 3) switches high and the IC enters its timing cycle, with C1 charging up via the R1/R4 circuit. Eventually, after a delay of 1.1 × C1 × (R1 + R4), C1's voltage rises to the upper switching threshold (⅔ V), and the output abruptly switches low, ending the timing cycle. The timing cycle can be terminated prematurely by briefly pulling RESET (pin 4) low via S2. The circuit can produce a pulse from 1.1 to 100 seconds; the duration is controlled by R4.

In most practical applications using the 7555 the designer will want to trigger the IC electronically, rather than manually (by pressing a button). If that's the case, the trigger signal must switch from an off value greater than ⅔V to an on value less than ⅓V (triggering actually occurs as pin 2 drops through the ⅓V value). The pulse width must be greater than 100 ns, but less than the desired output pulse, so that the trigger pulse is removed before the timing period ends.

One way of generating a trigger signal from a rectangular input is to connect the signal to pin 2 of the 7555 via a short-time-constant RC dif-

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