BY CLEMENT S. PEPPER

A MONOSTABLE CATALOG for Experimenters

A guide to today's IC monostable multivibrators emphasizes their usefulness in practical applications

MONOSTABLE multivibrators, sometimes called "one-shots," are electronic circuits that, when triggered, deliver an output pulse of a predetermined width.

Although today's IC monostables still provide the one-shot function, their usefulness has been greatly extended. These modern devices feature multiple inputs with both positive- and negative-edge triggering, complementary outputs, retriggerability and resetability. They are also very easy to use, lower in cost, and available in conventional and low-power TTL and CMOS.

The key features of a number of popular monostables are summarized in the "Catalog." The information is sufficient to enable using the mono without recourse to a data sheet. Summaries of the 555 and 558/559 timers (which can function as a one-shot) are included separately in Figs. 3 and 5.

Triggering. All of the monos in the catalog will trigger from a high-to-low or from a low-to-high transition. For triggering to actually occur on the transition, all inputs must conform to defined logic states. These states are shown in the "Input Table" for each device.

The logic tables in the manufacturers data sheets include inhibit as well as trigger conditions. Only trigger conditions are shown in the Catalog. Any other state is an inhibit.

Each line of the table defines a trigger mode for a "one-shot" output. "A" and "B" designators are used in the Input Tables. Several monos have multiple A and/or B inputs though not all manufacturers use this notation. An "A" input is defined as a high-to-low transition (shown as a down arrow), while a "B" input is defined as a low-to-high transition (shown as an up arrow). The CMOS 4098B/4528/14528 are exceptions—the A and B transitions being reversed.

The A and B inputs have a defined logical relationship to each other, but these are not consistent between devices. You should go by the Input Table for the mono being used. Triggering occurs at a voltage level independent of the transition time, while rise and fall times are consistent with the type of logic family.

The 74121 and the 74LS221 feature Schmitt circuitry at their B input. They trigger with a 1-volt/s rise time, and provide 1.2 volts of noise immunity.

All of the monos shown provide complementary outputs. The Q output is normally low and goes high for the pulse duration. The not-Q output is normally high and goes low. Pulse width is identical for both outputs.

The minimum pulse widths and delay times listed are subject to some conditions. They are included to provide a generalized picture of limiting conditions. If nanosecond timing is critical to your application, consult the manufacturer's data sheet.

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Pulse Timing. A typical timing equation has the form tw=k*RC* where tw is the pulse width in nanoseconds, k is a constant, *R* is the timing resistance in kilohms, and *C* is the timing capacitance in picofarads.

For example, the pulse width for the 74121 is given as tw=.693*RC*. Assume that *R* is 10,000 ohms, and *C* is 100 pF. Then the equation is tw=.693(10)(100) =693 ns or .693 μs.

Retriggering. Some monos are retriggerable. That is, if a second trigger arrives while the output is still high from the first pulse, the output will respond to the latest trigger and remain high. The extension is for one complete cycle and a train of input triggers will result in a sustained output pulse that will have a very long duration.

Retriggering may be accomplished from either the A or B inputs, simply or intermixed. This makes for some intriguing timing possibilities.

However, there is a time restriction on retriggering some monos. As shown in the Catalog, the required delay is the number in parenthesis following "re-triggerable." Thus, the 74123 cannot be retriggered before 0.22 ns after the previous input.

Retriggering is useful when you want it, but on the other hand, what do you do if you don't want it? Suppose, for example, you are using a 74123 dual mono because you need retrigger for one circuit, but you cannot live with it in the other. In this case, connect the B input to the not-Q output and trigger with the A input (or vice versa). When the mono triggers, B is pulled low thus inhibiting further triggering until the circuit times out. Be sure, however, that the A input(s) are in the inhibit mode at the time out, or you will have an oscillator instead of a mono.

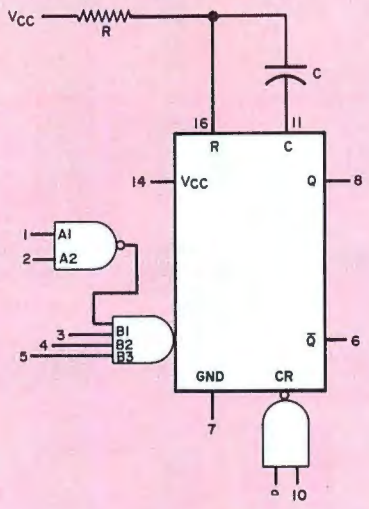
Reset. Some monos, but not all, provide for reset. This is implemented by applying a reset pulse to the CR (clear) input. The leading edge of this pulse resets the outputs to the initial state, and another trigger is required to obtain an output.

If the CR input is held in the reset state, the mono is inhibited and will not respond to an input trigger. This feature adds flexibility to the controlling logic for the mono.

R and C Limits. All monos have upper and lower limits for the range of resistance (R), while some have limits on

MONOSTABLE CATALOG-1

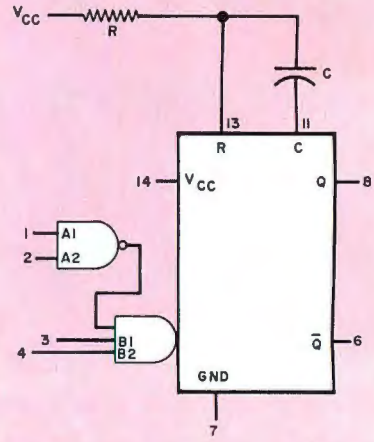
9600 SINGLE TTL



INPUT TABLE					FEATURES
A_1	A_2	B_1	B_2	B_3	RETRIGGERABLE (0.3Cns)
↓	1	1	1	1	RESET ON LOW TO
1	↓	1	1	1	EITHER "CR" INPUT
0	X	↑	1	1	t_{min}= 74 ns
X	0	↑	1	1	t_{pd}=29 ns
0	X	1	↑	1	LIMIT ON R=
X	0	1	↑	1	5k ⩽ R ⩽50k
0	X	1	1	↑	(0 ⩽ T°C ⩽75)
X	0	1	1	↑	LIMITS ON C:
					NONE

t_w=0.32RC (1+0.7/R)

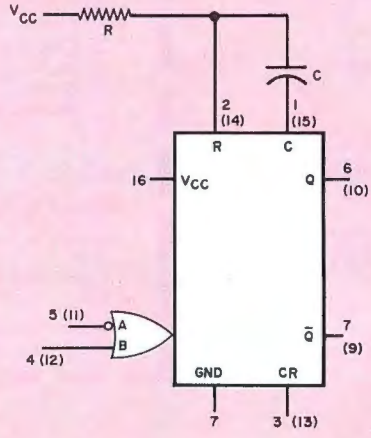
9601 SINGLE TTL



INPUT TABLE				FEATURES
A_1	A_2	B_1	B_2	RETRIGGERABLE (0.3Cns)
↓	1	1	1	NOT RESETTABLE.
1	↓	1	1	t_{min}=45 ns.
0	X	↑	1	t_{ps}=25ns.
X	0	↑	1	LIMITS ON R:
0	X	1	↑	5k ⩽ R ⩽50k
X	0	1	↑	(0 ⩽ T°C ⩽75)
				LIMITS ON C:
				NONE

t_w=0.32RC (1+0.7/R)

9602 DUAL TTL

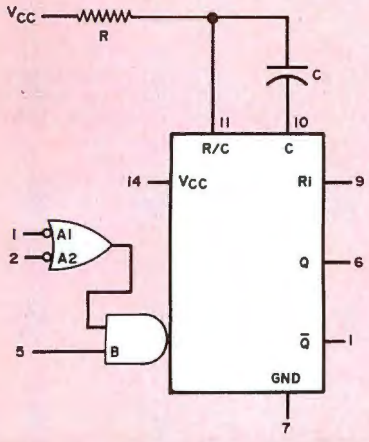


INPUT TABLE		FEATURES
A	B	RETRIGGERABLE (0.3Cns)
↓	0	RESET ON LOW TO "CR"
1	↑	t_{min}=72 ns
		t_{pd}=25 ns
		LIMITS ON R:
		5k ⩽ R ⩽50k
		(0 ⩽ T°C ⩽75)
		LIMITS ON C:
		NONE

t_w=0.31RC (1+1/R)

MONOSTABLE CATALOG-2

74121 SINGLE TTL



INPUT TABLE		
A_1	A_2	B
0	X	↑
X	0	↑
↓	X	1
X	↓	1

t_w=0.693 RC
TO USE THE INTERNAL TIMING RESISTOR, CONNECT PIN 9 TO V_{cc}.
FOR C=0, t_w=30 ns.

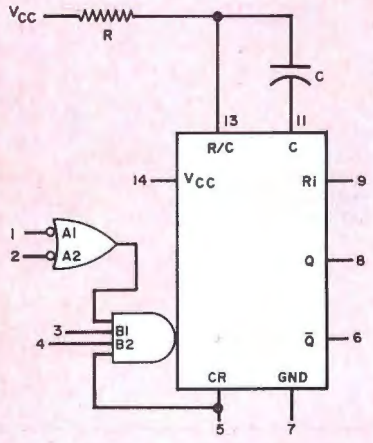
FEATURES
NOT RETRIGGERABLE
NOT RESETTABLE
"B" IS A SCHMITT INPUT
t_{min}=30 ns
t_{pd}=45 ns
R_{int}=12 kΩ
LIMITS ON R:
1.4k ≤ R ≤ 40k
(0 ≤ T°C ≤ 70)
LIMIT ON C:
0 ≤ C ≤ 1000 µF

74122 SINGLE TTL

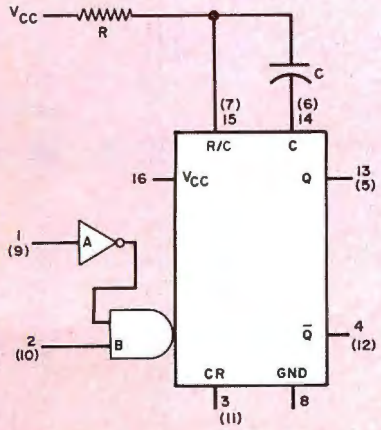
INPUT TABLE			
A_1	A_2	B_1	B_2
0	X	↑	1
0	X	1	↑
X	0	↑	1
X	0	1	↑
1	↓	1	1
↓	↓	1	1
↓	1	1	1

t_w=0.32 RC (1+0.7/R)
TO USE THE INTERNAL TIMING RESISTOR CONNECT PIN 9 TO V_{cc}.

FEATURES
RETRIGGERABLE (0.22 ns)
RESET ON LOW TO "CR"
t_{min}=40 ns
t_{pd}=21 ns
LIMITS ON R:
5k ≤ R ≤ 50k
(0 ≤ T°C ≤ 70)
LIMITS ON C:
NONE



74123 DUAL TTL



INPUT TABLE	
A	B
0	↑
↓	1

t_w=0.32 RC (1+0.7/R)

FEATURES
RETRIGGERABLE (0.22 ns)
RESETS ON LOW TO "CR"
t_{min}=40 ns
t_{pd}=21 ns
LIMITS ON R:
5k ≤ R ≤ 50k
(0 ≤ T°C ≤ 70)
LIMITS ON C:
NONE

capacitance (C). Typical limits for industrial devices are shown in the Catalog.

In general, try to stay away from maximum values of *R*, especially when using electrolytic capacitors for *C*.

Conventional electrolytics and aluminum electrolytics can be a problem. Most high-quality tantalums perform well. Inserting a silicon diode between the *R/C* terminal and the *RC* junction as shown in Fig. 1, will eliminate any leakage problem that may occur with reverse voltage across the capacitor. However, if you use this diode, the value of *R* must be reduced to less than 60% of its maximum value. Some circuits do use tantalums without the diode, but with reduced values of *R*. If your circuit has to operate at elevated temperature, be cautious.

Avoiding Problems. The greatest single source of problems is false triggering, and the second is no triggering at all.

IC monostables are very fast, and according to "Murphy's Law" if the inputs can couple to form a "glitch" generator, they will. Therefore, input lines should be kept short and isolated from neighboring lines to avoid the unwanted stray coupling.

A 0.1-µF or larger capacitor should be connected between the Vcc and ground right at the IC. The upper trace of Fig. 2 shows large "spikes" riding on the leading edge of each waveform. After installing the bypass capacitor, the signal cleared up as shown in the lower trace.

Using a scope whose ground lead is connected to the power supply ground, take a look at the signal ground line to make sure that it really is ground. It shouldn't be riding a half a volt or so above ground, or displaying a lush growth of grass (noise).

Always make the foil traces for Vcc and ground heavier than pin interconnections. This keeps their resistance low and current pulses passing through them do not develop voltage drops that can appear as signals to other devices connected to the lines.

If possible, test your mono outside the circuit, using the timing values you require. Don't forget the minimum retriggering time.

The 555. This timer IC, as well as the 558/559, do not conform to the standard monostable format and were not included in the Catalog. However, these timer ICs can be used as one-shots or as free-running or gated oscillators.

They do have limitations, though: they are slow when compared to the other monos, and pulses narrower than 10 μs are best obtained with a TTL device. Also, they're not retriggerable; and in the free-running mode, they have a duty-cycle limitation.

They do, however, have a single output, can operate with a wide range of supply voltages, and can sink or source 200 mA (which can save a driver transistor).

The use of a 555 as a one-shot or free-running oscillator is shown in Fig. 3. The capacitor connected to CV (pin 5) is essential to reduce noise.

In the mono mode, calculations are based on $t_W = 1.1RC$. For these timers, *R* is shown in ohms, *C* in farads and t is in seconds.

For any timing circuit, it is best to use a standard value of capacitance for *C*, then calculate the required resistance. It's always possible to combine different standard resistances in series, parallel or combinations, but it is difficult to locate an odd value of capacitance.

For the free-running mode, there are four defining equations:

$D = Rb/(Ra + 2Rb) = t2/t1 =$ duty cycle
$t1 = 0.693(Ra + Rb)C =$ output high time
$t2 = 0.693RbC =$ output low time
$T = 0.693(Ra + 2Rb)C = t1 + t2$

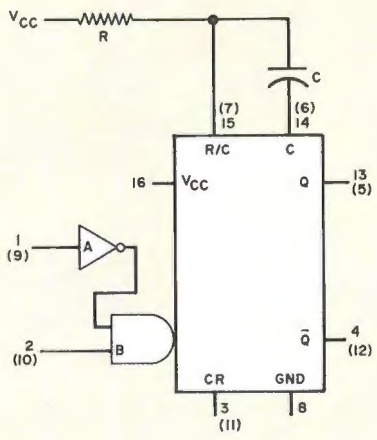
In the equation for D, note that if *Ra* is zero, then D becomes 0.5. This tells you not to try to get a square-wave output as you have to tie DS (pin 7) directly to Vcc. There is no internal current-limiting resistor within the chip, so do not try this. Select D as 0.25 or 0.3 for most cases.

It's usually best to start by selecting a value of *C* appropriate to the frequency and duty cycle. *Rb* is then computed using the equation for t2, and this is plugged into the D equation to solve for *Ra*. Then solve for T as a check on the values.

There are several ways to generate a square wave. The circuit shown in Fig. 3E allows a wide selection of both frequency and duty cycle from a single capacitor. This is illustrated by the composite scope traces shown in Fig. 4. In the circuit, *R1* was 2200 ohms, *R2* was a 10,000-ohm potentiometer and *C* was a 0.01-μF capacitor. The three traces represent three settings of *R2*. Overall frequency range was from 5 to 80 kHz. If trimmer potentiometers were used for both *R1* and *R2*, the frequency and duty cycle could be trimmed to the exact requirements.

MONOSTABLE CATALOG-3

74LS221 DUAL LSTTL

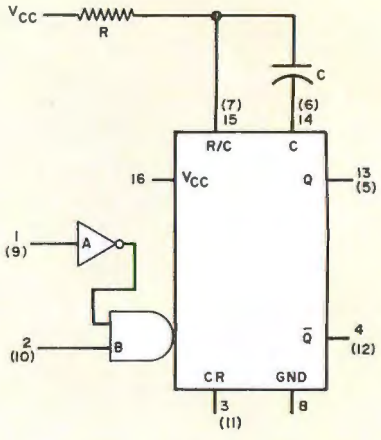


INPUT TABLE	
A	B
0	↑
↓	1

$t_W = RC\ (3.03\ RC)$

FEATURES
NOT RETRIGGERABLE
RESETS ON LOW TO "CR"
t_W RANGE=30 ns to 70 s
t_{pd}=45 ns
LIMITS ON R
1.4k ⩽ R ⩽ 100k
(0 ⩽ T°C ⩽ 70)
LIMITS ON C
0 ⩽ C ⩽ 1000 μf
SCHMITT INPUT ON "B"

74C221 DUAL CMOS

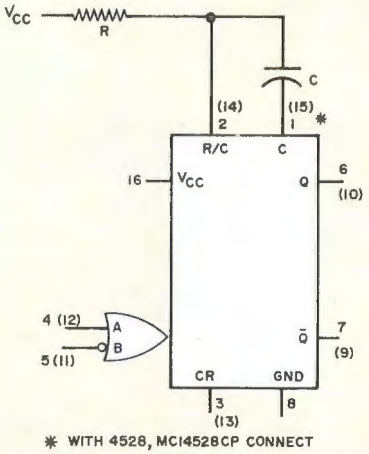


INPUT TABLE	
A	B
0	↑
↓	1

$t_W = RC$
REFERENCE:
AN-138 "USING THE CMOS DUAL MONO. MULTIVIBRATOR"
NATIONAL SEMICONDUCTOR

FEATURES
NOT RETRIGGERABLE
RESETS ON LOW TO "CR"
$t_W$min=50 ns, V_{cc}=5V
=30 ns, V_{cc}=10V
t_{pd} =250 ns, V_{cc}=5V
=120 ns, V_{cc}=10V
LIMITS ON R:
10k ⩽ R ⩽ 350k
(V_{cc}=5V
5k ⩽ R ⩽ 350k
(V_{cc}=10V)
NO LIMITS ON C.

4098B/4528B/MC14528CP DUAL CMOS



* WITH 4528, MC14528CP CONNECT PINS 1 AND 15 TO PIN 8.

INPUT TABLE	
A	B
0	↓
↑	1

$t_W = 0.2\ RC\ (\log_e V_{cc})$
$\log_e 5 = 1.61$
10=2.30
15=2.71

FEATURES
RETRIGGERABLE (0 ns)
RESETS ON HIGH TO "CR"
$t_W$min=75 ns (5V) } 4098B
25 ns (15V) }
240 ns (5V) } 4528, 14528
90 ns (15V) }
t_{pd}=300 ns (5V)
125 ns (10V)
100 ns (15V)
LIMIT ON R
5k ⩽ R ⩽ 1000k
(-40 ⩽ T°C ⩽ 85)
NO LIMIT ON C

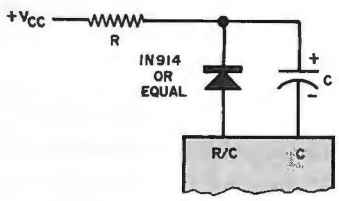


Fig. 1. Use of a diode prevents high inverse leakage currents through the timing capacitor.

The period is linear with respect to *C*. A substitution of a 0.1-μF capacitor reduced the frequency by a factor of 10 while preserving the duty cycle. This circuit allows for a low-cost pulse generator with lots of flexibility.

The 558/559 Timers. These are quad timers having a range of a few microseconds to a few hours. Each of the four monos are independent, but they share a common reset. They are edge-triggered, and several sections can be coupled in tandem to produce an output several hours long.

A function diagram and important features of these timers are shown in Fig. 5. The 558 has an open collector output (Fig. 5D) while the 559 has a Darlington follower output (Fig. 5E). In all other respects, the two are identical.

The output pulse width is the *RC* product of the timing components. Two devices may be cross-coupled to operate in the free running mode as shown in Fig. 5C. The potentiometer connected to the CV line allows adjustment of the output pulse width and duty cycle. The CV voltage range is from 0.5 V to Vcc minus 1 volt.

Applications. A simple pulse can be created by *RC* coupling between gates or flip-flops. Although this approach will work, it is marginal at best. For example, take a look at the circuit shown in Fig. 6A. Operation depends on the overshoot at the trailing edge. The system malfunctioned because the overshoot was marginal. Also, 750 ohms is too small a pulldown for TTL, and the circuit is susceptible to noise because there can be a volt or more of dc offset at the input.

If a 74123 dual mono had been used, as in the circuit shown in Fig. 6B, the time delay could have been achieved at

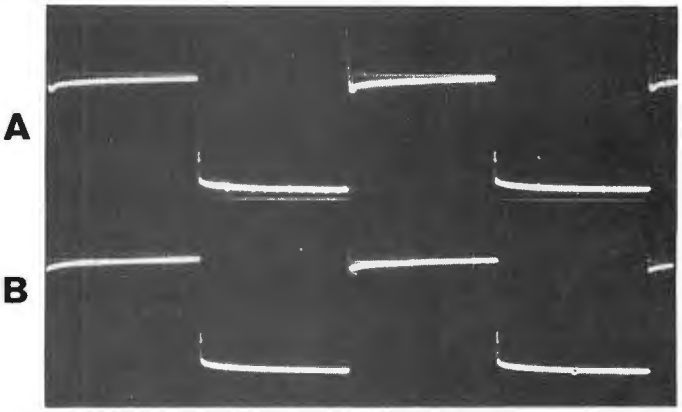
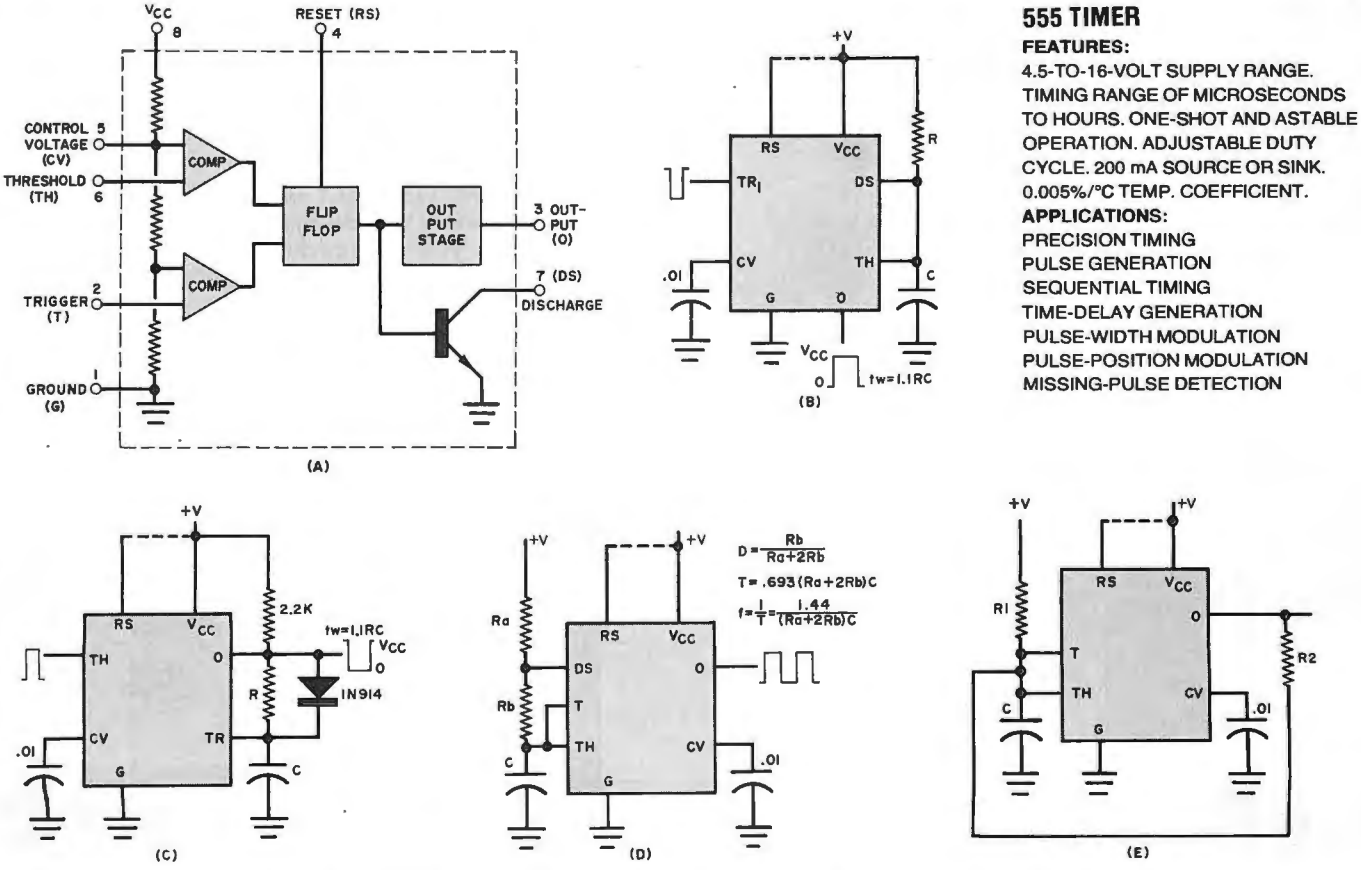


Fig. 2. A 2-volt spike on leading edge of waveform (A) is removed (B) by using a bypass capacitor from V_{cc} to ground.



555 TIMER

FEATURES:
4.5-TO-16-VOLT SUPPLY RANGE. TIMING RANGE OF MICROSECONDS TO HOURS. ONE-SHOT AND ASTABLE OPERATION. ADJUSTABLE DUTY CYCLE. 200 mA SOURCE OR SINK. 0.005%/°C TEMP. COEFFICIENT.

APPLICATIONS:
PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME-DELAY GENERATION
PULSE-WIDTH MODULATION
PULSE-POSITION MODULATION
MISSING-PULSE DETECTION

Fig. 3. The 555 timer function diagram (A), positive output with negative trigger (B), negative output for positive trigger (C), astable operation (D), and astable operation for a 50% duty cycle (E).

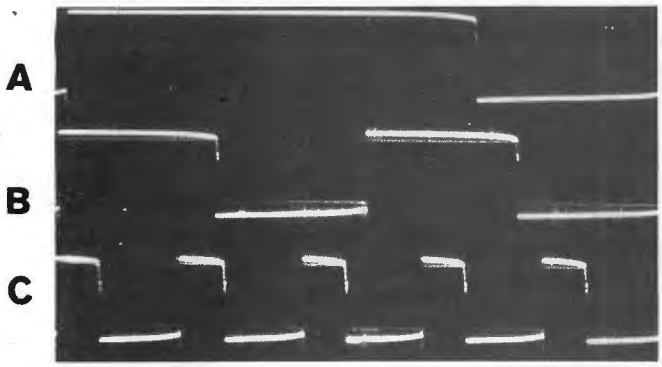
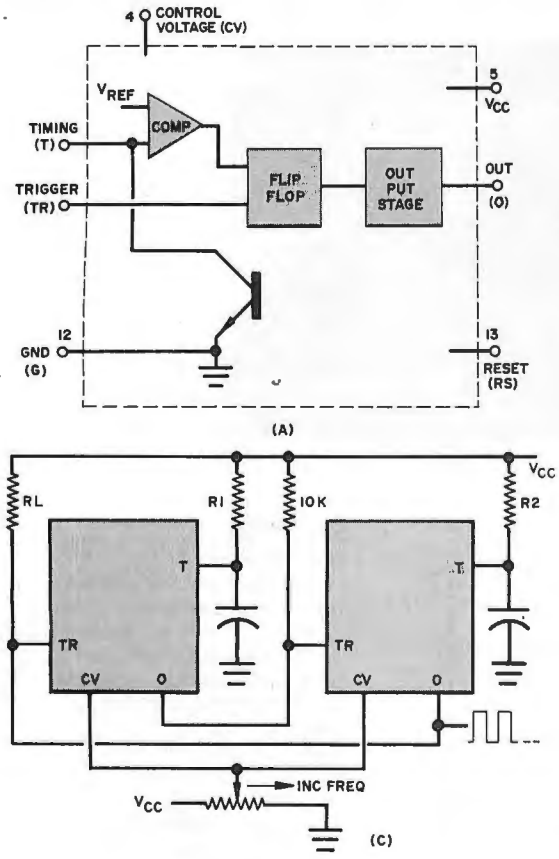


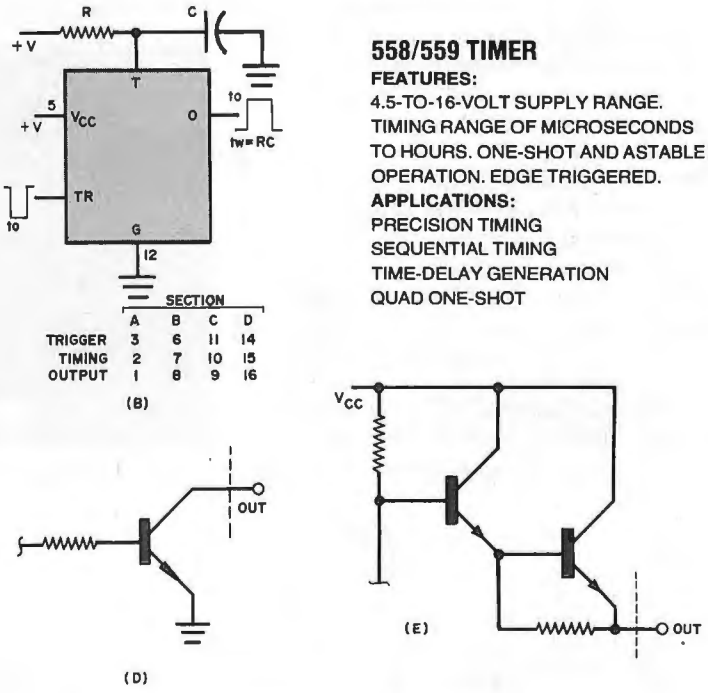
Fig. 4. Waveforms for various values or R2 in Fig. 3E. (A) is 10 kHz; (B) is 20 kHz; and (C) is 50 kHz.

no real increase in cost, but with greatly improved reliability. The output pulse would have defined and controlled width.

Occasions may arise when you need an oscillator having independent control of frequency and duty cycle. The 74123 (TTL) or the 74C221 (CMOS) dual monos perform this task very well using the circuit shown in Fig. 7.

If you use potentiometers for *R1* and *R2*, you can construct a low-cost, wide-



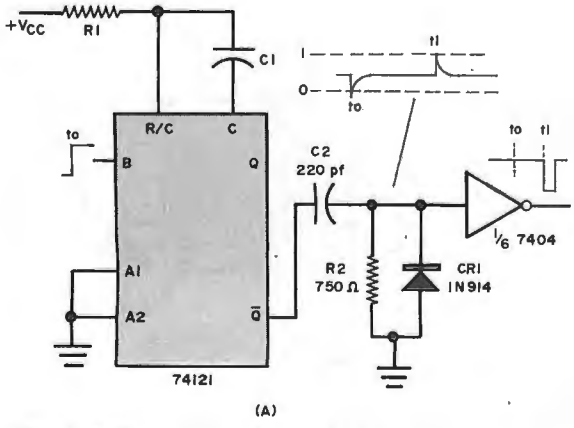


558/559 TIMER

FEATURES:
4.5-TO-16-VOLT SUPPLY RANGE. TIMING RANGE OF MICROSECONDS TO HOURS. ONE-SHOT AND ASTABLE OPERATION. EDGE TRIGGERED.

APPLICATIONS:
PRECISION TIMING
SEQUENTIAL TIMING
TIME-DELAY GENERATION
QUAD ONE-SHOT

Fig. 5. Function diagram (A) of 558/559 timer; monostable connection (B); 558 as a variable-frequency oscillator with fixed duty cycle (C); 558 open-collector output structure (D) and 559 Darlington follower output structure (E).



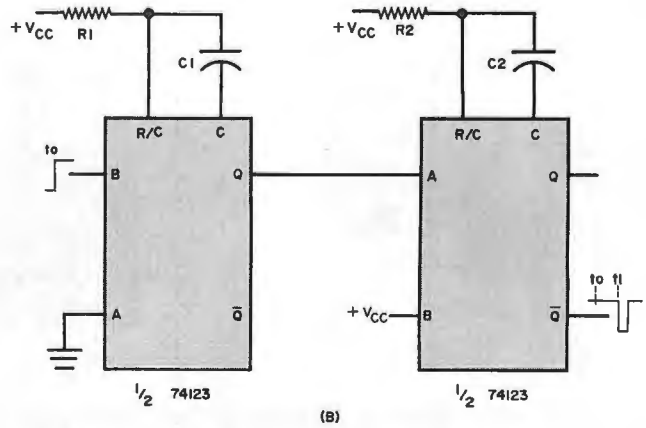


Fig. 6. RC coupling (A) used for leading edge delay for the 7404. Using a 74123 (B) provides precisely timed pulse with improved reliability.

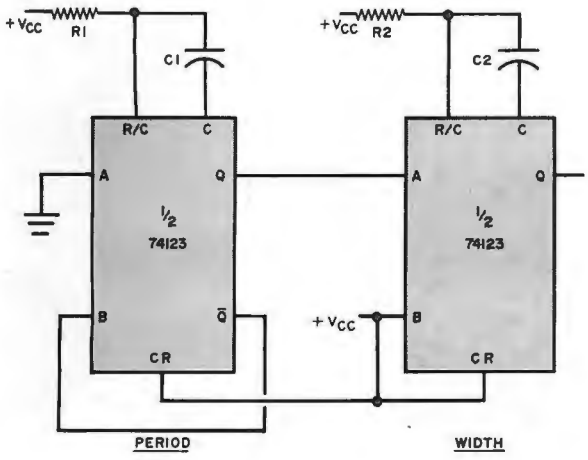


Fig. 7. A dual monostable can create an oscillator having independently adjustable period and pulse width.

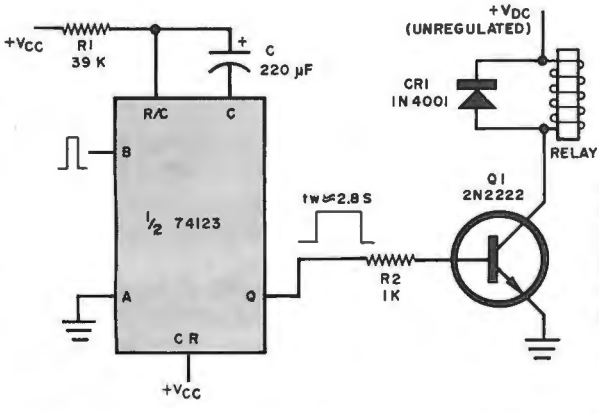


Fig. 8. A switching transistor provides relay driving power and isolates the mono from higher voltage required by the relay.

range pulse generator with lots of versatility. The capacitors may be switched to change the timing parameters.

Retriggering. This is a feature that should not be overlooked. A retriggerable mono will respond to inputs that arrive while the output is still high from the preceeding trigger. It then becomes possible to have a train of inputs that will hold the output high until the train stops.

A telephone toll restrictor was created using this effect. The problem was that there was only one signal to tell the circuit that the phone was lifted off the cradle, that the dial was being used, that dialing was completed, and that the phone was replaced on the cradle. The retriggering capability of the 74123 enabled the digits counter for the pulses from the dialer; and when the train stopped, there was a short delay, then a reset of the counter for the next digit.

Multiple Inputs. Several monos, such as the 9600,9602 and 74121 have multiple trigger inputs. These may be used as digital summing elements when you wish to form a single pulse train as a summation of triggers from several sources. Be careful here because the logic can be tricky.

Pulse Stretching. A mono can be used to stretch a brief pulse so that it can be used to drive a relay, among other applications. The basic circuit is shown in Fig. 8. The 555, 558 and 559 are well suited to this use because of their drive capabilities.

An advantage of this circuit is that the load can be powered from a higher voltage than the logic. In Fig. 8, the relay is powered from the unregulated dc supply, saving the power supply regulator. Isolating resistor *R2* is important to protect *Q1*. If heavy load current is required, the emitter of *Q1* should be returned to the power supply ground.

Summary. Because of the edge triggering features of each of the devices discussed here, many mono's can be interconnected to create complex digital waveforms that can be duplicated only with expensive commercial generators. Also, edge triggering greatly reduces the need for logic gates. ◇