DESIGNER'S NOTEBOOK

Inverting logic oscillators

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ONE OF THE NICEST THINGS ABOUT digital circuits is that you can make an oscillator out of just about anything. Just look around your design and find a few spare parts (unused gates on the board), connect them together and you've got an oscillator. While working with analog components requires some thought, digital stuff is just lying there, begging for the chance to squirt out squarewaves. But that kind of convenience tends to make you sloppy.

Because most gate-type oscillators are essentially trouble free, you can easily get into the habit of thinking that they all are—but they're not! Everybody is familiar with (and has used) the oscillator arrangement shown in Fig. 1. (We've shown it with inverters, but any type of simple inverting logic will fill the bill.)

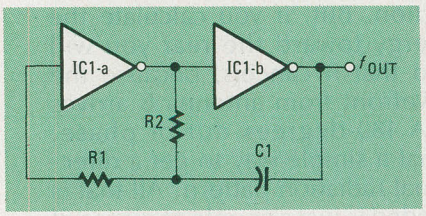

FIG. 1

Oscillator circuits

The circuit in Fig. 1 is simple to put together, forgiving of part values, and relatively stable for a given supply voltage. However, there is one problem associated with it—it won't always oscillate!

Like a good many of you, I've relied on that circuit whenever I needed a simple clock generator. More convenient ones, with fewer parts can be built with Schmitt triggers; however, not every circuit uses Schmitt triggers.

Imagine my surprise, after having figured out the component values for an oscillator I was building to get the clock frequency I wanted, and found that when I plugged the parts into the board, nothing happened. There I was, the victim of my own sloppiness.

The reason that the oscillator in Fig. 1 won't always work can be understood by taking the part values to the extremes—decreasing component values—and seeing what happens to the circuit. That kind of experimentation can come in handy when it comes to simplifying any circuit.

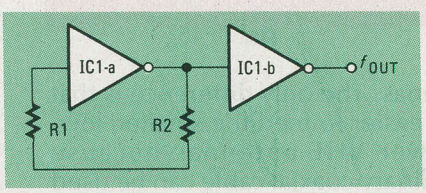

FIG. 2

If we keep on reducing the value of capacitor C1 and let it go to zero, we're going to wind up with the circuit shown in Fig. 2. There we see that IC1-b is no longer a part of the circuit, and it doesn't take much analysis to see that the circuit won't oscillate. What that tells us is that there are limits to the allowable value of the capacitor.

What those limits are will depend on several things; the supply voltage, load, component values, and a whole bunch of other stuff. In other words, what had been a really handy, no-thought type of circuit has turned into one that requires some consideration before we can use it.

The problem here is that the schematic in Fig. 1 is not an inherently astable circuit. That can been seen by looking at Fig. 2 and comparing it to Fig. 1. Remember, the capacitor forces the circuit to oscillate and if it's value is not large enough (or there is none at all), the circuit will just sit there and do absolutely nothing.

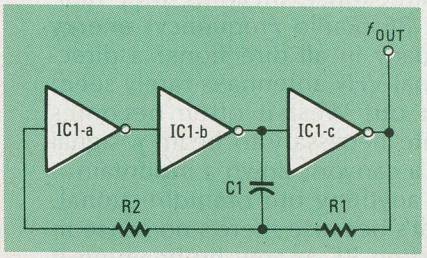

FIG. 3

What we need is a trouble-free oscillator that is inherently astable. Figure 3 is the type of circuit that we're looking for. As stated before, you can do a lot better and greatly simplify things by using Schmitt triggers. For all those other times, however, the circuit shown in Fig. 3 is just what the doctor ordered.

The circuit is sure-starting and trouble-free—it will oscillate over a much wider range than an oscillator made with just two inverters (like the one in Fig. 1). The formula for determining the output frequency is admittedly a bit complex, but several assumptions can greatly simplify things. Since it's not the kind of circuit that you would use if you need good stability or heavy-duty precision, the following approximations are more than adequate:

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- If R1 is close to R2, then $f = .56/RC$, where R is the average of R1 and R2.
- If R1 is much larger than R2, then $f = .46/R1C$.
- If R1 is much smaller than R2, then $f = .722/R1C$.

The output will be a squarewave with a duty-cycle that's pretty close to 50/50. That only happens with CMOS inverters because the switching point is the threshold of the inverters and (for CMOS) that's halfway up the supply rail. That switching characteristic also makes the circuit almost immune to power-supply spikes and other nasties.

The output frequency of the circuit is a function of the propagation delay through the gates. That means that the output stability will degrade as the frequency increases. The propagation delay is a constant and the lower the frequency, the smaller it (the delay) will be relative to each output pulse. **R-E**