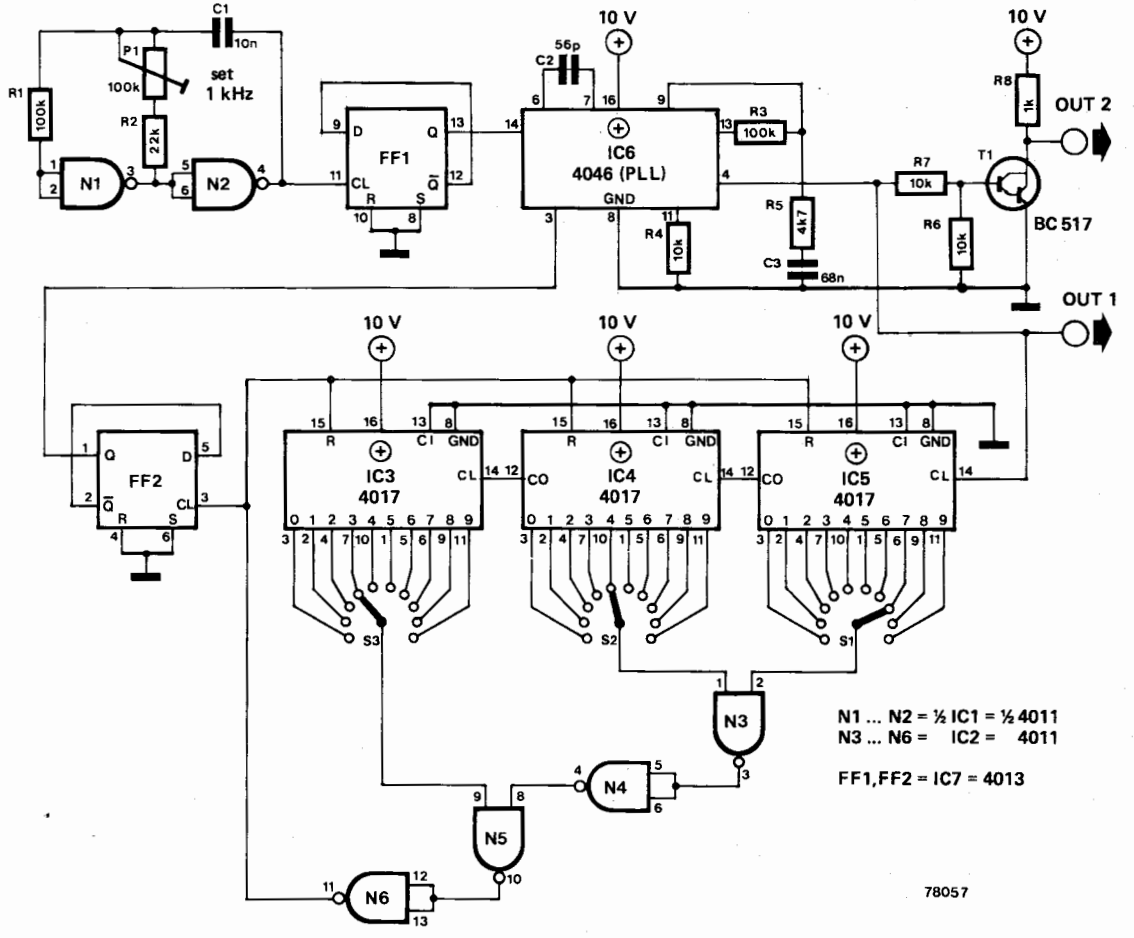
frequency synthesiser 103



The output frequency of this squarewave generator can be programmed in 1 kHz steps from 1 kHz to 999 kHz. The heart of the circuit is a 4046 CMOS phase-locked loop which has an extremely wide capture range.

The output of a 1 kHz clock generator, N1/N2, is divided down by FF1 to give a symmetrical 500 Hz squarewave output, which is fed to one of the phase comparator inputs of the 4046 (IC6). The Voltage Controlled Oscillator (VCO) output of IC6 is fed to the second input of the phase comparator via a programmable frequency divider (IC3-IC5) and FF2.

The VCO output frequency of the PLL adjusts itself until the output of FF2 has the same frequency and phase as the clock output from FF1. If the division ration set on switches S1 to S3 is n then the VCO frequency must obviously be n times the 1 kHz clock frequency. Setting a number n on switches S1 to S3 therefore gives an output frequency of n kHz. The VCO output from pin 4 may be used to drive CMOS circuits direct, however, for other applications a transistor buffer may be required.

If greater frequency accuracy is required then the clock oscillator may be replaced by a more stable 1 kHz reference frequency such as the divide-by-10^3 output of the IC counter timebase described elsewhere in this issue.