10-kHz VFC uses charge-pump variation

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A diode-capacitor charge pump is the starting point for many voltage-to-frequency-converter (VFC) designs. The circuit in **Figure 1** uses a variation on that classic theme to achieve linearity less than 0.05%, micropower operation of approximately 10-μA total draw from a 5 to 36V rail, and bipolar-input capability. The basis for these features is the switchable-polarity, self-compensating charge pump comprising D_1 to D_4, C_1 to C_4, and CMOS switches S_2 and S_3. Although simple in concept, VFCs using diode-capacitor pumps suffer from the need to cope with the nonideal characteristics of diodes used as analog switches.

Temperature-dependent forward-voltage drop, junction and stray capacitance, and reverse leakage current all conspire to limit converter accuracy. The stray capacitance and leakage current are especially troublesome in low-power applications, in which the need to minimize pump-current consumption limits the size of the pump capacitors. Because the total amount of charge pumped in each converter cycle is minimal, the error sources are proportionally more significant and thus harder to control and compensate. The unique pump circuit in this converter comprises two distinct halves: D_1, D_2, C_1, and C_2 generate a frequency-proportional current that closes the VFC's feedback loop, and D_3, D_4, C_3, and C_4 generate an error-correcting compensation current.

If you assume that $C_2=C_2=C_3=C_4$ and equality of diode forward drops (V_D) and stray capacitance (C_S), then the net feedback current from the pump is

$$f_{OUT}(2C_1+C_S)\left[4.55V\times\frac{2C_1}{2C_1+C_S}-2V_D-(4.55V\times\frac{C_1}{2C_1+C_S}-2V_D)\right]$$

$$=f_{OUT}(2C_1+C_S)\left[4.55V\times\frac{2C_1-C_1}{2C_1+C_S}+2V_D-2V_D\right]$$

$$=f_{OUT}\times4.55\times C_1=f_{OUT}\times10^{-4}\,\mu A/Hz.$$

You not only obtain compensation for the bothersome V_Ds, but also eliminate the effects of stray capacitance in the bargain. Operation of the converter depends on integrator IC_1's control of multivibrator IC_3. The combination is such that $f_{OUT}=0$ when IC_1's output is 1.2V. If, for example, $V_{IN}>0V$, IC_1 ramps negative. As IC_1 ramps through approximately 0.8V, Q_1 begins to conduct, thereby turning on both Q_2 and Q_3. Q_2 drives S_1 to the "plus" polarity state, providing a status signal to the connected system (typically, a gated up/down counter). The status signal indicates the presence of a positive V_{IN}. S_1 sets up S_2 and S_3 to provide a negative feedback current to C_5. Subsequently, Q_3's collector current causes IC_3's f_{OUT} to increase until $1E{-}7\times f_{OUT}=V_{IN}/R_1=4$ kHz/V

for the values shown, and the integrator is thus balanced.

V_{IN}<0V causes IC_1 to ramp positive, turning off the Q_1-Q_2-Q_3 transistor trio. This action causes S_1 to generate a "minus" status and set up S_2 and S_3 to generate a positive feedback current. The loop adjusts f_{OUT} until $1E{-}7{=}{-}V_{IN}/R_1$, as in the case of V_{IN}>0V. The converter's overall temperature coefficient depends on matching all pump capacitances, including the pc-board contribution to C_S parasitics. A ±5% capacitance tolerance is good enough to reduce the charge-pump temperature coefficient to approximately 50 ppm/°C. The converter linearity is ±0.03%, and the current draw is an unexcelled 6.5 to 10 µA as f_{OUT} goes from 0 to 10 kHz. IC_1's approximately 300-µV input-offset spec determines the converter's zero offset. IC_2's regulation of the 4.55V reference affords good power-supply rejection, yielding undiminished accuracy for supply voltages from 5 to 36V. (DI #2183) EDN

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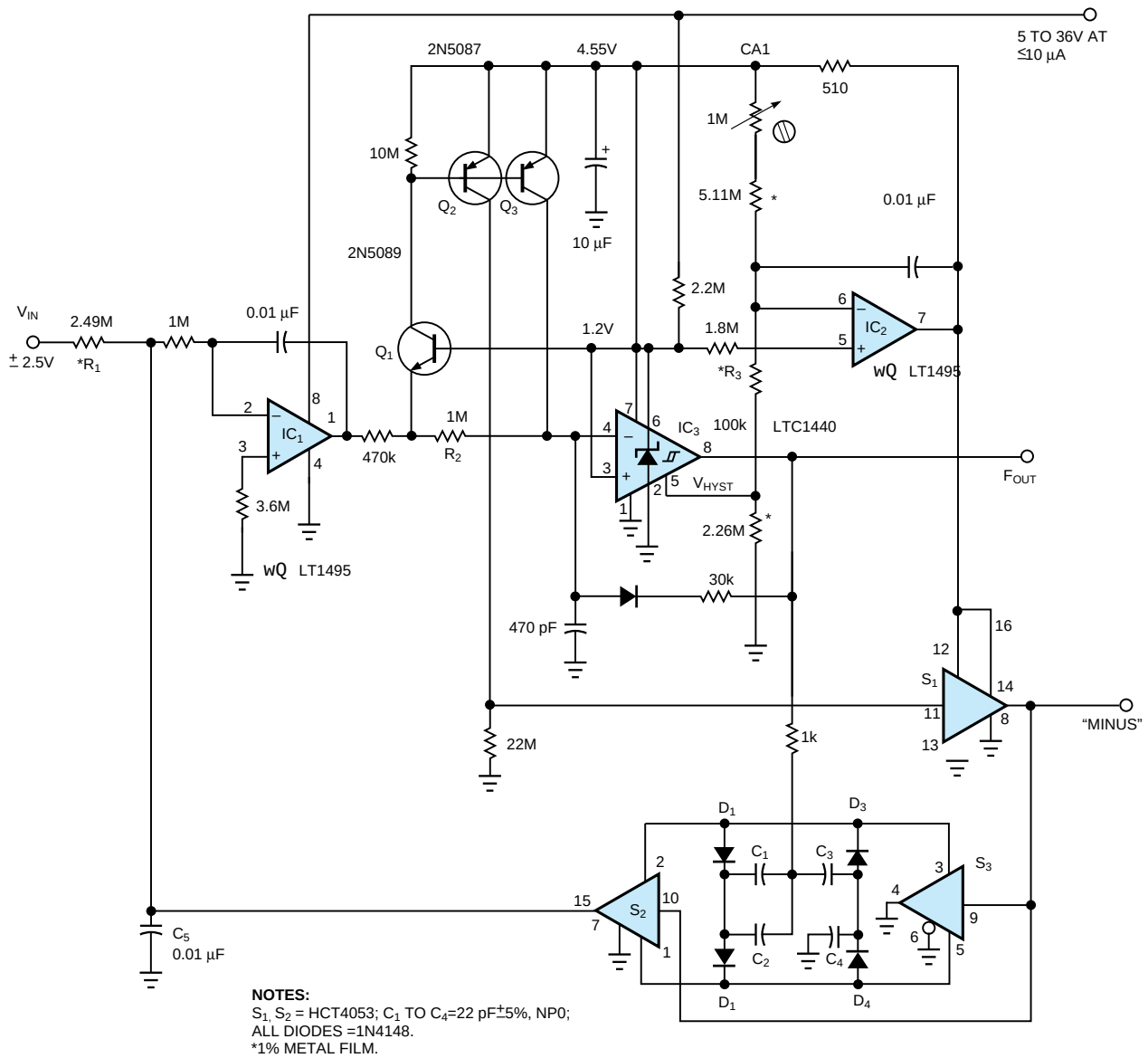
FIGURE 1



A fleapower bipolar-input VFC uses a modified charge-pump technique to achieve high linearity with power supplies ranging from 5 to 36V.