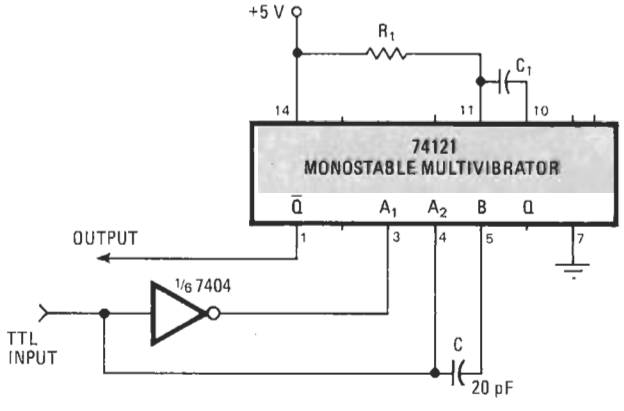
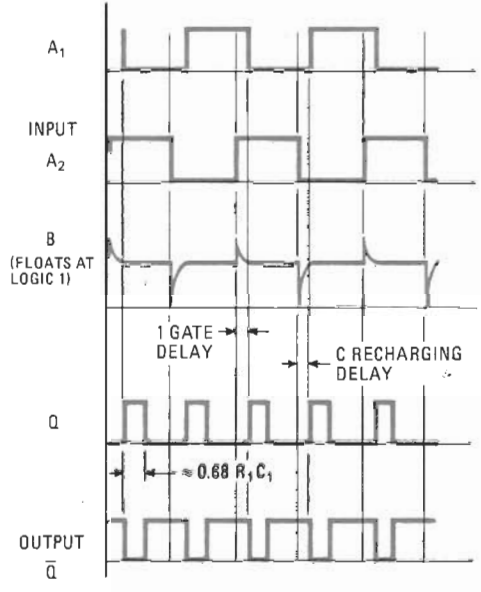
Frequency-doubler produces square-wave output

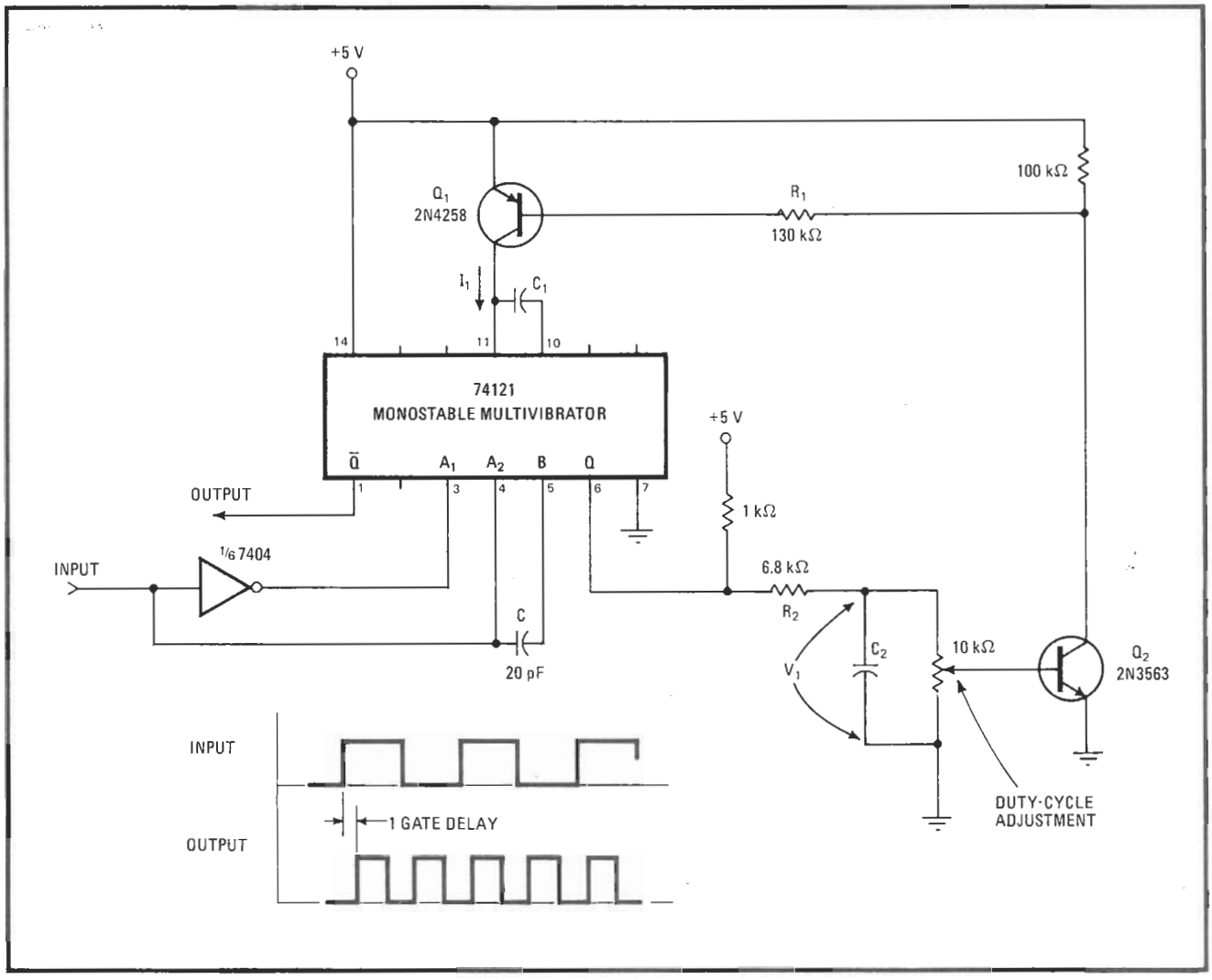
by Robert L. Taylor
I&F Electronics, Nashville Tenn.

Most digital frequency-doublers use edge-detection techniques to produce two narrow output pulses per input pulse. Although these types of doublers work well, they have the disadvantage of producing highly asymmetrical outputs and usually cannot be cascaded to ob-



1. Basic frequency-doubler. The monostable multivibrator produces two output pulses for each cycle of input waveform. One output pulse is triggered on falling edge of A_1, and second output pulse is triggered when B goes high after spiking low. If output pulse width is set for 50% duty cycle at one frequency, it is asymmetrical at other frequencies. The time delays are shown disproportionately large.





2. Constant duty cycle. Addition of feedback loop to circuit of Fig. 1 makes duty cycle of output wave independent of input frequency. Triggering of output pulses is the same as in the basic circuit, but the pulse width is automatically adjusted for the duty cycle set by the potentiometer. Here the pot setting gives a square wave at the doubled frequency. Delays of 30 or 40 ns are negligible at frequencies below 1 MHz.

tain higher multiplication factors. These problems can be eliminated by use of a monostable frequency-doubler with a modified version of H.P.D. Lanyon's feedback system [see "One-shot with feedback loop maintains constant duty cycle," *Electronics*, July 24, 1975, p. 93].

The basic doubler circuit and its timing diagram are illustrated in Fig. 1. The propagation delay introduced by the inverter allows the 74121 monostable multivibrator to trigger on the rising edge of the input wave, and the 20-picofarad capacitor triggers on the falling edge. Since both edges of the input are detected, the output frequency is twice the input frequency. By selecting the proper R_1C_1 value, a 50% duty cycle could be obtained with the circuit of Fig. 1, but only for one fixed input frequency.

In the improved circuit arrangement shown in Fig. 2, the output pulses from Q are filtered by R_2C_2 to produce a voltage V_1 that is directly proportional to the input frequency. A portion of V_1, tapped off the 10-kilohm potentiometer, is amplified and inverted in transistor Q_2. The amplified voltage is applied through R_1 to transistor Q_1, which serves as a controlled current source that feeds the timing circuit of the 74121. The value of R_1 is chosen to limit I_1 to a maximum of 5 milliamperes.

In operation, the 10-kΩ symmetry potentiometer is adjusted for a 50% duty cycle output. If the input frequency increases, V_1 increases proportionally and causes Q_2 to conduct more. This draws more base current from Q_1 and causes its collector current to rise. An increase in I_1 produces a corresponding decrease of output pulse width, tending to lower V_1. The high gain of this negative feedback loop keeps the output duty cycle very near 50% over about a 1,000:1 frequency range. Best results occur when the maximum frequency f_{max} is less than $1/(800\ C_1)$, where C_1 is in farads and f is in hertz. The size of capacitor C_2 is chosen to provide good filtering action for V_1 at the lowest frequency used—that is, C_2 is greater than $1/(1{,}000\ f_{min})$. Other parts values and transistor types are not critical. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.

Pulse-frequency doubler requires no adjustment

by Thomas McGahee
Don Bosco Technical High School, Boston, Mass.

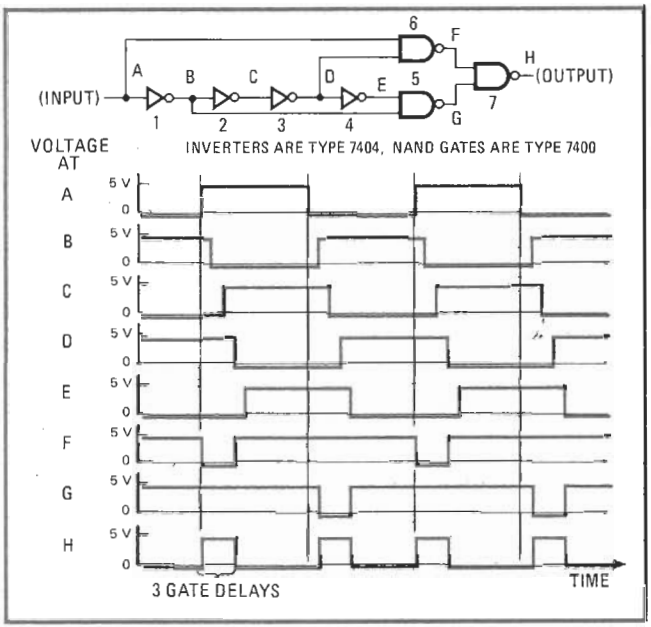
Sometimes a frequency doubler is needed in a digital system, and unfortunately most doubler circuits have to be adjusted for a particular operating frequency. However, this circuit, which has operated successfully in a specially designed divide-by-N counter, requires no adjustment over a range from near dc to 10 megahertz.

When a signal pulse passes through the circuit, each inverter introduces a small delay, typically of 20 nanoseconds, in addition to inverting the pulse. For example, the signal at point D inverts 60 ns after the input signal at point A has inverted; thus, gate 6 continues to have high signals at both of its input terminals for 60 ns after the input at point A changes from low to high. As a result, the output from gate 6 (i.e., point F) will go low for 60 ns after a positive-going transition at the input to the circuit.

Somewhat the same thing occurs at gate 5, except that it develops a 60-ns low output after a negative-going transition at the input. In the circuit diagram, inverters 1, 2, and 3 all serve double duty in producing these 60-ns low pulses at points F and G. This design reduces the number of gates needed.

The pulses from gates 5 and 6 are fed to the terminals of gate 7, which produces a positive pulse 60 ns wide every time either one of its input terminals goes low. Since one terminal goes low on the leading edge of each input pulse at point A, and the other terminal goes low on the trailing edge of each input pulse at A, the frequency of the output pulses at point H is twice the frequency of the input pulses at point A.

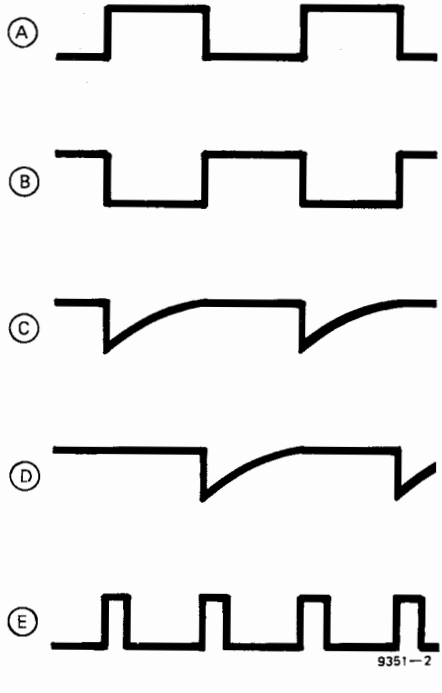
The output is in the form of positive pulses that are 60 ns wide. There is a 20-ns difference in the spacing between successive output pulses because the portion of the circuit that comprises the negative-going edge-detector has one more inverter stage than the positive-going edge-detector section does. This slight asymmetry is noticeable only at the highest frequencies. If particularly slow input signals are used, it is a good idea to place a Schmitt trigger just before the input. □



Frequency doubler. Propagation delays through inverters cause NAND gates 5 and 6 to go low for 60 nanoseconds following the rising and falling edges, respectively, of input pulse. Therefore output goes high twice as often as input.

positive-going pulse appears on the output of N3, (waveform E). The output of N4 is an inverted version of (E). The switching threshold of CMOS logic is about 45% of supply voltage, so the switching point of N3 on the rising exponential portions of waveforms (C) and (D) will occur at this point. The time taken for the waveform to rise to this voltage is just less than the time constant RC, so the pulse duration of waveform (E) is approximately equal to the time constants R1C1 and R2C2. For reliable operation these time constants should be chosen to be much less than the shortest possible period of the input waveform. The reason for this is that the width of the positive-going pulses (E) is constant, but the length of the spaces between them diminishes as the input frequency increases. If the pulses are not of short enough duration they may overlap at high input frequencies.

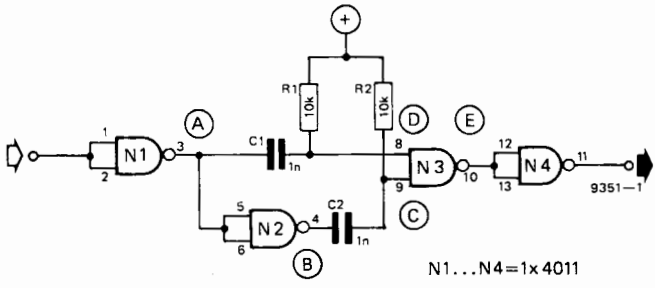
2



17 This frequency doubler uses one CMOS quad, two-input NAND gate package type 4011. The frequency doubler proper consists of an inverter N2, two differentiating networks R1/C1, R2/C2 and NAND gate N3. N1 and N4 function as input and output buffers.

The incoming signal is buffered and inverted by N1, giving waveform (A) (it is assumed the waveform has 1:1 mark-space ratio). (A) is inverted by N2, giving waveform B, which is the complement of (A) (i.e. it is in antiphase). The negative-going edges of waveform (B) are differentiated by R2 and C2, giving waveform (C), while (A) is differentiated by R1 and C1, giving waveform (D). Waveforms (C) and (D) are fed into N3, and every time one of these waveforms is negative-going a

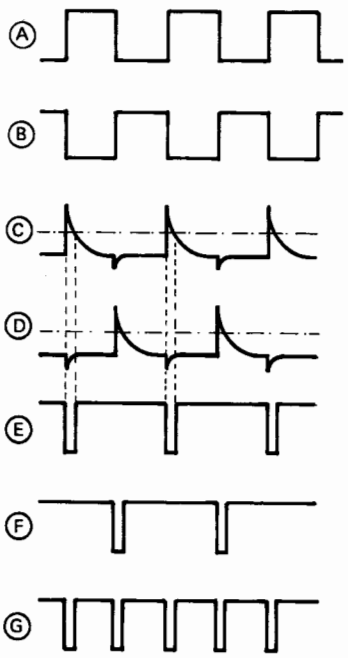
1

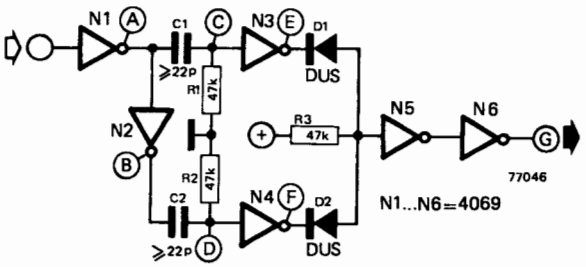


41

frequency doubler using 4069

A.M. Bosschaert





Using a single 4069 hex inverter IC, a frequency doubler can be constructed to give an output pulse train whose frequency is twice that of a squarewave input signal.

The signal is applied to the input of N1. It should be a squarewave with a duty-cycle of approximately 50% at a level compatible with CMOS logic (3 – 15 V peak-to-peak depending on supply voltage). The input signal is buffered and inverted by N1, and inverted again by N2, so the outputs (A and B) of N1 and N2 are squarewave signals 180° out-of-phase. The output of N1 is differentiated by C1 and R1 and the output of N2 is differentiated by C2 and R2, giving two spike waveforms (C and D) 180° out-of-phase. These signals are buffered, inverted and 'squared up' by N3 and N4 to give waveforms E and F. These are then combined in a NOR gate consisting of D1, D2, R3 and N5, and finally inverted by N6 to give the output waveform G, which has a frequency twice that of the input signal.

The circuit will operate over a wide frequency range. The upper frequency restriction is imposed by the fact that the width of the negative-going pulses E and F must be greater than the minimum pulse width that N3 and N4 will reliably transmit. Assuming that waveforms E and F have the minimum possible pulse width, as the frequency of the input signal increases the duty-cycle of the output signal will approach 50% as the pulses come closer together. When this situation is reached then the width of the positive output pulses is also the minimum that the 4069 will handle.

With the component values shown the width of pulses E and F is about 500 ns, so the duty-cycle of the output will be 50% when the frequency is 1 MHz, i.e. when the input frequency is 500 kHz.

DESIGNER'S NOTEBOOK

Frequency multiplication

ROBERT GROSSBLATT

ONE OF THE BIGGEST ADVANTAGES THAT A digital approach to circuit problems has over more traditional analog solutions can be summed up in one word—precision. In fact, some of the stickiest problems that come up when dealing with analog circuitry have been just about eliminated, now that a handful of silicon shavings can replace acres of glass epoxy and miles of wiring.

Certainly the area where that has become most outrageously evident is in the whole field of frequency generation and division. At one time, super-precise frequencies could only be generated by using crystal oscillators, expensive hand-picked components, and then building elaborate divide-by networks with components that had names like 12AX7, 6AU6, and so on.

Of course, we're talking about techniques most commonly used by monks and we know about them through ancient hand-illuminated parchment scrolls. Seriously though, the whole idea of frequency-synthesis and division has undergone a major change with the development of the IC.

One of the first experiments that any newcomer to design encounters is building a simple circuit that can generate several frequencies by dividing down a master oscillator. Not only that, but the whole design can be accomplished using less than three IC's! And if you use a binary ripple-counter, like the 4060, you don't even need an external oscillator—it's built right onto the substrate and can be either an R-C type or crystal based. But enough beating around the bush.

The point here is that while everyone knows twelve-million ways to easily divide any frequency by any number, it's sometimes necessary to do exactly the the opposite. Multiplying a frequency with the same degree of precision that we can get with division is possible by using things like rate multipliers and some exotic special-purpose IC's. And if you have to multiply a frequency by some "odd-ball" number, special-purpose IC's are the way to go. But suppose your needs are really simple. Just as you can easily divide by two using nothing more exotic than a flip-flop, this month's handy-dandy circuit will multiply a frequency by two just as easily. You can take the same ideas even farther and multiply by four, eight, or whatever, by cascading.

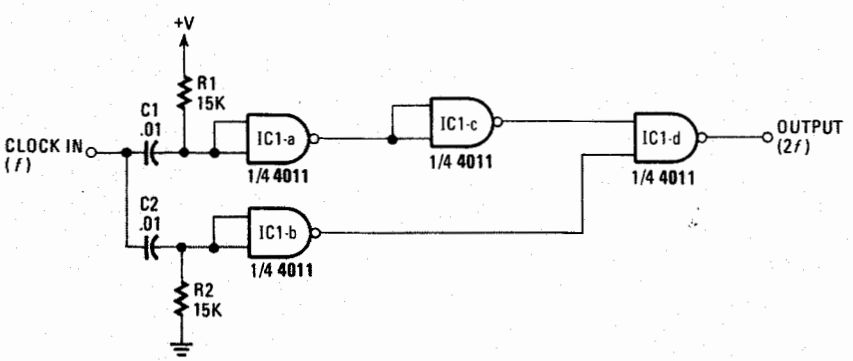


FIG. 1

How it works

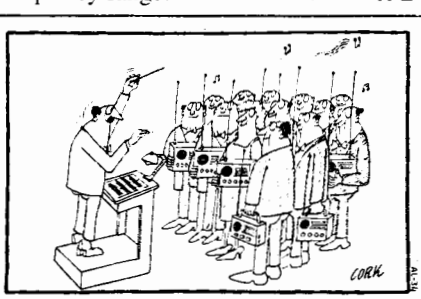
Figure 1 shows a circuit that can be used as a frequency multiplier. The operation of the circuit is so simple it doesn't require much of an explanation. The whole thing is made from a single quad two-input NAND gate! Two gates, IC1-a and IC1-b, are set up as inverters and their inputs are isolated from each other by two capacitors, C1 and C2. Resistors R1 and R2 hold the inverter inputs high and low respectively. Since IC1-c is on the line between IC1-a and IC1-d, both inputs to IC1-d will be high. As long as there's no signal at the clock input, the output of IC1-d is low.

When a clock pulse shows up at the input, the negative edge will charge capacitor C1 and thus change the output state of IC1-a. The output of that IC is then again inverted by IC1-c. As a result, a low is applied to one leg of IC1-d, causing it to output a high. All the IC's will stay in their present state until either the R-C network times-out or the input clock goes high.

When the input clock goes high, capacitor C2 will charge-up and force IC1-b to output a low on the other leg of IC1-d, forcing its output to go low again. The cycle will repeat over and over again, resulting in an output frequency that is exactly double that of the input clock. Just about the only thing to be careful of is to make sure that the R-C time-constant is well above the maximum frequency that you expect to put through the circuit. If the input frequency has a period that is shorter than the time constant of the R-C network, the circuit will hang up.

With the component values shown, you should be OK, provided that you don't apply a frequency to the input that is greater than 500 kHz. Also, be certain that the IC that you are using can handle double the input frequency, since IC1-d will be switching at twice the input frequency. It should also be noted, at this point, that the IC used in the circuit should be compatible with the circuitry that it is to feed. For example, if you are using 7400 series TTL's, use a TTL NAND gate such as the 7402; and as for circuits that contain CMOS or low-power Schottky devices, use a CMOS IC such as a 4011 or 74LS00 series TTL respectively.

You should be able to use the same technique to build circuits that will triple or even quadruple an input frequency. All that you need is more inverters and a final gate with the right number of inputs. There are other, even simpler methods to do the same thing. But the operation of this circuit is very reliable over a wide frequency range. **R-E**



tech-tips SPECIAL

FREQUENCY DOUBLER

This is a simple three transistor circuit to raise an audio frequency by a factor of two i.e., one octave. Q1 is connected as a phase splitter with anti-phase signals appearing at it's collector and emitter. These signals are fed to two emitter followers Q2 and Q3, which have a common emitter resistor, and thus add the two anti-phase signals. A degree of distortion is inevitable as shown in Fig. 2, but is acceptable for speech and soloists and produces a sound similar to the Chipmunks or Pinky and Perky.

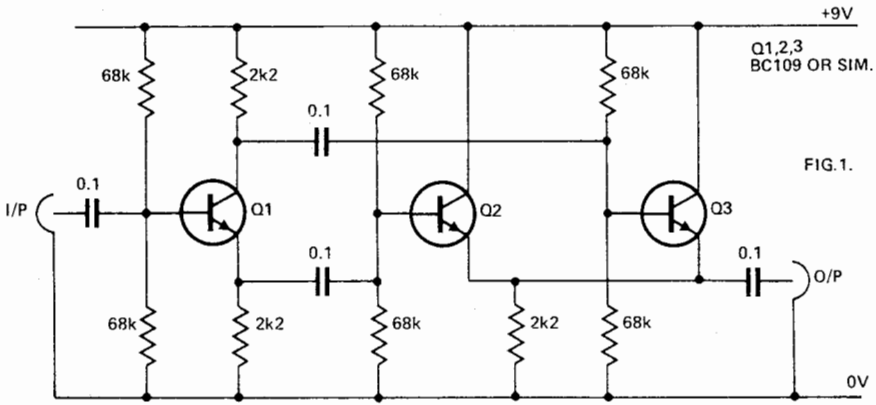
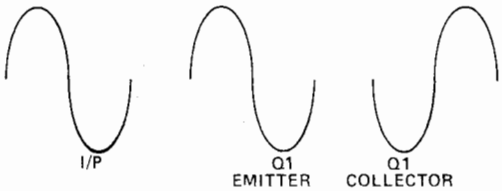


FIG.1.



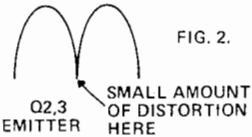


FIG. 2.