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Astable multivibrator gets hysteresis from positive-feedback stage

Robert Larson, Seattle, WA

Many designs exist for logic-based astable multivibrators, one of the simplest being an RC feedback loop around a single inverting Schmitt trigger inverter (**Figure 1**). The output charges the capacitor to the upper switching threshold, at which point the output switches to its opposite state, the threshold switches to a different value, and the capacitor's charging current reverses direction. When the capacitor's voltage crosses the lower threshold, the output and threshold both toggle back to their original values, and the process repeats. The timing depends on both the RC time constant and the hysteresis resulting from the spread between the two threshold values (**Figure 2**). Unfortunately, although inverter manufacturers specify the hysteresis voltages in their data sheets, the devices have a fairly large range. In addition, they likely have some temperature dependence. These uncertainties make it difficult to design the circuit to have a predictable oscillating frequency.

A simple inverter, without the hysteresis to let it overshoot the nominal threshold, charges the capacitor to the threshold voltage and stops in its narrow linear region. At this point, the negative feedback from the inverting output to the input regulates the output to the threshold voltage. Adding another inverting stage injects hysteresis of a different form by means of positive feedback, which external passive

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TABLE 1 74VHC04 RESULTS

Resistance (kΩ)	Timing capacitance (pF)	Hysteresis capacitance (pF)	Expected results: Hysteresis voltage (V)	Expected results: Total time period (nsec)	Measured results: Hysteresis voltage (V)	Measured results: Total time period (nsec)	Total time differential (%)
10	470	100	0.88	3462	0.75	2930	18
10	470	220	1.59	6850	1.8	7340	−7
10	12,000	12,000	2.5	333,526	2.6	364,800	−9
0.3	220	220	2.5	221	1.75	240	−8
1	12,000	12,000	2.5	34,086	2.5	36,000	−5

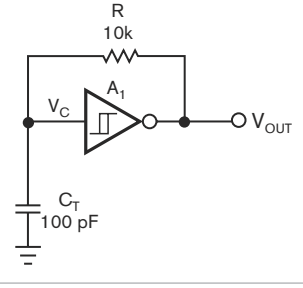

Figure 1 A basic astable multivibrator uses a Schmitt trigger and an RC network.

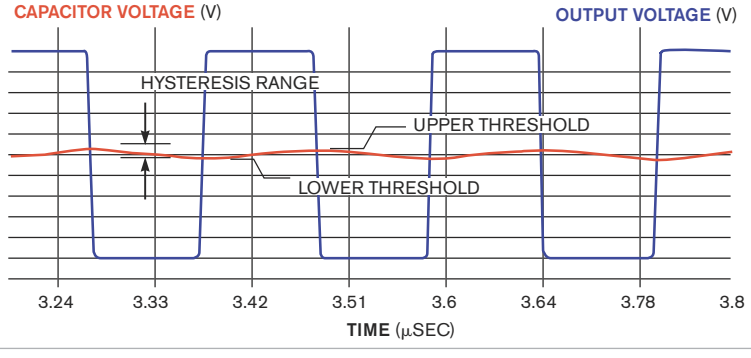

Figure 2 A part's hysteresis, in large part, determines switching thresholds.

parts determine (**Figure 3**).

Whenever Stage 1 crosses its threshold, the extra Stage 2 injects an additional charge through a feedback capacitor to make the timing capacitor's voltage jump past the threshold. The RC charging current reverses direction to get back to the threshold voltage. When it gets there, the hysteresis-injection circuit again jumps the voltage past the target so that the RC timing circuit must again reverse the charging current to seek the threshold voltage (**Figure 4**). This process continues endlessly at a fairly predictable rate. In the **equations**, C_T is the timing capacitor, C_H is the hysteresis capacitor, V_{THRESH} is the threshold voltage, V_{LOW} is the low output voltage, and V_{HIGH} is the high output voltage.

You can view the hysteresis-overshoot voltage, V_{HYST}, as the result of a capacitive voltage divider that timing capacitor C_T and hysteresis capacitor C_H form. When Stage 1 toggles Stage 2, its output jumps from a low value to a high value or from a high value to a low value by an amount of $V_{HIGH}-V_{LOW}$, and the voltage of the timing capacitor jumps by $V_{HYST}=(V_{HIGH}-V_{LOW})(C_H/(C_H+C_T))$. Second, the voltage of the timing capacitor relaxes back toward Stage 1's output voltage by drawing current through both the timing capacitor and the hysteresis capacitor.

Thus, the relaxation time constant is $R(C_T+C_H)$ and the relaxation voltage is either $V_{CT}=(V_{THRESH}+V_{HYST}-V_{LOW})\exp(-t/R(C_T+C_H))$ or $V_{CT}=(V_{HIGH}-(V_{THRESH}-V_{HYST}))\exp(-t/R(C_T+C_H))$, depending on which half-cycle is occurring. You calculate the time from $V_{THRESH}+V_{HYST}$ back to V_{THRESH} as $t_1=-R(C_T+C_H)\ln((V_{THRESH}-V_{LOW})/(V_{THRESH}+V_{HYST}-V_{LOW}))$. For the other half-cycle, $t_2=-R(C_T+C_H)\ln((V_{HIGH}-V_{THRESH})/(V_{HIGH}-V_{THRESH}+V_{HYST}))$.

You should add the total propagation time ($t_{PLH}+t_{PHL}$) through stages 1 and 2 to the total period. Unless you want the circuit to operate at its maximum frequency, these propagation times become insignificant. The period prediction then depends only on passive-component values and their tolerances, temperature, and aging coefficients. The series combination of C_T and C_H, however, presents a capacitive load to Stage 2. This load affects Stage 2's rise and fall times, the sum of which you must add to the total period, T.

In the case of CMOS parts, such as the 74VHC04 from Fairchild Semiconductor (www.fairchildsemi.com), rise and fall times depend on the output resistance of the part as well as on the external components. If you model the Stage 2 output as an RC circuit, you can estimate the 10 to 90% exponential rise and fall times as $t_{RISE2}=t_{FALL2}=2.2R_O(C_TC_H/(C_T+C_H))+t_O$, where t_{RISE2} is the rise time, t_{FALL2} is the fall time, R_O is the output resistance of the part—30Ω for the 74VHC04—and t_O is the no-load rise time—in this case, 4.5 nsec for the VHC04. Thus, the total period is $t_1+t_2+2(t_{PLH}+t_{PHL})+t_{RISE2}+t_{FALL2}$.

Also note that the timing depends on inverter output voltages and the location of the threshold voltage within that range. For example, a CMOS part whose outputs are close to the power rails is more predictable than a TTL (transistor-transistor-logic) part, and a 74HC part with a midpoint threshold voltage has a more symmetric output than an HCT part whose threshold voltage is offset for TTL interfacing.

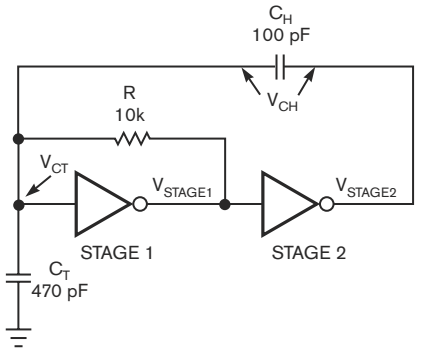

Figure 3 The addition of a positive-feedback stage provides hysteresis to a simple inverter stage.

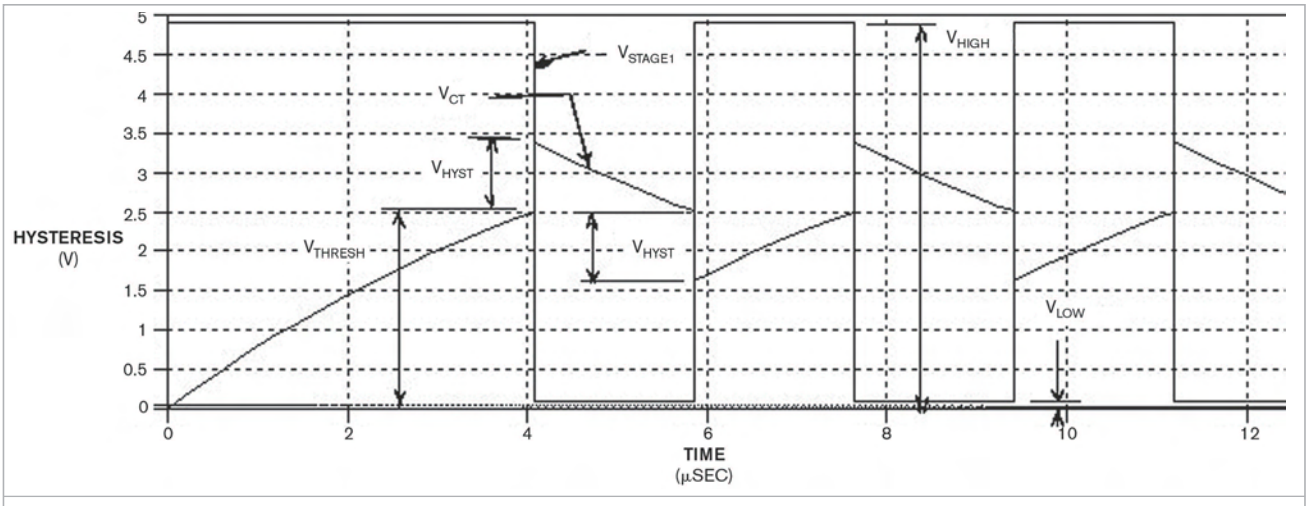

Figure 4 Hysteresis results from a charge burst from Stage 2 that jumps the timing-capacitor voltage past the switching threshold by a known, fixed amount.

For higher frequencies, you must use smaller resistor values, smaller timing-capacitor values, or both. For predictable results, the value of the timing capacitor should be no less than 10 times the inverter's input capacitance, which ranges from 3 to 10 pF for a typical CMOS, and R should not be so low that it significantly loads down the output. As a precaution, the value of the hysteresis capacitor should not exceed that of the timing capacitor so that it does not exceed the maximum input voltage on Stage 1. If the value of the hysteresis capacitor were much greater than that of the timing capacitor, then the threshold voltage and the hysteresis voltage would approach 7.5 and −2.5V, respectively. The 74VHC04 part proves the calculations using 5% resistors and 20% capacitors.

Table 1 summarizes the results, which are within the component tolerances. **Figure 5** shows a typical input and output plot.EDN

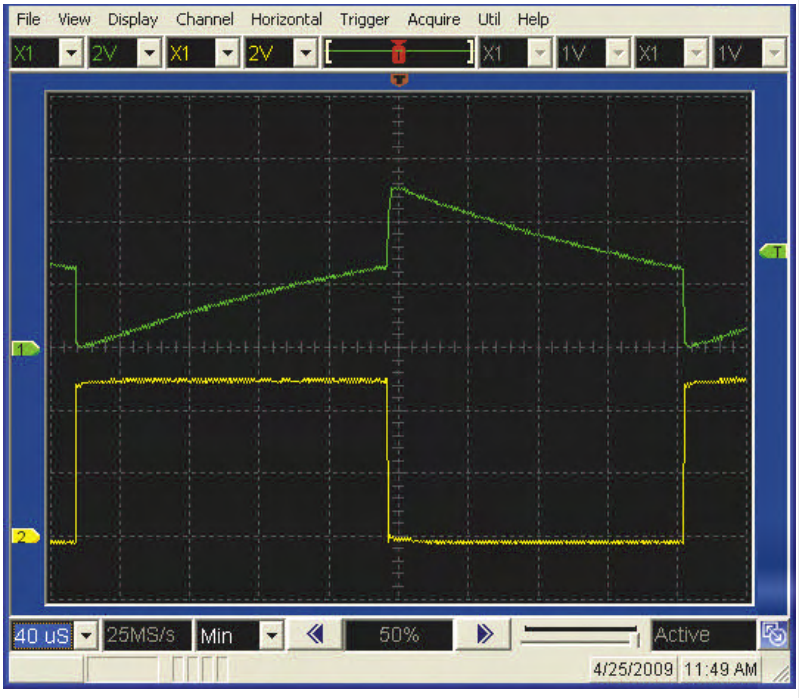

Figure 5 The circuit is well-behaved at low frequencies.

Class B amplifier has automatic bias

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Class B amplifiers are prone to crossover distortion, which occurs in the output stage in which conduction transfers from one transistor to the other. To prevent crossover distortion, a bias current must flow in both transistors simultaneously. The bias current prevents both transistors from turning off in the transition region. Classic bias circuits keep a constant dc polarization voltage between the bases of the two transistors. Often manually adjusted, it keeps the two transistors on the edge of conduction when there is no signal present. Such a circuit is sensitive to temperature and needs some form of compensation to prevent thermal runaway, which can lead to failure. **Figure 1** shows an approach in which automatic bias eliminates the problem.

In this Class B amplifier, R_1 sets the bias current at idle mode with no signal. Emitter current for Q_3 is $(V_{CC}-V_{BIAS}-V_{BEQ3}-V_{BEQ1})/R_1$, where V_{CC} is the power-supply voltage, V_{BIAS} is the dc voltage on the emitters of Q_1 and Q_2, V_{BEQ3} is the base-to-emitter voltage of Q_3, and V_{BEQ1} is the base-to-emitter voltage of Q_1. Q_1 and Q_2 mirror this current because Q_1 and Q_3 share the same base current, as do Q_2 and Q_4. Assuming that the four transistors are perfectly matched, all of them have the same base current and the same collec-

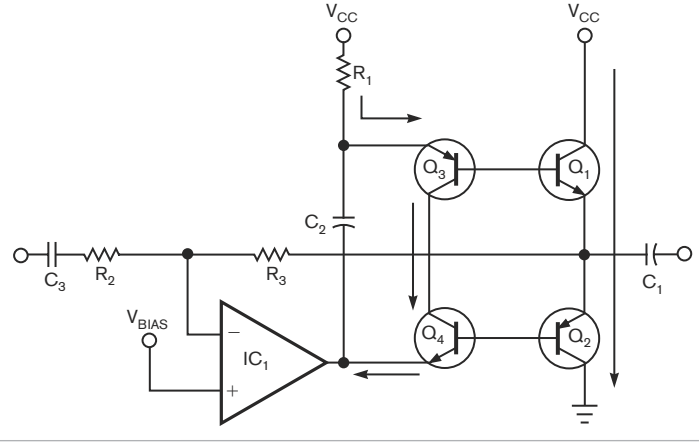

Figure 1 A bias current flows in the transistors that prevents Q_1 and Q_2 from being off simultaneously.