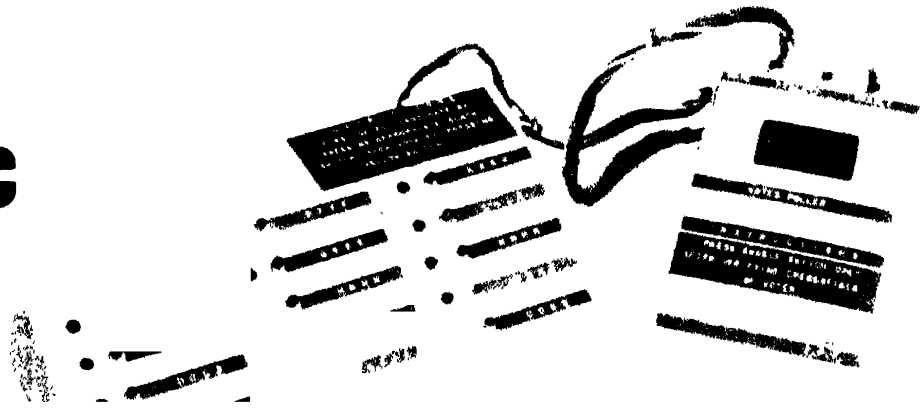
Electronic Voting Machine



Part II

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Last month we discussed the modules of the main board. This month we shall see the working of the other boards.

The memory board

The circuit uses 16×4-bit RAMs for recording the results. The ICs can register 4-bit words at 16 different locations. A number of these ICs can be cascaded as shown to give any desired maximum vote count.

IC14 registers the least significant digit whereas IC20 registers the most significant digit. The memory is addressed through pins 1,13,14 and 15. On receiving a low pulse at pin 3, the memory registers the data placed at pins 4,6,10 and 12 which, after an inversion, are available at pins 5,7,9 and 11.

IC16 is a counter that can be pre-set. If parallel load pin 11 is held low, data at pins 1,9,10 and 15 is loaded into the counters and is made available at pins 2,6,7 and 3.

The counter is incremented on receipt of clock pulses at pin 5. To facilitate cascading of the counters, a terminal count output is available at pin 12 which serves as a clock for the next counter. The BCD count is available at pins 3,2,6 and 7.

IC15, a 7400 quad 2-input NAND gate IC, is used for clearing the memories at power switch 'on' and to invert the counter output before it is stored in the memory. Since the memory outputs are inverted by feeding inverted data, the right output is obtained.

At power switch 'on', monostable IC13 is activated, producing a high-going pulse at its pin 3. (Refer Fig. 3 of Part I). This is inverted by transistor T1 and fed to pins 2, 5, 10 and 13 of ICs 15, 18 and 21. Since at least one input of each of these NAND gates is forced low, their corresponding outputs at pins 3, 6, 8 and 11 of ICs 15, 18 and 21 go to logic 1. This places a '1111' at the memory inputs of ICs 14, 17 and 20.

Further, pin 1 of IC12 (on main board) is held low during this period. IC12 is a quad 2-input data selector which selects data between the input available at pins 2, 5, 11 and 14 and the input available at pins 3, 6, 10 and 13 according to the control input at its pin 1. During the period that pin 1 is held low, the input at pins 2, 5, 11 and 14 (i.e. the output of counter IC8) is available at its output pins 9, 12, 7 and 4. This causes all the memory locations to be strobed in quick succession.

Since the pulse generators are also triggered during 'power up', a 'write enable' pulse is provided at pin 3. This clears the entire contents of the memory and a '0000' is written at each address. The 'memory clear' sequence is initiated automatically at power switch on.

Once the monostable IC13 has timed out, its pin 3 goes low thereby switching off transistor T1. Now since pin 1 of IC12 goes high, the output of IC11 is placed on the memory address lines. The machine is now ready for use.

The monitor/display board

The monitor board is used by the polling booth incharge for controlling the voting machine. It also indicates the total votes polled during a particular time period.

Whenever the 'vote' switch is pressed, a down-going pulse is available at pin 12 of the control flip-flop. This is used for counting the total votes polled during a day. Ripple counter 7490 ICs are used. The clock pulse from the control flip-flop is fed to pin 14 of IC23. The count is available at pins 12,9,8 and 11. The output at pin 11 is fed to the clock input of the next counter. With four counters, a total vote-count of '9999' is possible. More can be cascaded if desired.

In order to utilise the same displays for indicating the results and the total votes polled, IC 74157s are used. 7446 ICs decode the BCD count for the 7-segment displays.

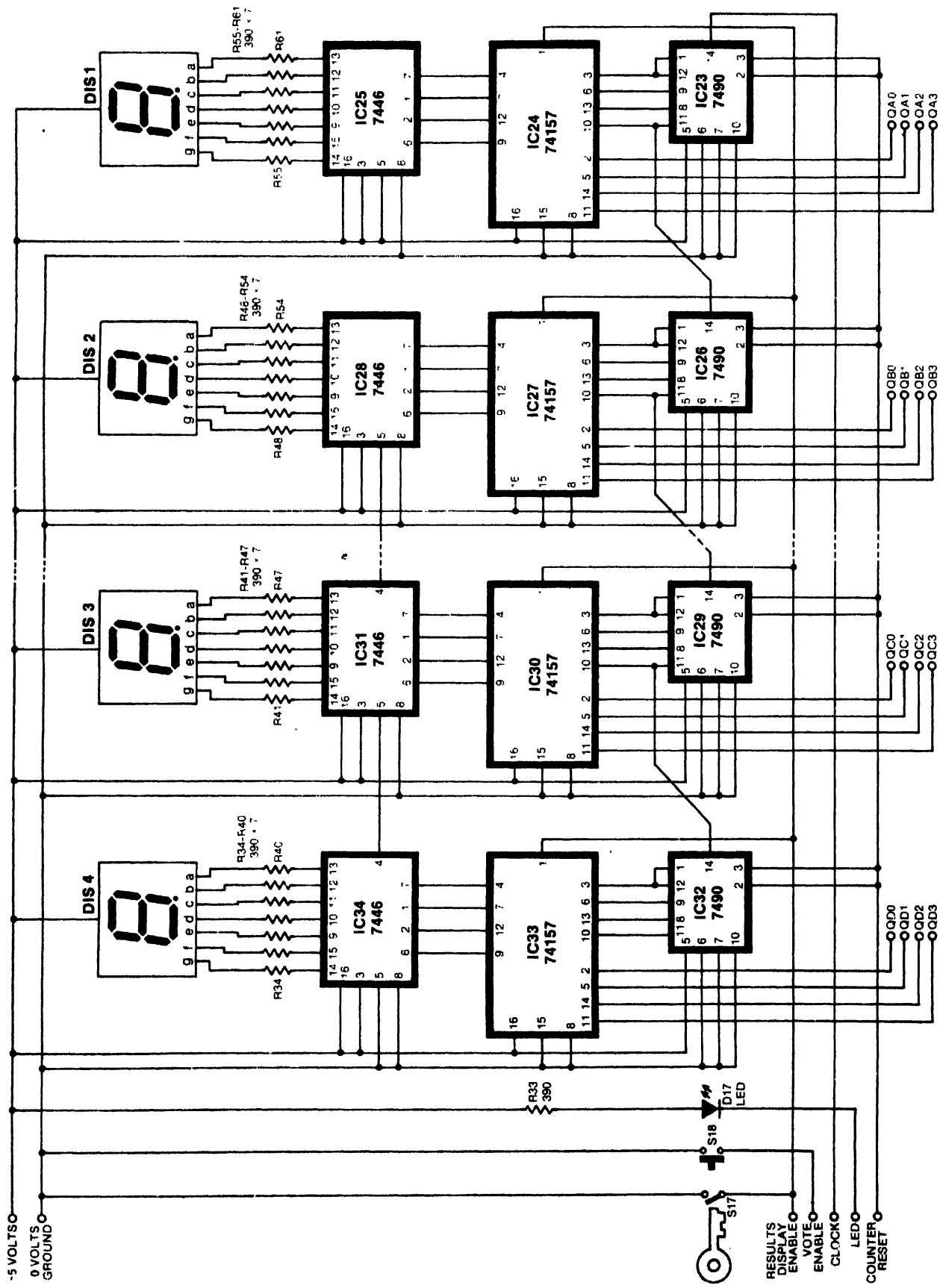

Fig. 8: Circuit diagram for Monitor board.

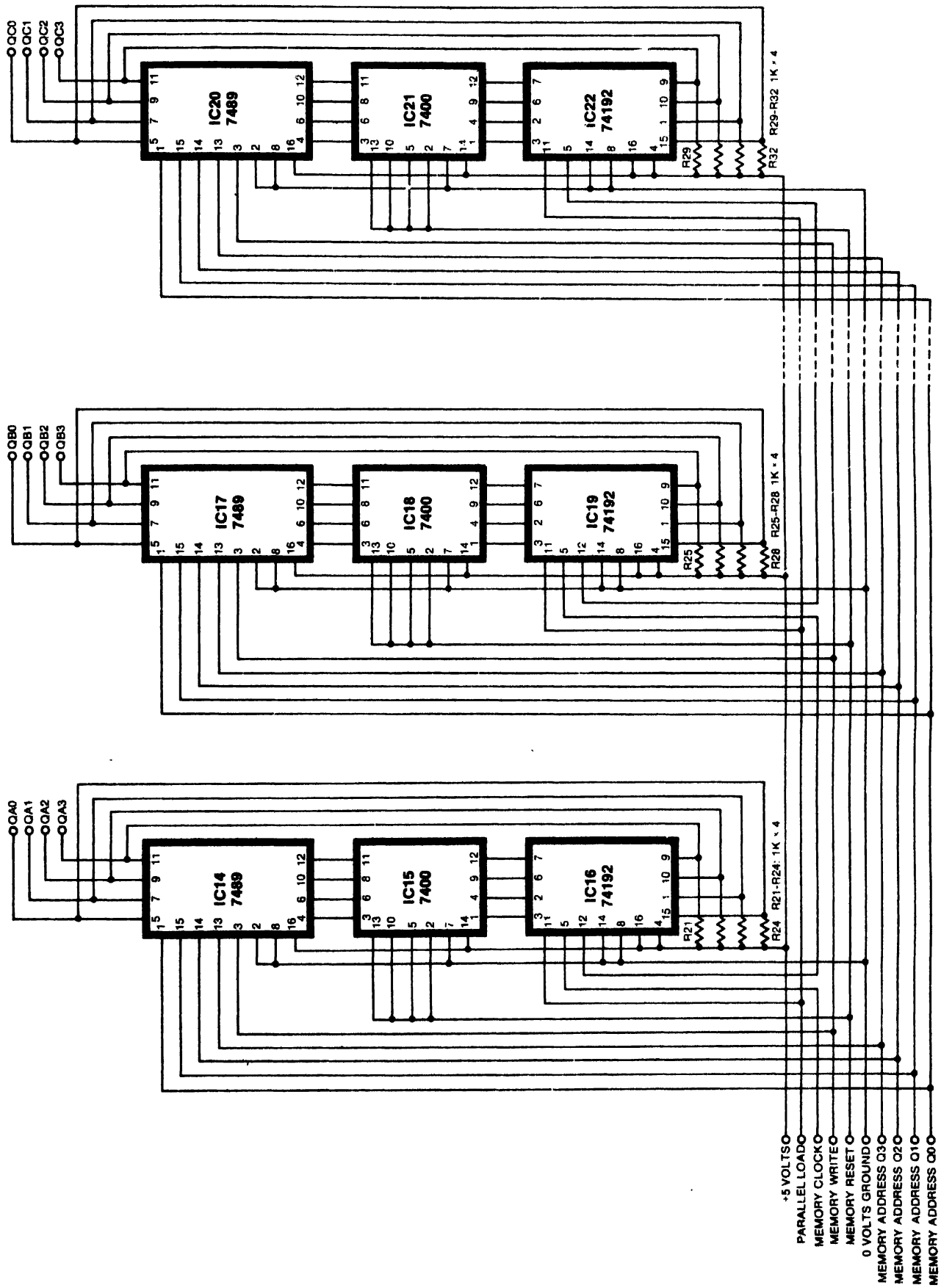

Fig. 9: Circuit diagram for memory board.

PARTS LIST

(For Memory Board)

Semiconductors:

IC16, IC19, IC22	74192 presettable BCD up/down counter
IC15, IC18, IC21	7400 quad 2-input NAND gate
IC14, IC17, IC20	7489 64-bit random access memory

Resistors (all ¼ watt, 5% carbon)

R21-R32	1 kilohm

Miscellaneous:

IC sockets, PCB, ribbon cable, PCB connectors, suitable enclosure, spacers, nuts, bolts and washers etc

PARTS LIST

(For Monitor Board)

Semiconductors:

IC23, IC26, IC29	
IC32	7490 BCD ripple counter
IC24, IC27, IC30, IC33	74157 quad 2-input data selector
IC25, IC28, IC31, IC34	7446 BCD to 7-segment decoder driver
DIS1-DIS4	LND507 common cathode display

Resistors (all ¼ watt, 5% carbon)

R34-R61	390-ohm

Miscellaneous:

S17	Auto ignition key switch
S18	Push-to-on switch
	PCB, IC sockets, ribbon cable, PCB connectors, spacers, nuts, bolts, washers, suitable enclosure etc

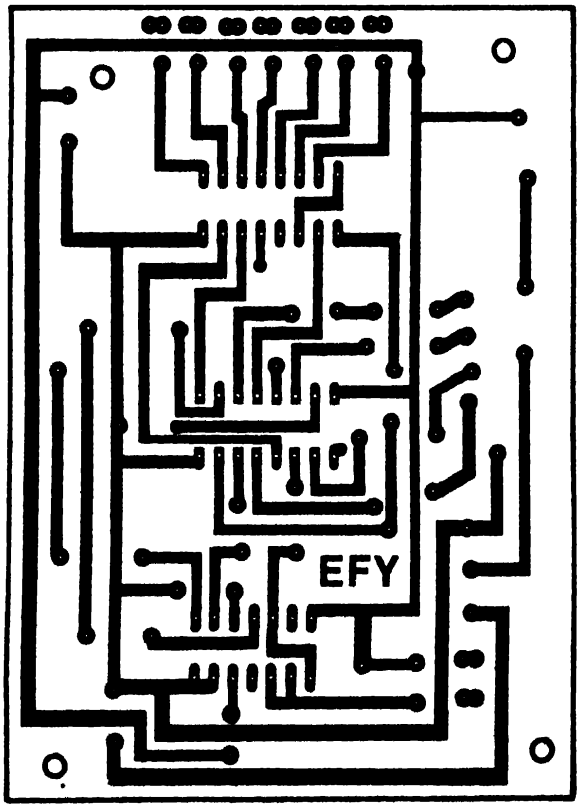

Fig. 10: Actual size PCB layout of monitor board for single display operation. To extend the display digit to more than one join two or three boards serially as per the number of digits required.

Power supply

The unit requires a current of about 950 mA. The current can be reduced considerably by using the 'LS' version of the TTL ICs instead of the normal TTL ICs used in the prototype.

Since the current consumption is high, it is not advisable to run the machine on battery power alone. However, to ensure that the memories are not wiped out due to power failure, a battery back-up is essential. The circuit of a suggested power supply is shown in Fig. 14.

Transformer X1 steps down the mains voltage to 12 volts which is rectified by diodes D18 and D19. IC35, a variable voltage regulator IC, is used for obtaining a 9 volt regulated output. The output voltage is adjusted by potentiometer R62. Similarly, the battery output is regulated by IC37 to provide an 8 volts output.

As long as the mains supply is available, diode D25 remains reverse biased and no current flows from the battery. However, if the mains fail, D25 is no longer reverse biased and current will flow from the battery.

IC36 finally steps down the voltage to 5 volts -- the voltage suitable for operating the TTL ICs.

Operating the machine

At power switch on, as we have seen earlier, the machine automatically clears the memories and the 'total votes polled

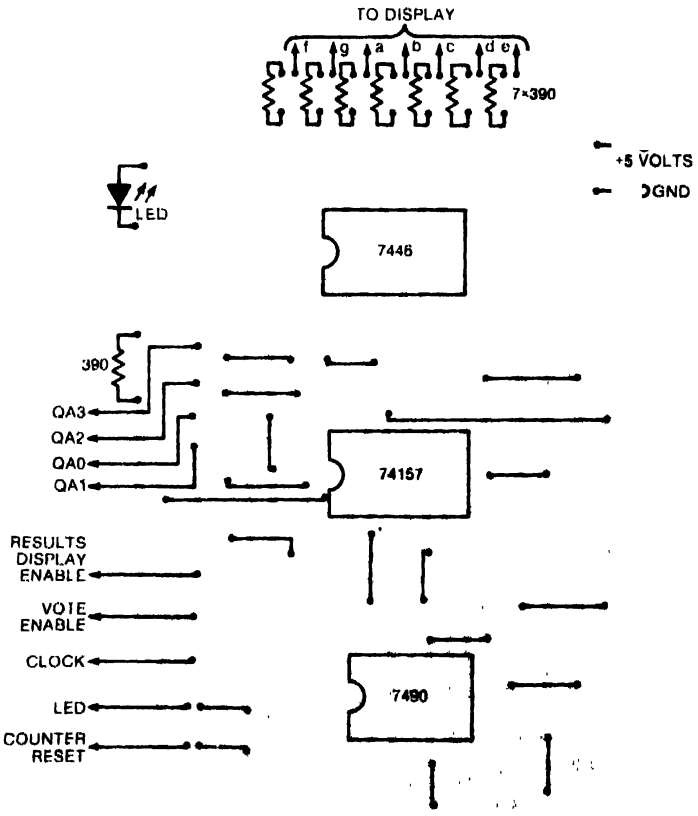

Fig. 11: Component layout for PCB.

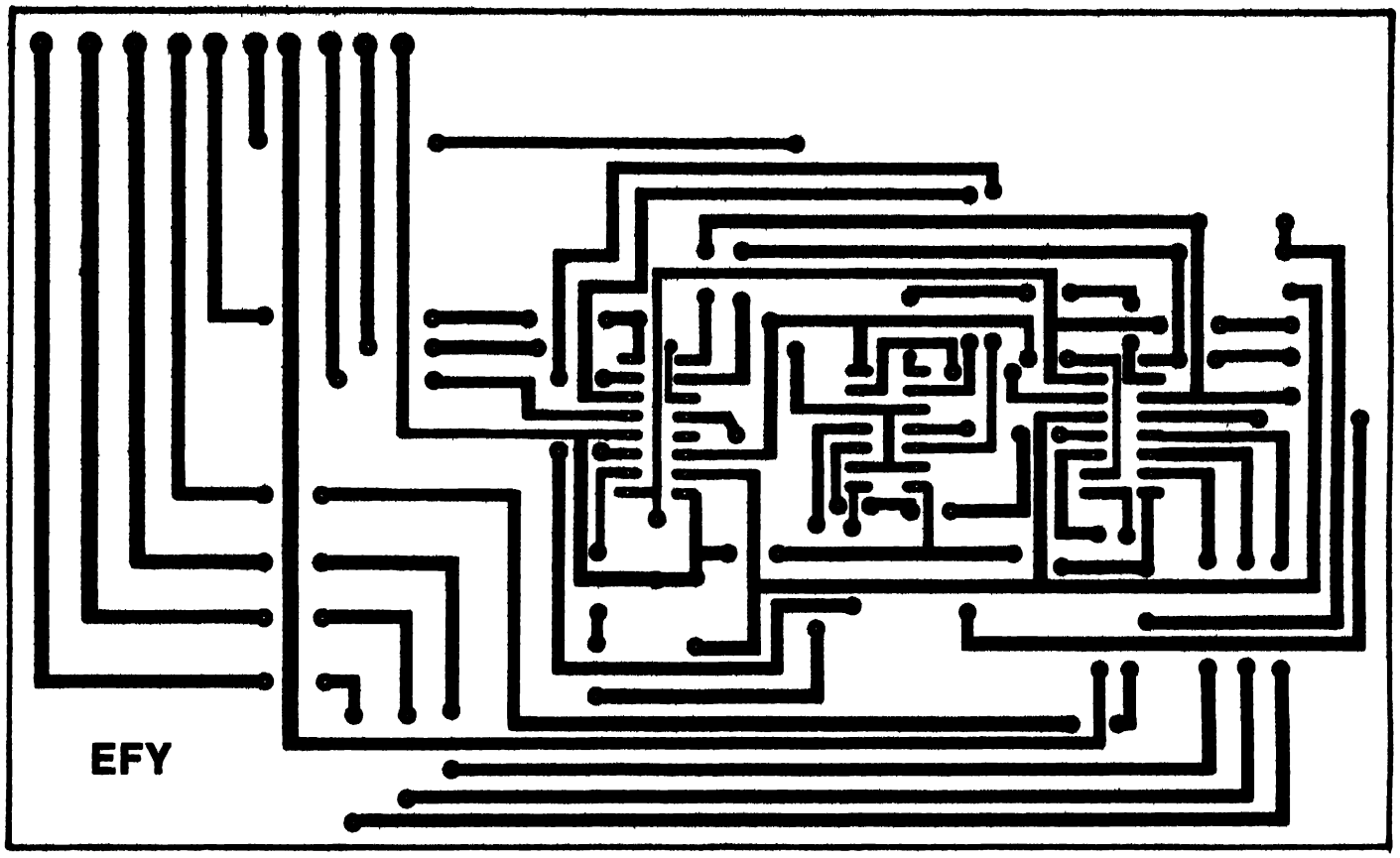

Fig. 12: Actual size PCB layout of memory board for single display monitoring. To extend the display digit to two or three join two or three such boards serially

Fig. 13: Component layout for PCB.

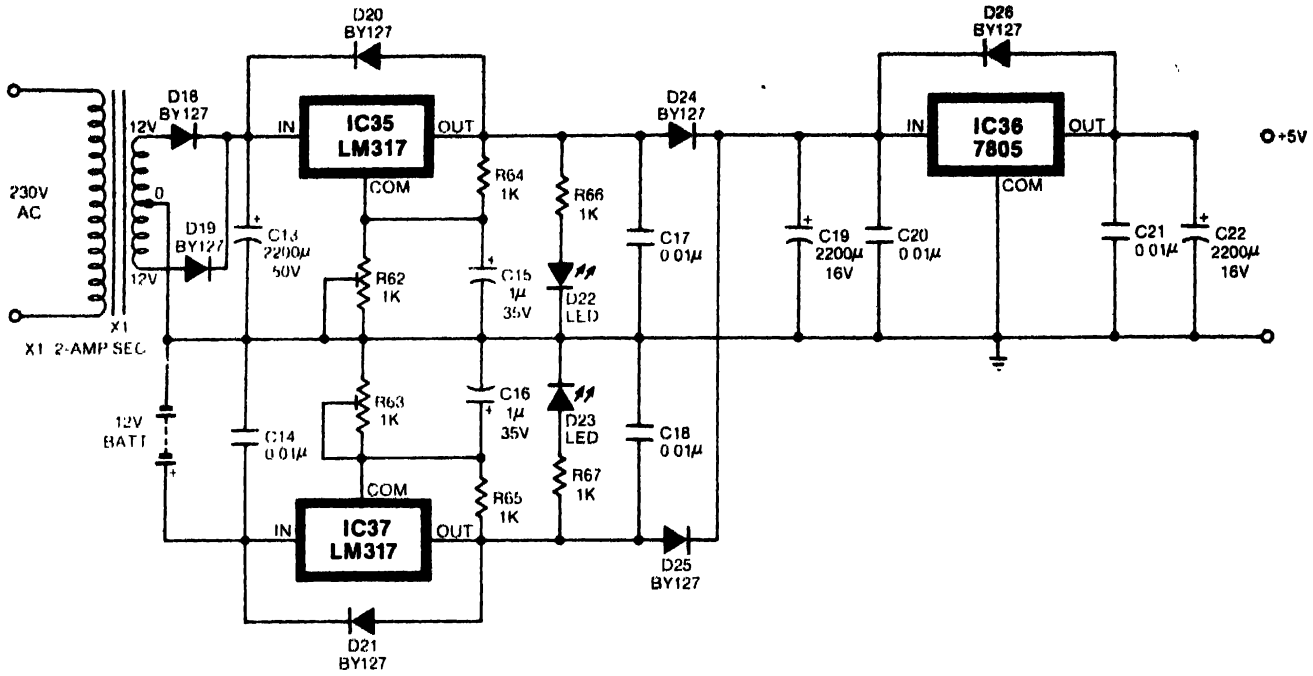

Fig. 14: Circuit diagram for power supply.

PARTS LIST

(For Power Supply)

Semiconductors:	
IC35, IC37	LM317K, 3-terminal adjustable regulator
IC36	LM7805, 5-volt voltage regulator
D18-D21, D24, D25, D26	BY127, 1-amp rectifier diode
D22, D23	5mm light emitting diode
Resistors (all ¼ W, 5% carbon)	
R64-R67	1-kilohm
R62, R63	1-kilohm, vertical preset
Capacitors:	
C13	2200μF, 50V electrolytic
C14, C17, C18, C20, C21	0.01μF ceramic disc
C15, C16	1μF, 35V tantalum
C19, C22	2200μF, 16V electrolytic
Miscellaneous:	
X1	12V-0-12V, 2-amp secondary transformer, Heatsink for voltage regulator, LED holders, mains cord, battery connectors, suitable enclosure, screws and nuts, bolts, spacers etc

counters'. The machine has to be enabled by the polling booth incharge before the first vote can be cast.

After verifying the credentials of the voter, the booth incharge presses 'enable' switch S18. Pin 8 of IC2 will go low. This will 'enable' the parallel load inputs of the memory counter ICs. Pin 6 of IC2 will go high, thereby enabling IC10. The keyboard now becomes operative.

The voter chooses his candidate by pressing the appropriate switch. The corresponding binary word is latched in IC11. This is used for addressing the memories. Since the parallel load inputs of the memory counters are enabled during the period, the memory contents get loaded into the counters.

On pressing the vote switch, pin 8 of IC2 goes high. Parallel load is disabled. Further, a down-going pulse is received at pins 3 and 4 of IC4 which produces a low-going pulse at its pin 1. The rising edge of this pulse serves as a clock for the memory counters. The pre-loaded data is therefore increased by one.

Thereafter, the second pulse generator is activated which produces a low-going pulse at pin 4 of IC5. This serves as a 'write enable' pulse for the memories. The contents of the memory are therefore replaced by the counter output. This in effect means increasing the previous data in the memory by one.

As such, the voter's desire is recorded at the location corresponding to his choice. The pulse available at pin 13 of IC5 enables an astable which generates an audio tone. This serves as an annunciator for indicating that the vote has been registered.

The third pulse generator is activated next. This produces a 'latch enable' pulse. Further, since after pressing the 'vote' switch, pin 6 of IC2 goes low, the outputs of IC10 are held high. The latch registers a '0000' on receipt of the 'latch enable' pulse. This is essential to maintain secrecy of the voter.

At the end of the day, the 'results enable' switch is activated. Pin 6 of IC2 is forced high which enables the keyboard. Further, the contents of the memory are diverted to the decoder displays by ICs 24, 27, 30 and 33. As such, the displays will indicate the results of the candidate corresponding to the key pressed on the keyboard.

Further, if any person tries to cast vote to two persons simultaneously an invalid vote will be registered. This happens because, if any key is held pressed after the 'vote switch' has been pressed, the latch resets and addresses '0000' location of the memory, thereby passing no benefit to the candidate.

(Concluded)