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Combating noise effects in adaptive cable equalizer designs

The adaptive cable equalizer is an essential component in the receiver front-ends of serial digital video (SDV) broadcast and serial telecommunications equipment. These equalizers can also be used in other types of wired communications systems. Equalizers interface directly with the transmission line and restore the signal amplitude and bandwidth loss caused by the cable. Because it connects directly to the cable, the equalizer is vulnerable to the effects of ESD, EMI/RFI, and device-generated noise. The equalizer's operating characteristics also tend to exaggerate the effects of noise on a design. A robust system using an adaptive cable equalizer which combats interference must also preserve the equalizer's desirable operating characteristics such as wide input dynamic range, wide signal bandwidth, low residual output noise, high input return loss, and maximum cable length of equalization.

ESD, EMI/RFI, and device-generated noise are the three main interference modes in wired communications systems. ESD can damage or destroy active and passive devices whether in or out of circuit. EMI/RFI compromises system signal handling, and if serious enough, basic system functionality can fail. Device-generated noise can degrade performance by compromising circuit operation which also can lead to system failure.

Designing systems that are robust when subject to the types of interference mentioned is no small challenge. Adaptive cable equalizers are not simple digital devices, an essential fact designers must appreciate. The National Semiconductor CLC014, CLC012, and the new CLC034 adaptive cable equalizers are high-performance analog devices. They are high-gain, wideband, analog, RF, AGC amplifier filters. They and all other system components such as the enclosure, the passive components, and the PCB, when properly integrated, resist internal and external interference.

Normally when the cable length is a maximum, the signal received by the equalizer is a minimum. Therefore, the equalizer gain and bandwidth are at maximums. But the gain and bandwidth are also maximums when the input is unconnected and there is no apparent signal. Under these maximum gain conditions, even small amounts of unwanted EMI or conducted interference are greatly amplified and compromise proper equalizer operation. Good PCB design stops the interference and prevents some common equalizer application faults such as:

- Inability to equalize the maximum cable length at a given data rate
- Data errors with cables which are less than maximum length
- Spurious or random output data when the input is unconnected
- False detected signal indications

These faults are usually caused by one of the following things:

- Radiated EMI originating inside the system enclosure or from the PCB
- Noise coupled to the inputs from logic devices or the power supply via the input network component mounting-pads
- Crosstalk to the input and/or AEC circuits from other nearby circuits
- Coupling between the input and output circuits of the equalizer

ESD events can cause major damage to semiconductors, particularly when they are not protected by conductive packaging materials and are most vulnerable. Semiconductors can also be damaged even after mounted on the PCB. Devices intended for direct cable interface such as line drivers and cable equalizers are designed to maximize ESD voltage ratings. Even so, it is unwise to rely only on the semiconductor to provide all of the ESD protection regardless of how high its ESD rating may be. Equalizer input circuits have the advantage of a low impedance path through the termination resistor to ground which increases ESD resistance. Components used in the input circuit should have ESD withstand

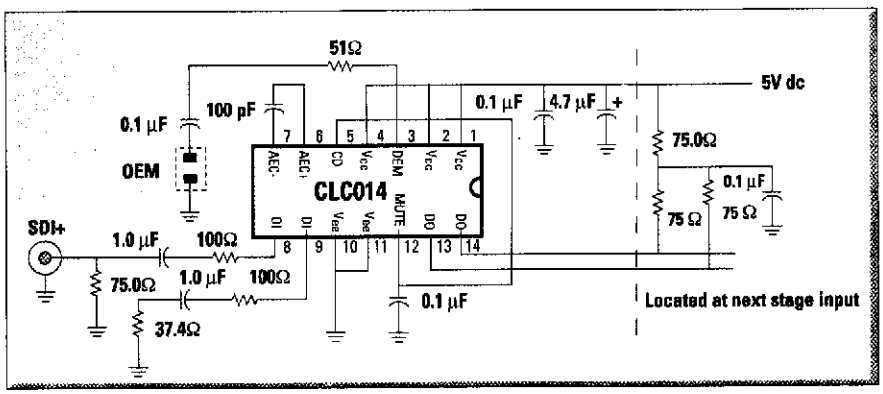

Figure 1—Equalizer schematic

ratings sufficient to handle the design maximum ESD event unaided. By proper choice and design, all circuit components, the enclosure, connectors, and the PCB can enhance ESD protection of the equalizer and other interface devices.

These simple design practices combat electrical interference and improve overall equalizer operation.

- Isolate or shield equalizer input networks and the AEC circuit from external and on-card, high level signals
- Use robust input network components to suppress ESD events
- Use multi-layer PCBs with separate transmission line and power/ground layers for isolation, shielding, and ESD protection
- Use thin dielectrics for power-ground layer pairs, 6 mils or less, to increase intrinsic capacitance and high-frequency attenuation
- Use two vias for pad-to-plane connection of bypass capacitors, termination resistors, collector load resistors, and V_{CC} and V_{EE} pins

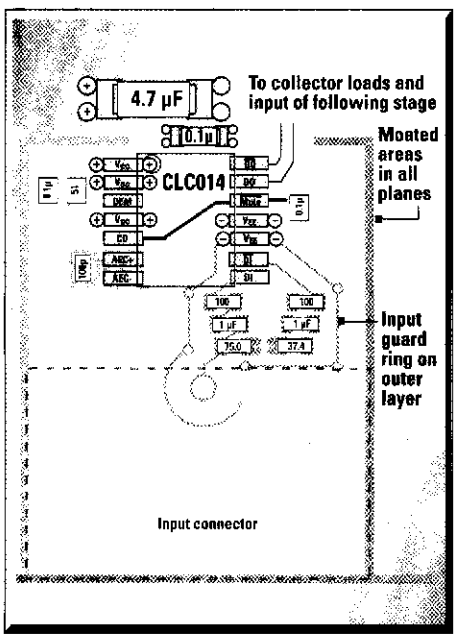

Figure 2—Input circuit guarding

- Do not connect multiple V_{CC} and V_{EE} pins to a single via as this may induce noise in the device

The recommended CLC014 equalizer circuit is shown in *Figure 1*. *Figure 2* shows a corresponding PCB layout. On the PCB, several things have been done which isolate the equalizer circuit from unwanted signal interference. The coupling path for noise from the power planes to the input and AEC circuits is prevented by removing copper in plane layers under the input networks and the AEC capacitor.

The equalizer circuit has been isolated by removing strips of copper (dark shaded lines) in all plane layers. These moats prevent signals in adjacent circuits from directly reaching the equalizer circuit through the planes. To reach input circuits, interference signals must follow a longer path around the moats. This adds low-pass filtering and increases attenuation for unwanted signal.

Cable drivers used to provide a signal loop-back function are frequently located adjacent to the equalizer. The cable driver output signal is usually much larger than the signal being received by the equalizer. Moats help isolate the cable drive signal and reduce interference with the equalizer input signal.

Surround the input circuits with a well-grounded guard (shield) ring to reduce RFI pickup as shown in *Figure 2*. Copper floods on the outer PCB layers may be used instead of guard rings, *Figure 3*. The copper floods must be connected to all ground planes at about 1 cm intervals to form an effective shield.

The common-mode rejection of the equalizer's differential input amplifier and a symmetrical input component

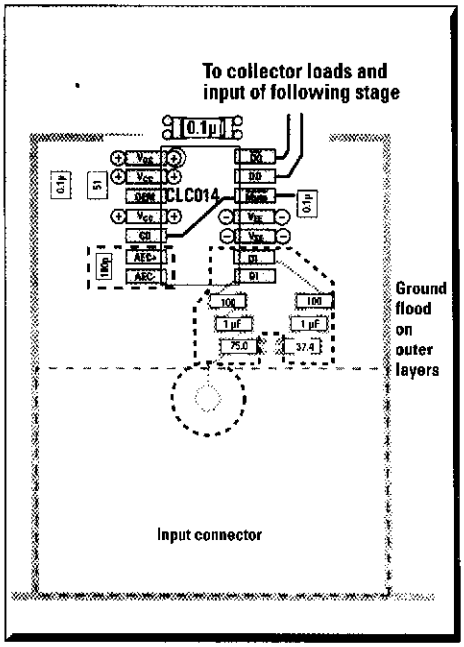

Figure 3—Using copper floods for shielding

layout will improve RFI rejection. RFI will be a common-mode signal when received equally by both inputs. A symmetrical input circuit layout with balanced termination impedances equalizes RFI signals reaching both inputs so that the common mode rejection of the input differential amplifier can cancel most of the interference signal.

Interference can be minimized and adaptive cable equalizer performance enhanced using the simple techniques described here. Moreover, these design techniques cost nothing to use. Interference rejection and operational reliability are more economical to design in first than to add later. By making these design recommendations the starting point for your adaptive cable equalizer design, you will improve their performance in your system and eliminate the need for redesigns to fix interference and performance problems. ■

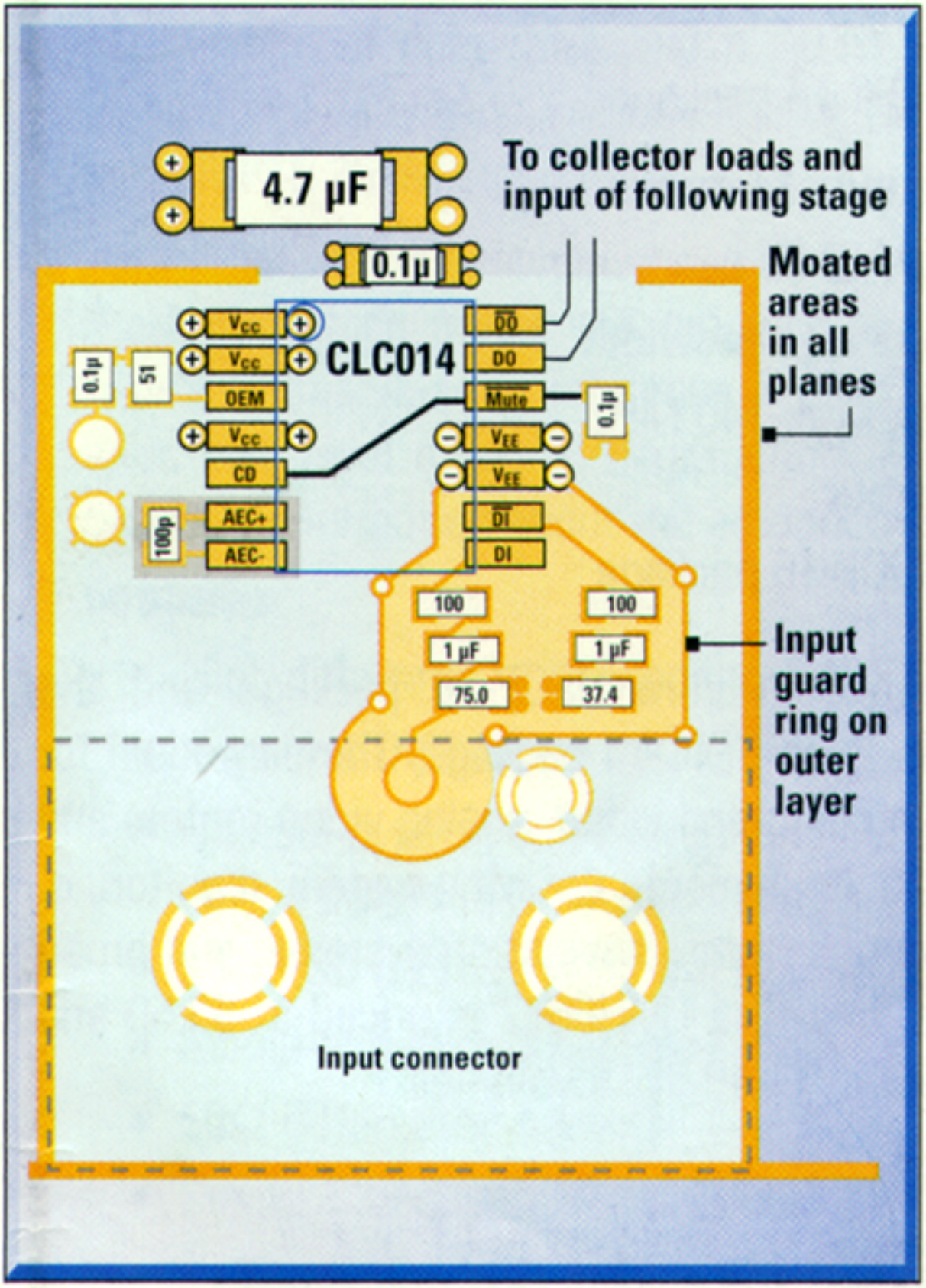

Figure 2—Input circuit guarding

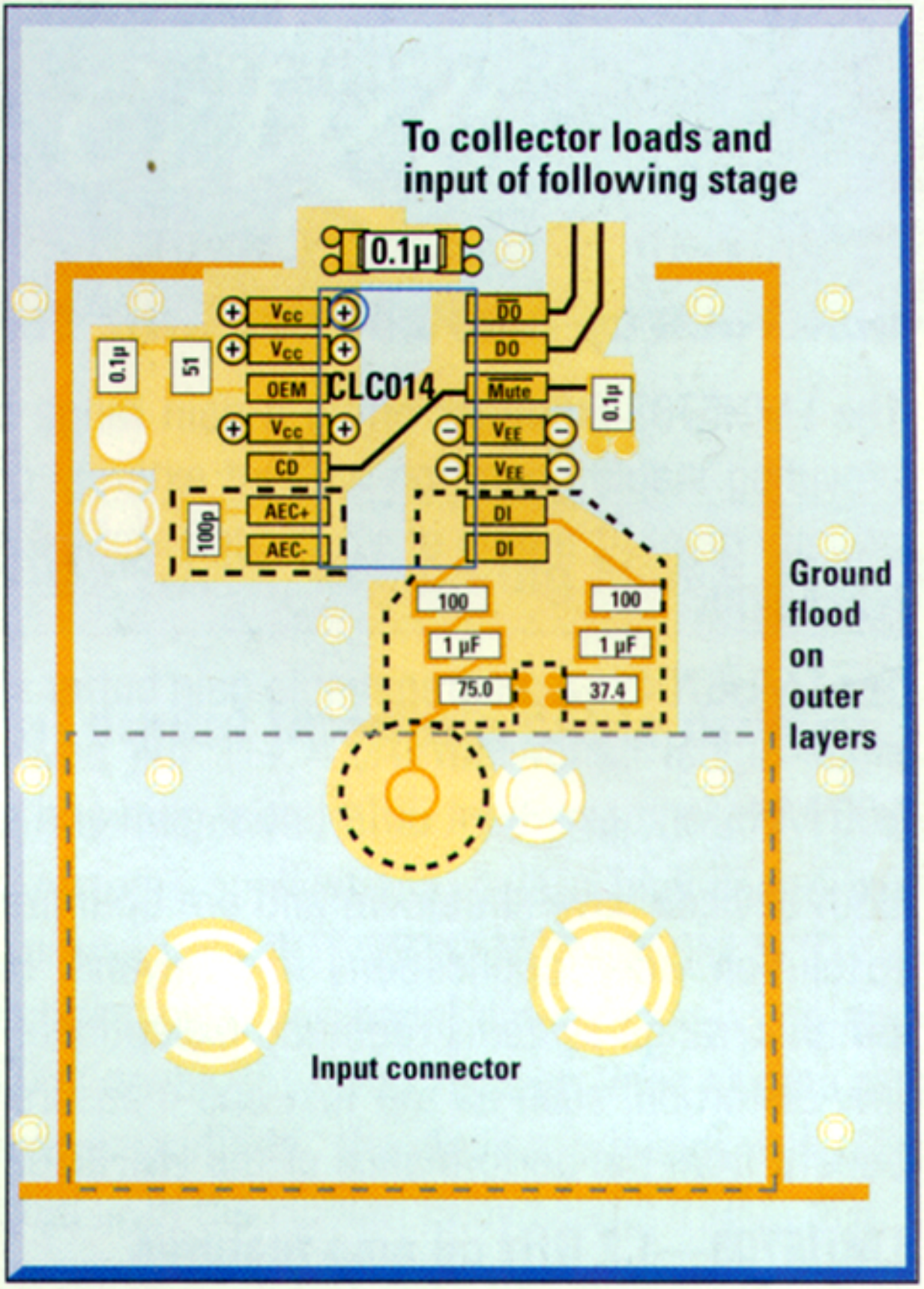

Figure 3—Using copper floods for shielding