USING HYPERLYNX DRC TO FIND EMI ISSUES

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HIGH SPEED DESIGN

WHITEPAPER

ELECTROMAGNETIC INTERFERENCE

Electromagnetic interference, or EMI, is a disturbance that could degrade the performance of an electrical circuit, thus preventing it from functioning correctly, or not functioning at all. EMI on PCBs is caused by unintended radiation from circuit elements, traces, vias, and connectors. High speed PCB designs are more vulnerable to EMI problems if not designed to properly suppress unwanted radiation.

COMMON CAUSES OF EMI IN PCBS

Here are a few typical causes of EMI problems and how they can be avoided in PCB designs.

INTERRUPTED RETURN PATH

An interrupted return path is a very common, and can be an unintentional source of EMI issues (Figure 1).

At high frequencies, a signal traveling along a trace is traverses through electromagnetic fields which are coupled through the trace into the nearest plane (also known as reference planes), which act as current return paths and thus form a closed current path. If this closed current path is interrupted, or broken, radiation occurs, causing EMI issues.

Typical interrupted return path cases include a net crossing gap, a net near a plane edge, and reference plane changes.

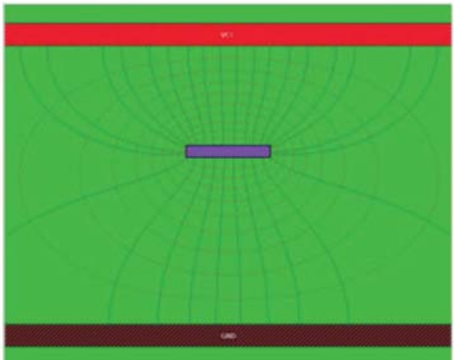


Figure 1: Interrupted return path

NET CROSSING A GAP

Also known as trace-crossing split, or signal-crossing split, a net crossing gap occurs when a trace return path, i.e. on its reference planes, is a split so that interrupts the return path (Figure 2). The split could be a "hole" on a single plane, or a gap between two power islands.

Ideally all high speed signals should be referenced to solid ground planes. But if a split happens, a stitching capacitor should be used to form an AC path through the gap.

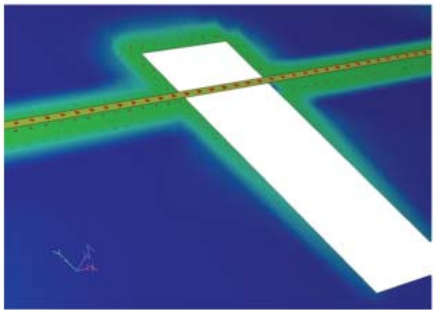


Figure 2: A net crossing a gap.

NET NEAR A PLANE EDGE

If a high speed signal trace is routed near its reference plane's edge, the electromagnetic field will wrap around the edge and radiate some energy.

There are two common cases when this happens. One happens when a trace is routed too close to the edge of a board (Figure 3). The second, Figure 4, occurs when a trace is routed too close to a large void on the reference plane.

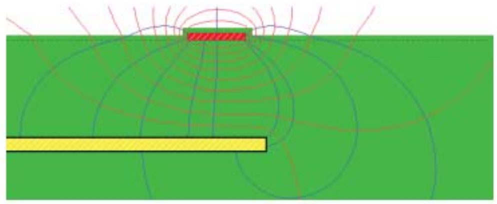


Figure 3: A trace routed too close the edge of the board can produce EMI.

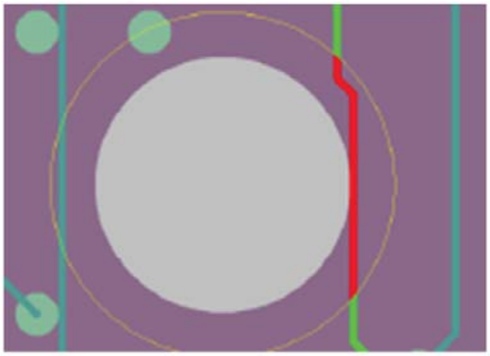


Figure 4: A trace routed near a large void on the reference plane can produce unwanted EMI.

REFERENCE PLANE CHANGE

When a signal is routed from one layer to another layer through a via, it can result in the signal's return path changing, making the closed current path even more complicated. In this case, the current flowing on the traces of different layers couples (or references) to different planes, and the return current on these different reference planes needs to be continuous as well, otherwise the whole current loop is interrupted, or broken, and subsequently produces EMI issues (Figure 5).

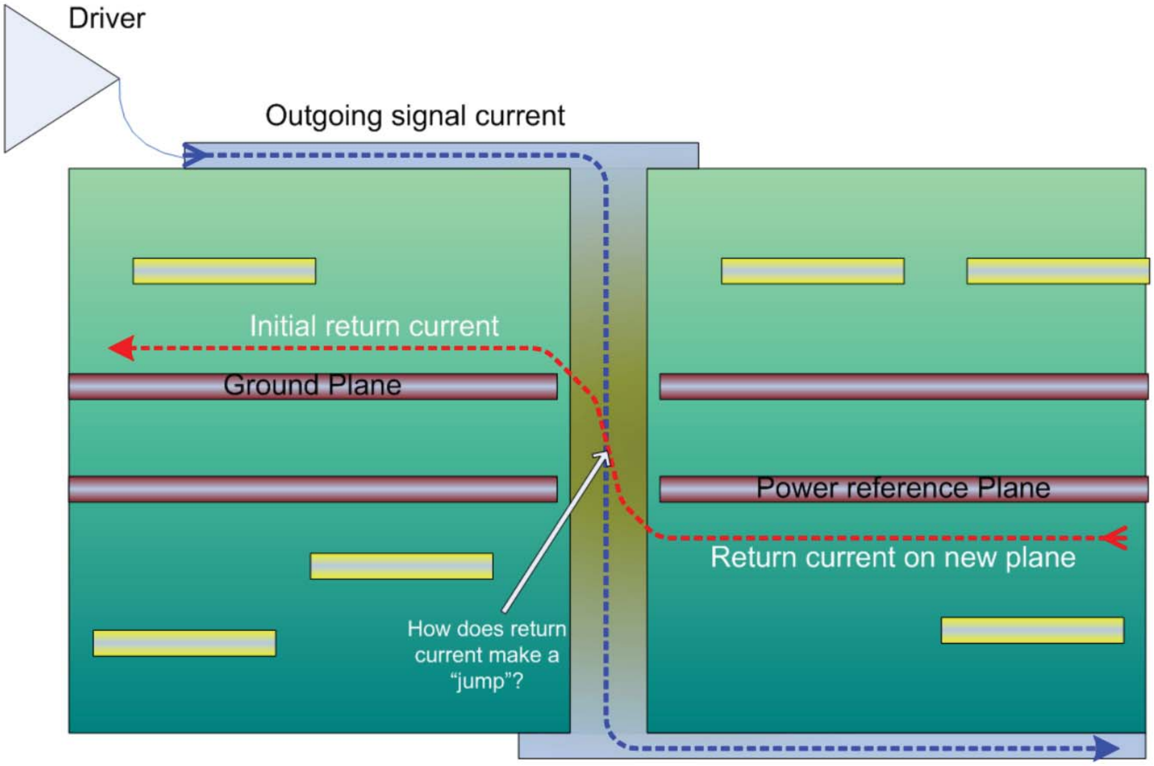


Figure 5: Unintended current flow, and unintended EMI, can result from a signal path that changes reference planes.

To ensure a closed current path, you must provide a continuous path for the return current:

- If the reference plane changes from power to ground, one or more stitching capacitors is required
- If the reference plane changes between grounds (or same-voltage planes), one or more stitching vias is required

ISOLATED METAL AREAS

Isolated metal areas are usually unwanted and isolated metal areas left in a PCB design, they are commonly unintentional sources that cause EMI issues.

VIA STUB

A via stub is a via, or portion of a via, that may have its pad removed and does not connected to any layer thus the via stub is not in series with a signal flow (Figure 6). However, the stub may be drilled and plated during the manufacturing process, thus form an isolated metal area. In a high speed design a long via stub can act as an antenna and emit energy.

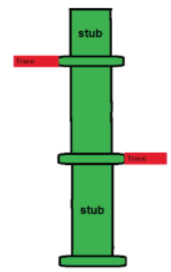


Figure 6: A via stub.

METAL ISLAND

A metal island is an isolated, floating metal area on a board, which can act like an antenna and radiate energy, thus causing EMI issues. The metal island should be properly connected with vias at both ends, as shown in Figure 7, to avoid radiation.

Figure 7: A metal island needs vias at both ends.

INTEGRATED CIRCUITS

An integrated circuit can be a source of EMI through coupling its energy to certain objects such as planes, etc.

IC OVER A PLANE SPLIT

Some ICs lack reference planes within their package, thus rely on a solid plane underneath their placement on the board to provide a continuous return path. If that path doesn't exist or is split, unintended radiation can occur (Figure 8).

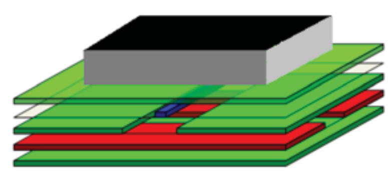


Figure 8: An IC mounted over a plane split.

DECOUPLING CAPACITOR REQUIREMENTS

Decoupling capacitors are usually required to be placed close to IC power pins as possible. Even a short trace to the capacitor can radiate.

VULNERABLE SIGNALS

Certain signals, if not handled properly, are vulnerable to radiate energy and cause EMI issues.

EDGE-RATE-TO-PERIOD RATIO

A high speed signal with fast rising and/or falling edges and with a small edge-rate-to-period ratio, shown in figure 9, carries higher frequency harmonics, this not only increases the risk of radiated emissions, but also causes signal integrity (SI) issues.

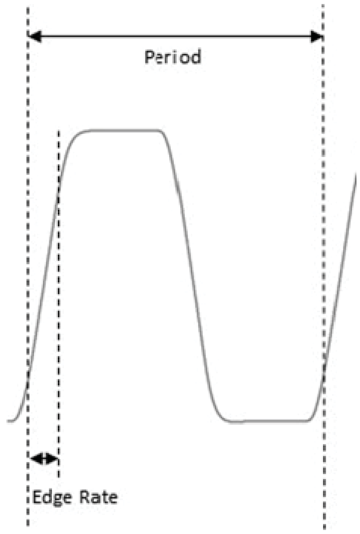


Figure 9: Edge-rate-to-period ratios that are too small can produce high frequency harmonics and EMI.

SIGNAL SHIELDING AND EXPOSED LENGTH

Periodic signals, such as clocks, pose the risk of generating an impulse of radiated energy at certain operating frequencies. To prevent this, the signals should either have continuous current return paths (referencing solid planes) as discussed previously, or be properly shielded on both sides of traces with guard traces or metal. Otherwise, the non-shielded portion of traces can act as antennas and radiate energy.

I/O NETS AND CONNECTORS

There are a several reasons that high frequency energy could leave the system through a connector on the board. For example, if I/O nets couple with high speed signals, the resulting high frequency noise generated can leave the system. One way to prevent this from happening is to place a choke near the connector pins

BOARD SHIELDING

Adding metal-fill edges near the board outline is a technique to shield a board and reduce the radiation emitted from the board. To make the edge shield more effective, metal-fill edges need to be connected with stitching vias, and these vias should be close to each other.

HYPERLYNX DRC

Known radiation sources on PCBs should be taken care of by carefully designing the board, for example, adding filters close to a connector's pins, shielding a board in the proximity of the board outline, adding guard traces to high speed clocks, and so on. But human error can leave certain known sources untreated thus lead to failure. Identifying them requires knowledge, patient, time, intense labor, no human errors.

On the other hand, many EMI problems are actually caused by unknown or unintentional sources, for example, interrupted signal return paths, via stubs, etc. The number of sources could be dozens, hundreds or even thousands, manually finding them is impractical.

HyperLynx DRC, an electrical design rule checker, helps effectively and efficiently review layout designs for electrical performance. One of HyperLynx DRC capabilities is to automatically identify potential EMI issues on PCB boards. The inspection process is automated to eliminate errors that can be generated with manual inspection and reduce hours — or days — worth of tasks to just minutes. It also provides accurate and informative result for problem examination and design correction. In addition, HyperLynx DRC is customizable and expandable so that you can develop custom DRC checks.

In short, HyperLynx DRC is an excellent way to capture and preserve design knowledge and consolidate checks done by multiple disciplines into a single, comprehensive set of checks. A2ll DRCs are repeatable and reusable for every different design.

HYPERLYNX DRC EMI RELATED RULES

HyperLynx DRC provides a set of EMI-related DRC rules to help identify all potential EMI issues discussed in this paper. Those rules include:

- Edge- rate-to-period ratio
- Edge shield
- Exposed length
- Filter placement
- ICs over split
- I/O coupling
- Metal island
- Net crossing a gap
- Net near a plane edge
- Vertical reference plane change
- Via stub length

These rules are parameterized and customizable, which means that per design specific requirement, violation conditions are different from design to design, and these rules can be adjusted to fit the different requirements.

Each rule can be run on the whole design. For example, you can run the via-stub length rule to find all via stubs that exceed the certain length specified through the rule's parameter settings. Rules can also be applied to portion of design, such as critical part or more vulnerable part, for example, you can run the vertical reference plane change rule for all clocks of a DDR3 interface to ensure closed current paths.

Each rule is self-documented with its purpose, parameter explanations and violation conditions. A rule document can be viewed directly in HyperLynx DRC user interface.

PERFORMING CHECKS

Running EMI checks in HyperLynx DRC is a process as simple as five easy steps:

1. **Load layout design** — This simply loads a layout design into HyperLynx DRC; various EDA vendors and layout formats are supported.
2. **Prepare the data to be checked** — You can gather the critical or vulnerable parts of a design to be checked, and categorize them into different groups so that the necessary rules can be setup and applied.
3. **Set up DRC rules and their parameters** — As explained, a rule can be run on the whole design, or portion of design. You can also run a rule with multiple instances, and each instance is run on different portion of design with different requirements.
4. **Run DRCs** — Depending on the number of checks and the complexity of a design, a complete EMI board check takes a few minutes to less an hour.
5. **Examine the results, or violations** — If any EMI issues exists in a design, they will be flagged and recorded as violations in HyperLynx DRC. You can then examine and highlight violations in board viewer, prioritize them if necessary, create and export violation reports to present to necessary parties.

HYPERLYNX DRC RULE EXAMPLE – NET CROSSING A GAP

The Net Crossing Gap rule is for identifying one of the interrupted return path cases, the rule itself is self-documented in HyperLynx DRC, as shown in Figure 10 when the rule is selected:

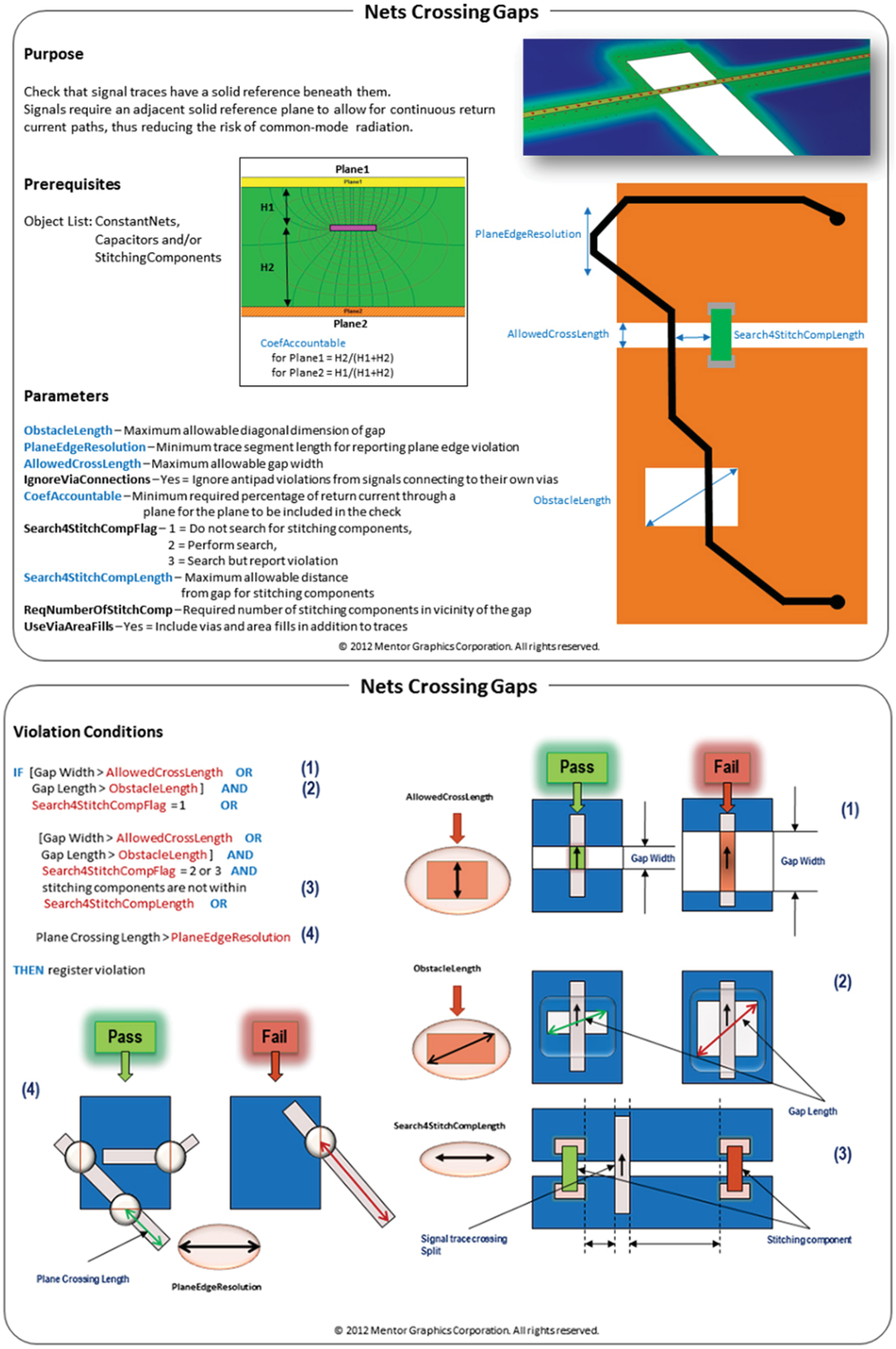
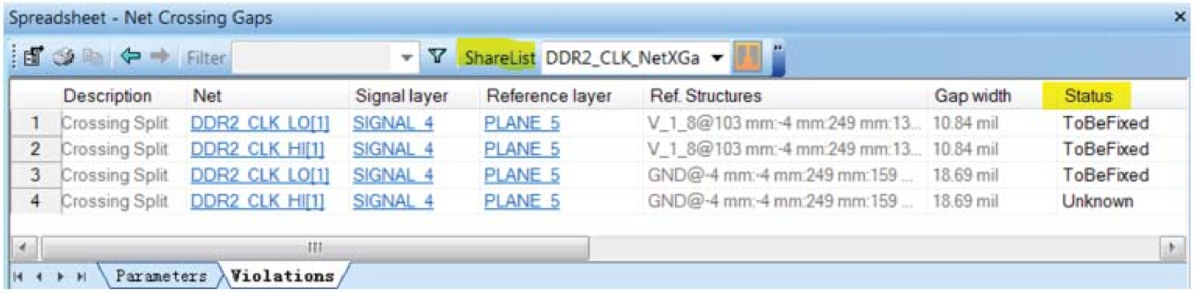


Figure 10: HyperLynx DRC example.

The rule can be applied to the whole board, or a particular portion of interest. Figure 11 shows an example with four violations that were caught on the DDR2 clocks of a design:



	Description	Net	Signal layer	Reference layer	Ref. Structures	Gap width	Status
1	Crossing Split	DDR2_CLK_LO[1]	SIGNAL_4	PLANE_5	V_1_8@103 mm:-4 mm:249 mm:13...	10.84 mil	ToBeFixed
2	Crossing Split	DDR2_CLK_HI[1]	SIGNAL_4	PLANE_5	V_1_8@103 mm:-4 mm:249 mm:13...	10.84 mil	ToBeFixed
3	Crossing Split	DDR2_CLK_LO[1]	SIGNAL_4	PLANE_5	GND@-4 mm:-4 mm:249 mm:159 ...	18.69 mil	ToBeFixed
4	Crossing Split	DDR2_CLK_HI[1]	SIGNAL_4	PLANE_5	GND@-4 mm:-4 mm:249 mm:159 ...	18.69 mil	Unknown

Figure 11: Here, HyperLynx DRC displays the four EMI violations that it discovered affecting DDR2 clock signals.

When a violation is selected from the table, the location of the violation will be highlighted in the board viewer as shown in Figure 12, further actions and information can be found in the detail viewer (Figure 13):

After further examination, the status of violations can be updated, selected violations can be added to a share list that can be exported to an HTML report file with violation pictures captured, so that the report file can be shared and viewed by other team members.

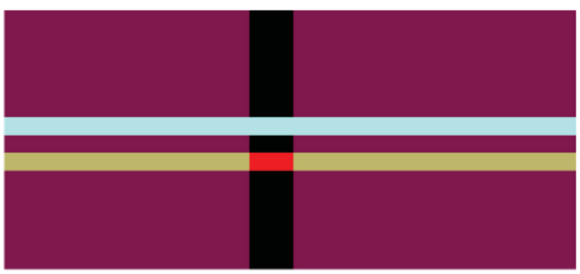


Figure 12: The violation is identified on the board viewer.

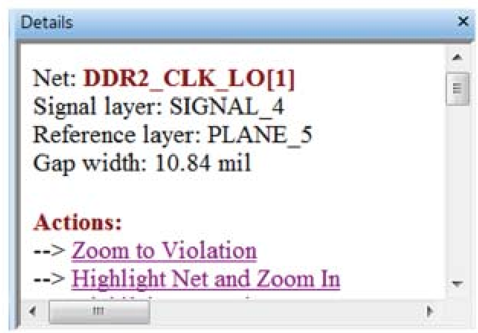


Figure 13: More details can be found in the detail viewer box.

SUMMARY

EMI issues commonly occur in modern designs, especially in high speed design field. Some of EMI issues are caused by known sources and can be avoided by a careful PCB designing process. Many issues, however, are caused by unintentional sources or human mistakes, and can be difficult to find by a manual review process. HyperLynx DRC is an industry leading solution to identify EMI issues in your layout designs.

REFERENCES

For more information about HyperLynx DRC, please visit
http://www.mentor.com/pcb/hyperlynx/electrical-rule-check.

Want to get a firsthand experience with HyperLynx DRC? Try it in the cloud
http://www.mentor.com/pcb/product-eval/hyperlynx-drc-vlab.

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