Crosstalk in differential vias with grounds

In 2002, the XFP (10-Gbit small-form-factor pluggable-module) committee, working on standards for 10-Gbps interconnections, published some terrific guidelines for high-speed differential vias (**Reference 1**). The guidelines propose surrounding your differential pair with an oval clearance and pinning the reference planes together at either end of the clearance hole with ground vias (**Figure 1**).

The guidelines assume that no long dangling via stubs connect to your signal path, meaning that either (a) your signal goes all the way from the top layer to the bottom, or (b) in a less-than-full-length transition, you have cut off the dangling ends of the via beyond the point at which signal current actually flows.

In boards as thick as 100 mils and with rise times on the order of 100 psec, the recommended structure produces a good, 100Ω transition between layers.

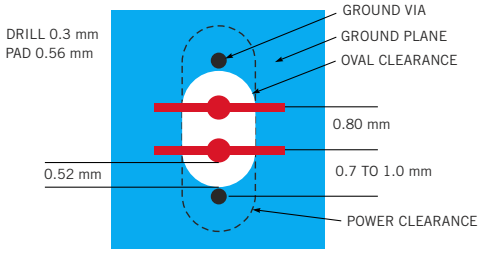

Figure 1 These proposed pc-board-layout dimensions for 10-Gbps standards help with proper performance.

TABLE 1—CROSSTALK IN MILLIVOLTS WITH GROUND VIAS

Row/Column	0	1	2	3	4	5
0	0	42	5	1	0	0
1	0	23	1	0	0	0
2	0	3	2	0	0	0
3	0	3	0	0	0	0
4	1	0	0	0	0	0
5	0	0	0	0	0	0

TABLE 2—CROSSTALK IN MILLIVOLTS WITH GROUND VIAS REMOVED

Row/Column	0	1	2	3	4	5
0	0	85	27	13	7	5
1	0	14	15	10	6	4
2	35	14	1	4	4	3
3	14	10	3	0	1	2
4	8	6	4	1	0	1
5	5	4	3	2	1	0

If you want to use this design in a dense architecture, you need to know about the crosstalk between these structures. To make the math easy, I will assume your layout provides a uniform grid of possible via locations, with a grid spacing of 0.8 mm and hole diameters of 0.3 mm. Index the grid by rows and columns.

Place one installment of the layout from **Figure 1** with the topmost via at position Row 0, Column 0. The crosstalk voltages (millivolts) into this spot from other possible via locations appear in **Table 1**. For example, placing an aggressor pair one position to the right (one column over), the crosstalk from **Table 1** in position Row 0, Column 1, reads 42 mV. I did these quasi-static calculations using MathCad.

Because the layout in **Figure 1** is four positions long, if you stay in the same column, the closest you can place the next structure (shifting straight down) is four units. The shaded areas in the **table** designate impossible positions.

This **table** assumes a 2V p-p differential signal (that is, 1V p-p on each wire), driving 100Ω differential traces with 100-psec rise and fall times. The important aspect of this specification is the total change in current per unit time (dI/dt). Crosstalk in millivolts scales in proportion to dI/dt. If you have a lower voltage, a slower rise time, or a larger trace impedance, then scale down the numbers in **Table 1** according to the extent of that difference in your architecture. As the **table** shows, crosstalk quickly plummets to small values as you separate aggressor from victim. Enforcing white space between signals is the surest way to guarantee low crosstalk.

What happens if you omit the ground vias? In that case, signals pass through the via in much the same way, but the crosstalk floats generally higher. More important, crosstalk falls off less rapidly with distance (**Table 2**). Ground vias help contain the electromagnetic fields emanating from each differential structure, arresting the spread of crosstalk.□

Reference

1. 10-Gigabit small-form-factor pluggable module, Revision 2.0, XFP multisource agreement.

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