OVERCOME THE CHALLENGES OF HIGHLY CONSTRAINED PCB DESIGNS WITH PADS®

VASILY ERSHOV, MENTOR GRAPHICS

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INTRODUCTION

Layout constraints are an essential part of a PCB design. As the technology in modern electronic devices has become more complex (e.g., increasing speed, decreasing rise time and supply voltage values), signal integrity issues have become a primary concern. For many designs, this means a large percentage of nets require PCB layout constraints to meet signal integrity requirements.

This brings two major challenges: creating a proper set of layout constraints for your design and applying those constraints during the PCB layout design process.

This paper shows how PADS helps address the challenges of highly constrained designs.

SIGNAL INTEGRITY REQUIREMENTS

The increasing use of high-speed memory interfaces (DDR2/3) and differential serial interfaces (like PCI Express, SATA, and others) in the gigahertz frequency range adds enormous complexity to PCB layout activities including placement, power plane design, and routing.

Signal integrity requirements drive the entire PCB design process. These requirements include signal quality, timing relationships between clock signals and data buses, and acceptable levels of crosstalk.

PADS provides pre-layout simulation and analysis capabilities for:

- Designing board layer stackup
- Making termination decisions
- Evaluating how net topologies and length restrictions affect signal quality
- Estimating crosstalk effects between closely placed traces.

The best time to begin simulation and analysis is before the schematic is completed, as soon as you've decided which high-speed devices will be used in your design and you've obtained and installed models for your drivers and receivers. If you prefer, you can select a net, or a group of nets, and run pre-layout simulation directly from the schematic.

After simulation and analysis you'll be able to:

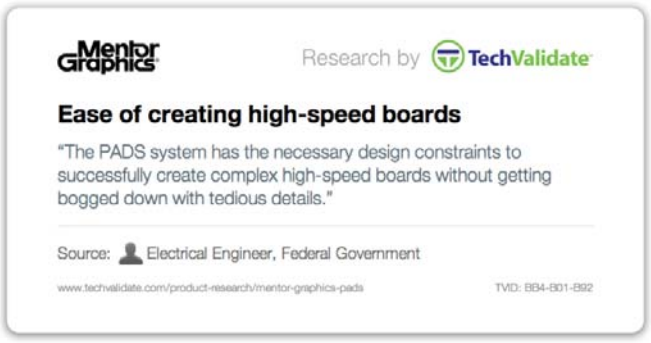
- Define parameters of the board-layer stackup
- Update the schematic with verified termination schemes
- Define and capture high-speed constraint sets that will drive physical layout activities
- Define additional spacing constraints to guarantee acceptable levels of crosstalk

Alternatively, you could use layout guidelines provided by electronic component manufacturers as a source for constraint definition. Be careful not to apply these parameters to your particular design blindly, however, as they are often too conservative, too generic, or require you to use materials and/or manufacturing technology that are too expensive.

For this reason, more and more high-speed device manufacturers recommend simulation of high-speed signals in order to refine your layout constraints.

LAYOUT CONSTRAINTS IN PADS

PADS supports an easy-to-use, powerful, and flexible layout constraint model. In this paper we'll concentrate on the constraints derived from signal integrity requirements for high-speed signals.



NET CLASSES

First you should define net classes where nets with similar SI requirements, and thus similar constraints, are grouped together. The constraints defined for a net class are automatically applied to all nets included in the net class.

For a net class you can define:

- Minimum and maximum length restrictions (the allowed length range)
- Minimum spacing between nets included in the class
- Minimum spacing to nets from other net classes, to control crosstalk levels
- Allowed trace-width range to maintain characteristic impedance; these can be layer dependent.
- Layer restrictions, to identify the layers on which nets from the class can be routed to ensure that high-speed traces are adjacent to a proper plane layer
- Via restrictions, the maximum via count per net and allowed via pad stacks
- Topology restrictions, where you can specify that nets should be routed using a daisy chain pattern and restrict the stub length

In PADS you can also redefine specific constraints to individual nets. In this case, the redefined values would take precedence over the net class values giving you maximum flexibility over the net.

TOPOLOGY CONSTRAINTS

The most common use of custom topologies and virtual pins is H-tree topology for a DDR2 memory interface. Here, PADS allows you to create custom topologies for individual nets that specify propagation paths from net source(s) to loads and terminators. For custom topology nets you can specify length restrictions for individual net branches in addition to the above-mentioned constraints. While defining a net topology, you can also use 'virtual pins' to specify branching points in a signal propagation path.

MATCHED LENGTH CONSTRAINTS

Matched propagation delay requirements are very common for high-speed busses. For example, in a DDR3 memory interface each data bus signal and corresponding data strobe signal must reach the memory module at the same time.

In physical layout this translates into matched-length constraints that are assigned to matched-length groups. PADS recognizes two types of matched-length (ML) groups: ML groups for nets and ML groups for net branches (pin pairs).

For a ML group you can specify a (length) tolerance value and min/max length restrictions. It is possible to create matched-length groups using nets from different net classes and using pin pairs from different nets.

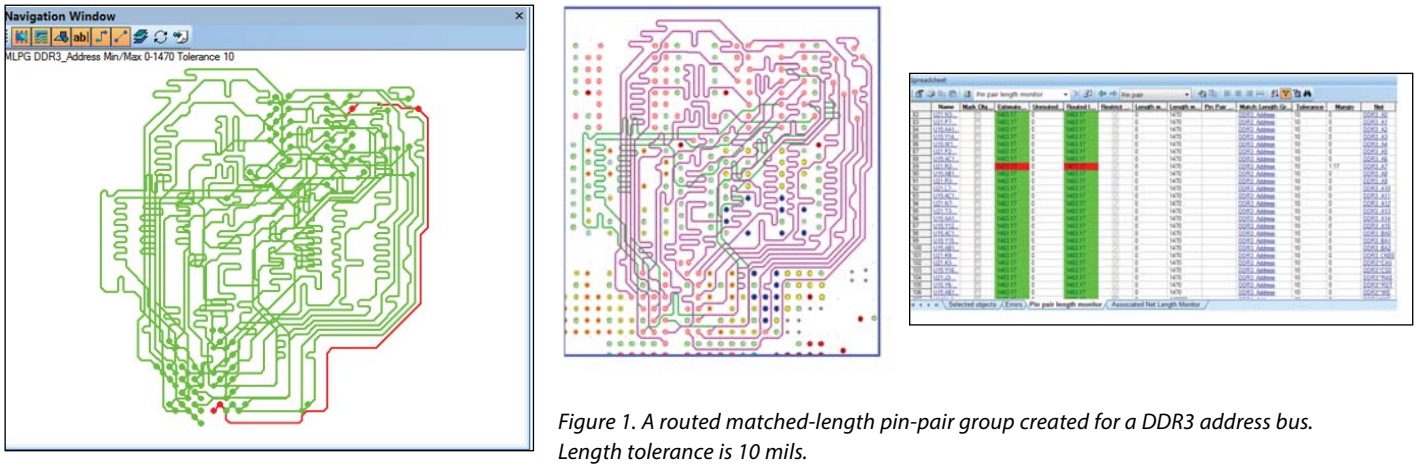


Figure 1. A routed matched-length pin-pair group created for a DDR3 address bus. Length tolerance is 10 mils.

DIFFERENTIAL PAIRS

Differential pairs can be created in either the schematic or in layout by selecting two nets, typically from the same net class. For each differential pair you specify trace width and a gap between the traces. Width and gap values can be layer dependent to maintain differential impedance for the entire propagation path of the differential signal. You can specify minimum and maximum length constraints. Typically, differential pair nets are included in some matched-length groups but in PADS you also have the option to create differential pairs from pin pairs (net branches). PADS supports same-layer differential pairs.

ASSOCIATED NETS

Associated nets are useful when you need to assign constraints to a signal-propagation path, one that runs from a driver to a receiver and that includes a series resistor (or other discrete element). For an associated net you can create minimum and maximum length constraints. Associated nets can be included in a matched-length net group. A differential pair can be created from two associated nets.

Figure 2. An example of an associated net.

PLACING COMPONENTS WITH HIGH-SPEED NETS

When placing components with high-speed nets it's important to pay attention to nets with length constraints, especially to those with maximum-length constraints. PADS makes this easy, providing real-time feedback on the status of length-constrained nets through the Net Length Monitor. This monitor greatly simplifies the need to search for component locations, thus ensuring maximum length constraints are satisfied in your design.

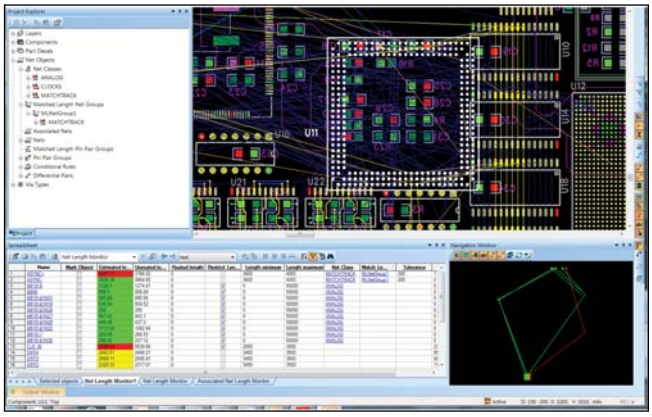
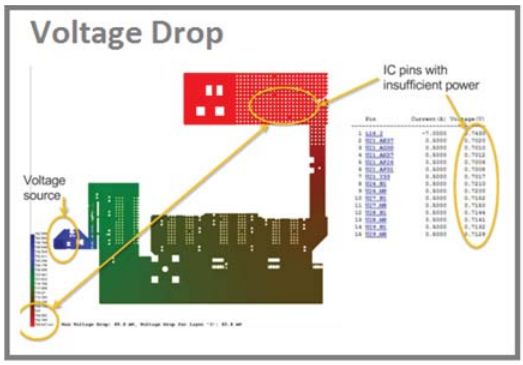


Figure 3. Color coding indicates the status of length-constrained nets during part placement. Red indicates a maximum length violation; yellow indicates nets with insufficient length, either minimum-length or matched-length violations.

DESIGNING A POWER DISTRIBUTION NETWORK

Another area of concern in high-speed layout design is power integrity or the quality of power and ground planes. Typically high-speed signals are routed on layers adjacent to solid power or ground planes. Discontinuities in planes can affect trace impedance and local voltage deviations in planes may affect the behavior of nearby high-speed devices.

Once board placement is largely defined, you can start creating shapes for power/ground planes. Use PADS optional power integrity tools to check the quality of plane areas by performing a DC Voltage Drop analysis and indentifying hot spots where current density is too high.



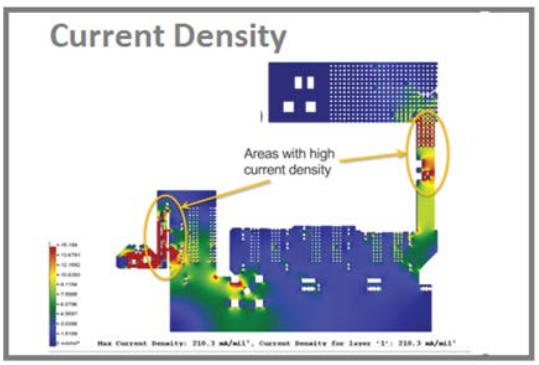


Figure 4. Power integrity capabilities provide information on voltage and current density peaks.

INTERACTIVE ROUTING OF HIGH-SPEED NETS

A common practice is to interactively route nets with high-speed constraints. As previously mentioned, the Net Length Monitor gives you unprecedented real-time assistance in checking the status of length-constrained nets and pin pairs while you're creating a trace path. It is especially useful when you're routing a differential pair or a net from a matched-length group because it shows the constraint status of all nets included in the group. PADS also supports accordion (zigzag) interactive routing, making it easy to add length to traces in order to meet matched-length requirements.

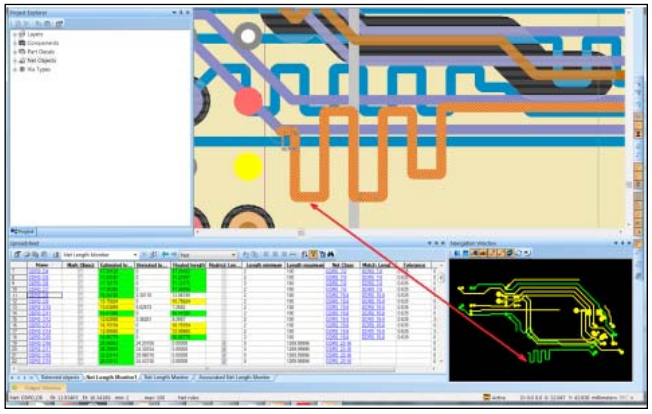


Figure 5. Interactive accordion routing of a matched-length group-member net. The constraint status of the entire group is shown in the Net Length Monitor and Navigation Window. The yellow color indicates nets that violate the matched-length constraint, set here to 0.635 mm.

AUTOMATIC ROUTING OF HIGH-SPEED NETS

Although many designers prefer to route high-speed nets interactively, proper use of autorouting can be helpful and save routing time. PADS supports automatic routing of differential pairs and automatic length tuning when you auto-route a matched-length group. The router also adheres to net topology constraints and stub length restrictions. For better automatic tuning control, you can specify accordion keepouts that specify board regions where trace length should not be added. With layer and via restrictions properly set, PADS shows good results in autorouting matched-length busses including busses with differential pairs.

Another effective use case for autorouting is to do preliminary routing of high-speed nets to assess the routability of your placement configuration. This can be done as soon as you've placed your critical high-speed components.

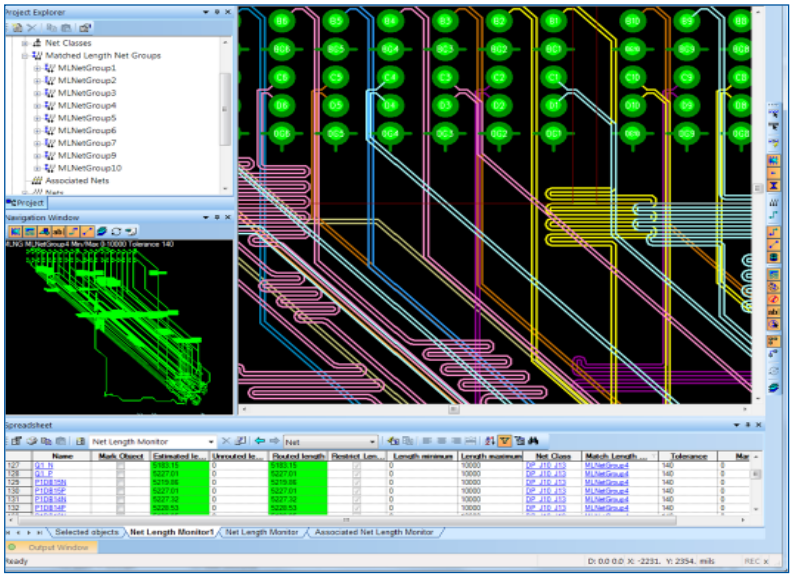


Figure 6. Fragment of an automatically routed matched-length group of differential pairs. The entire group is shown in the Navigation Window on the left. Green color coding indicates that all nets are tuned with a 140 mil tolerance.

CONSTRAINT VERIFICATION

PADS has a very convenient interface for layout constraint verification and analysis. It includes three basic things:

- An easy-to-use verification setup where you can specify a verification scheme
- Selectable, graphical error markers
- Interactive error report with sorting and filtering capabilities

Clicking on an error inside the error report gives you immediate access to the error description, the violated constraint definition, and the object(s) that created the violation.

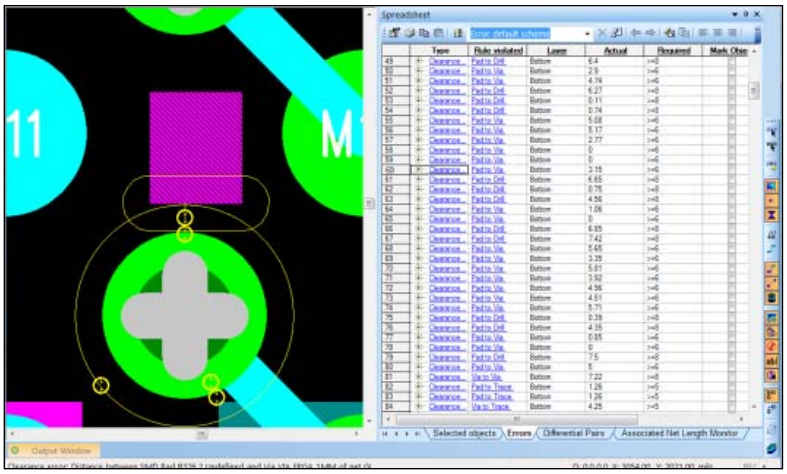


Figure 7. Error report (on the right) and main window showing error markers and details of clearance violation number 60. The error description is located at the bottom of the screen.

VIRTUAL PROTOTYPING — POST-LAYOUT VERIFICATION

Once you've finished your PCB design and verified that all layout constraints are met, you have two choices: 1) Send your design for prototype manufacturing, or 2) Go back to simulation and verify your work.

Post-layout verification is tightly integrated within the PADS flow. Simulation is based on real trace/via/plane geometries that are extracted from your layout design and it can be performed for the entire board or for selected nets.

Typical outcomes of post-layout signal-integrity verification activities are:

- Finding and fixing timing violations that can result from slight increases in signal propagation delay due to accordion routing patterns
- Finding issues with, and adjusting, terminator values

As already mentioned, you can also use PADS power-integrity capabilities to assess the quality of power and ground planes in your final design and to adjust plane shapes if necessary.

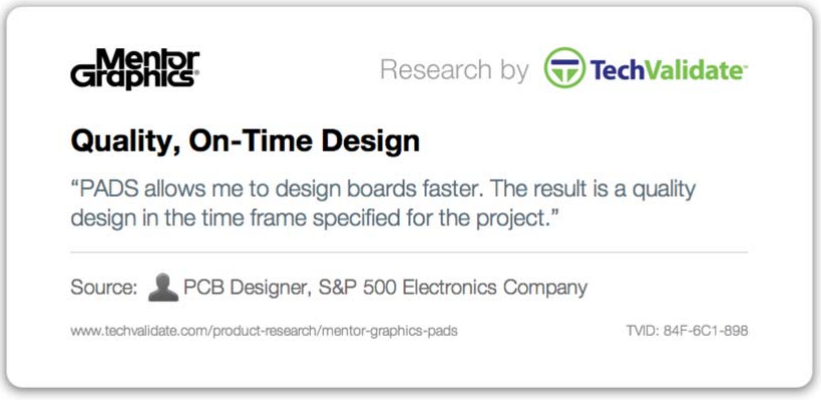
Detecting and fixing signal and power integrity issues early, without going to physical prototyping, makes time to market more predictable, increases product reliability, and results in big savings down the road.

CONCLUSION

To eliminate costly re-spins of highly constrained boards it's critical for electrical engineers and PCB designers to analyze signal integrity issues, create a reliable set of layout constraints, and manage those constraints during layout.

PADS delivers the capabilities needed to successfully design highly constrained boards:

- Pre-layout simulation and analysis tools for stackup planning, definition of termination schemes, and development of constraint sets for high-speed signals
- Powerful, easy-to-use capabilities for constraint definition and editing
- Easy, bi-directional propagation of constraint-definition data between schematic and layout
- Real-time, high-speed constraint monitoring tools for placement and interactive routing
- High-speed constraint adherence during autorouting
- Power integrity analysis that allows you to check the quality of power/ground planes
- Convenient constraint verification tools with cross-probing capabilities
- Post-layout verification of signal integrity requirements and PDN quality (virtual prototyping approach)



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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408.436.1500
Fax: 408.436.1501

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
Room 1001, 10F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886.2.87252000
Fax: 886.2.27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: 81.3.5488.3033
Fax: 81.3.5488.3004

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