PCB Design Guidelines for 0.4mm Package-On-Package (PoP) Packages, Part I

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ABSTRACT

Ball grid array (BGA) packages having 0.4mm ball pitch require careful attention to printed circuit board (PCB) design parameters to successfully yield reliable and robust assemblies; the standard rules of thumb don't apply anymore. In fact, the design guidelines for 0.4mm and 0.5mm differ primarily due to issues surrounding shorts or opens between balls under the processor.

In addition to the design rules, fine-pitch board design is a team effort. Close coordination and communication between the device supplier, the PCB designer, the board fabricator, and the assembly shop is mandatory.

The following factors have a major effect on the quality and reliability of PCB assembly: pad design, via-in-pad (VIP) guidelines, via finishing, stencil design, solder paste requirements, solder paste deposition and reflow profile. This application report provides a starting point for understanding the current set of guidelines. It is strongly recommended that you perform actual studies in conjunction with your assembly house and board supplier to optimize the process.

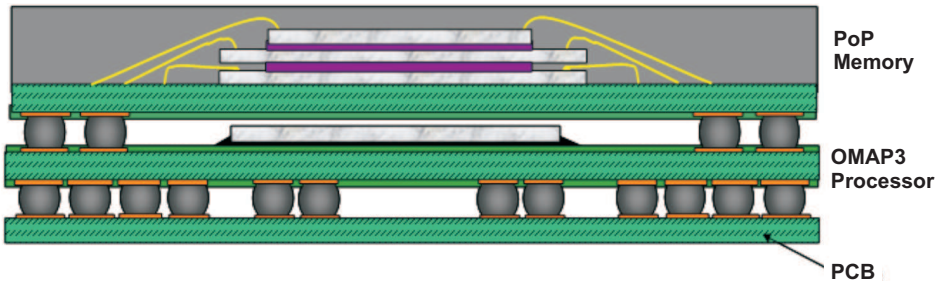

Figure 1. OMAP35x Processor (bottom device) and PoP Memory (top device) Stack Up on PCB

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1 Using This Guide

This application report focuses on circuit board design guidelines specific to the OMAP35x processor, with 0.4mm pitch on the bottom and 0.5mm pitch pads on the top for memory attachment, using package-on-package technology. Experience has shown that PCB board design is the most crucial aspect of PoP design due to the extremely small pad pitches. Also, not all assembly houses can build such small pitch assemblies or properly mount the memory on top of the processor.

Figure 2 shows a 0.4mm pitch processor and its matching memory at 0.5mm pitch.

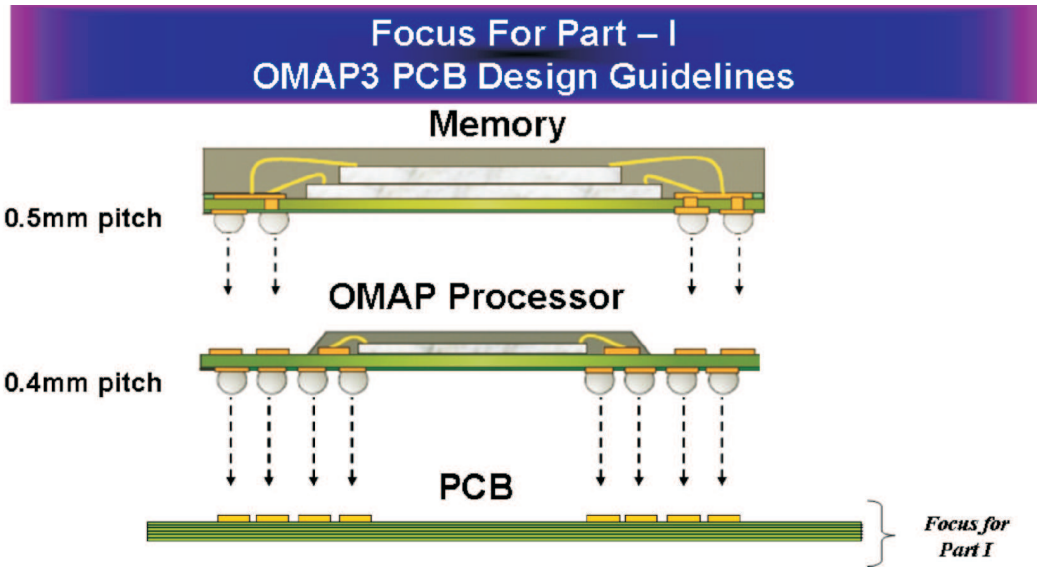

Figure 2. Part 1 - Focus for Part I - PCB Design Guidelines

Guidelines for the assembly of PCBs that use the PoP package are covered in the companion article to this document, *PCB Assembly Guidelines for 0.4mm Package-On-Package (PoP) Packages, Part II* (SPRAAV2) - which will be referred to as Part II throughout the remainder of this document. Included are assembly options and suggestions to use when qualifying and working with your assembly sites, either internal or contract.

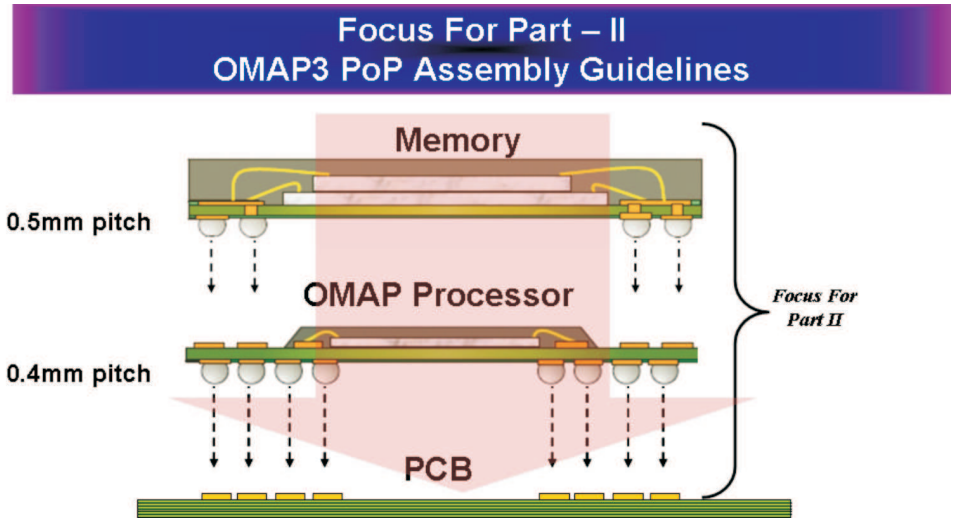

Figure 3. Focus for Part II - Assembly Guidelines

2 A Word of Caution

This section discusses the BGA package and the circuit board immediately below the BGA. The guidelines do not cover all aspects of circuit board design, nor is it a discussion on how to use your favorite CAD tool.

Design of circuit boards for fine-pitch BGA packages at 0.4mm and smaller is more of an art than a science, due to the lack of published data. In many cases, 0.4mm pitch pcb fabrication technology is considered proprietary and/or advanced and may require that a non-disclosure-agreement (NDA) be executed. Therefore, the material in this document will age and go out of date quickly as more assembly houses adopt smaller pitches and PoP assembly.

Since this is a rapidly evolving technology, spend some time reading the huge number of articles, papers and company presentations on all aspects of fine-pitch board design.

When the 0.5mm pitch design guidelines were created, it was stated that the long standing *rules* for circuit board design were no longer applicable at these small geometries and a new batch of guidelines were established. With the release of 0.4mm pitch BGA packages, the *new rules* needed to be modified. This was determined through the design and assembly of TI developed evaluation module (EVM) boards and a new circuit design called the BeagleBoard.

The BeagleBoard is referenced extensively throughout this document and Part II. Be sure to obtain the Gerber files for this board at http://beagleboard.org. The files will be an invaluable reference during the design of your board. Also be sure to check for updates to this document which will be found on the beagleboard.org website as well as all TI websites for OMAP35x, Application Notes Section.

It is strongly recommended that you plan on performing your own experimental layouts and prototype runs before committing to volume production to determine if: your suppliers can handle the device, you may have to change circuit board vendors, and/or find assembly shops with better equipment.

One important aspect of 0.4mm design is the need for close cooperation among the various entities that are involved in the board design, fabrication, and assembly.

3 A Team Sport

Successful design and assembly of complex, fine-pitch circuit boards is a *Team Sport*. The days of tossing circuit diagrams over the cubical wall to the board designer who then tosses them to the assembly shop are gone. Today's board design requires a team approach and the entire process, from component selection to assembly requires careful coordination.

The typical team is composed of four different members representing the four major steps in product fabrication: the device supplier (chips, passives, mechanical), the PCB designer, the PCB fabrication shop, and the PCB assembly shop. There may be more members or some members may do more than one job.

Each of the team members brings their own experiences and design guidelines to bear on the task. As a result, it is not uncommon to find conflicting guidelines. These conflicts must be resolved prior to the start of work. Unresolved conflicts will result in poor assembly yields at best or 100% failure at worst. Constant and frequent communication is the key to resolving conflicts and everyone must be in the loop.

Get to know your team members and be sure to have frequent meetings as the project proceeds from design through production. It will be money and time well spent.

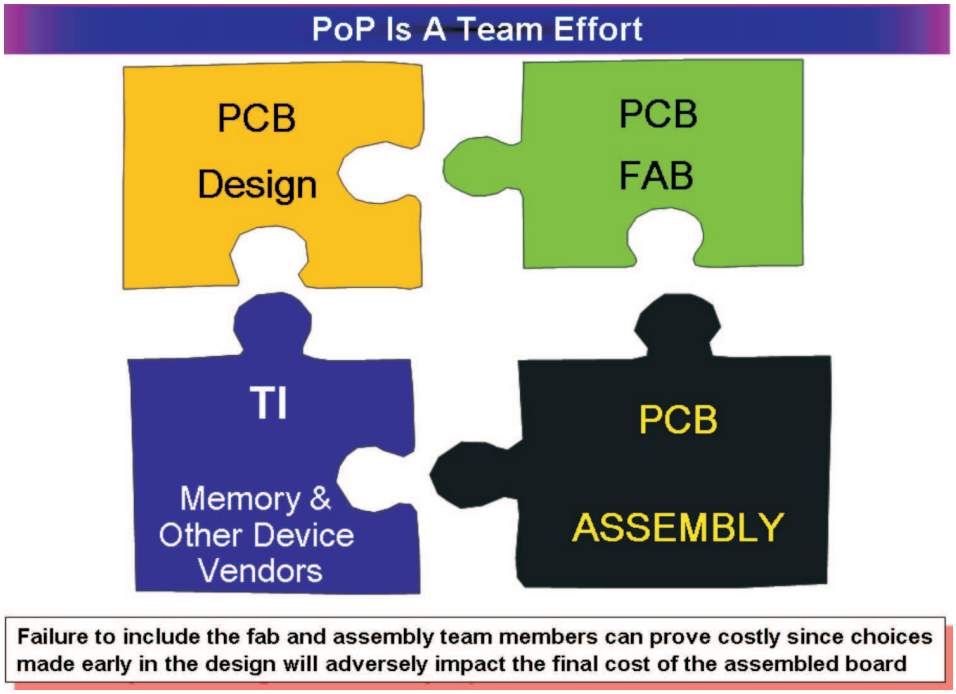

Figure 4. PoP Assembly Teamwork

4 Be Wary of Quotes

Board fabrication cost estimates vary widely. There are two key parameters that go into the overall quote cost: 1) Experience with fine pitch fabrication and 2) The quantity of boards in the production run.

Several board design and layout options are described with some options featuring a lower price. However, the lower price assumes that a relatively large number of boards are being fabricated. For smaller volumes, or for prototyping, the cost may be the same or even higher for some options.

Also, be wary of quick quotes that seem out of line. In many cases, the board vendor may be using outdated design rules causing a relatively high dollar quote for what might now be standard technology. Press them hard for ways to lower the cost. And be sure to obtain several quotes or get a second opinion.

5 Don’t Forget Your CAD Tools

Review the microvia capabilities of your CAD system. Blind microvias open up routing channels on the inner layers. Therefore, your CAD system must be capable of handling blind and buried microvias as well as through-hole vias. Your system’s features and setup dictates the difficulty or ease with which the board will route. Some of the setup parameters include via size, span, and a whole slew of clearance rules. Most CAD vendors offer specialized training on high-density interconnects and fine-pitch BGA circuit boards. Talk to them – they are part of your design team, too.

Your CAD tools can also help with the DFM checking task; take advantage of those tools. Each CAD platform is different and has different capabilities. For example, the Altium PCB design rules checking section spans more than 119 pages. Your particular CAD platform will have various checks and tests that can be performed on the finished circuit board design. Learn them and use them.

6 Metric Vs English

Here is one of the most common complaints about moving to fine-pitch BGA package design – use of the metric system. Most designers dislike this simply because all of their familiar rule-of-thumb guidelines are in the English system. Quick test, which is easier to understand 0.0033" or 83 µm? It is strongly suggested to set up your CAD grid in micrometers (µm) and do away with the four decimal places of accuracy needed to represent small features in the English system.

7 PCB Fab Limits

Most circuit board vendors publish a table that indicates various limits for drills, trace widths, thicknesses and so on. In many cases, there are different limits depending on the most important characteristic for the board. What this means is that there are tradeoffs and options for the designer to consider. Always consult with your circuit board vendor for their limits and capabilities and remember that as you approach the limit of the vendor's equipment, yields go way down and costs go way up. Let's look at one vendor's (vendor X) technology and capabilities:

Standard Technology— Usually means this is the middle of the vendor's capability and pricing. The technology does not push the limits of the vendor's equipment. For example, vendor X shows that a *standard* minimum trace width and clearance are 3 mils with 4 mil vias and 10 mil pads.

High Yield Technology— Loosens up the specifications to provide more clearance and wider traces resulting in lower cost per unit board and higher yields. For example, the same vendor X lists a minimum trace width and minimum clearance of 4 mils with 4 mil vias and 10 mil pads for high yield boards. However, a hi-yield board may be larger and have more layers.

Engineering Development Technology— Really pushes the vendor's capabilities. It is at the limits of the vendor's equipment. For example, vendor X lists a minimum trace width and minimum clearance of 2.5 mils with 3 mil vias and 9 mil pads.

8 Routing and Layer Stackup

One huge benefit of PoP is the elimination of the high-speed, balanced transmission lines between the processor and memory. The external memory's data and control lines no longer have to be routed out from under the processor. This is a huge savings in both time and the number of layers. This also impacts your pad and layer stackup decisions. OEMs have quickly adopted PoP as their processor/memory package of choice for these reasons.

It is possible to use a 6-layer stack and route all of the connections without requiring buried vias. For the BeagleBoard, relatively common VIP technology was used. There are several suitable layer setups; the one described below was used in the BeagleBoard. This format is also popular because it allows sensitive clock signals or relatively high-speed lines to be routed between power planes.

Layer 1	Signal (Top Copper)
Layer 2	Ground
Layer 3	Signal
Layer 4	Signal
Layer 5	Power
Layer 6	Signal (Bottom Copper)

Package footprints and pad stacks are the next important item to consider. Proper definitions and strict adherence to clearance plays a key role in the development of high yield PoP designs.

9 OMAP35x 0.4mm Pitch

Familiarity with the basic dimensions of the OMAP35x processor is helpful. This section discusses the key parameters.

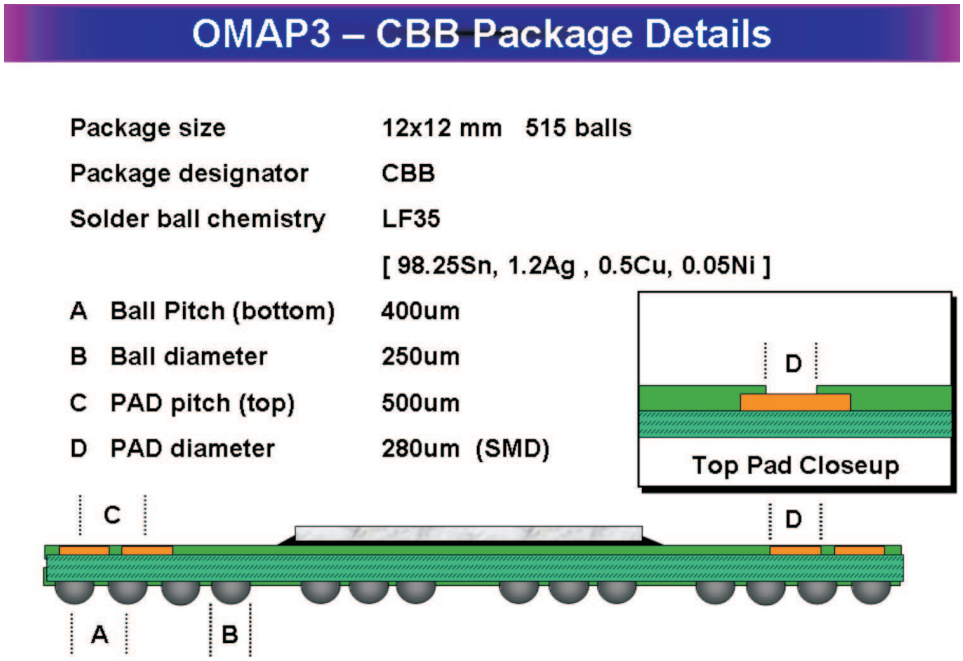

Figure 5. OMAP35x - CBB Package Specification Details

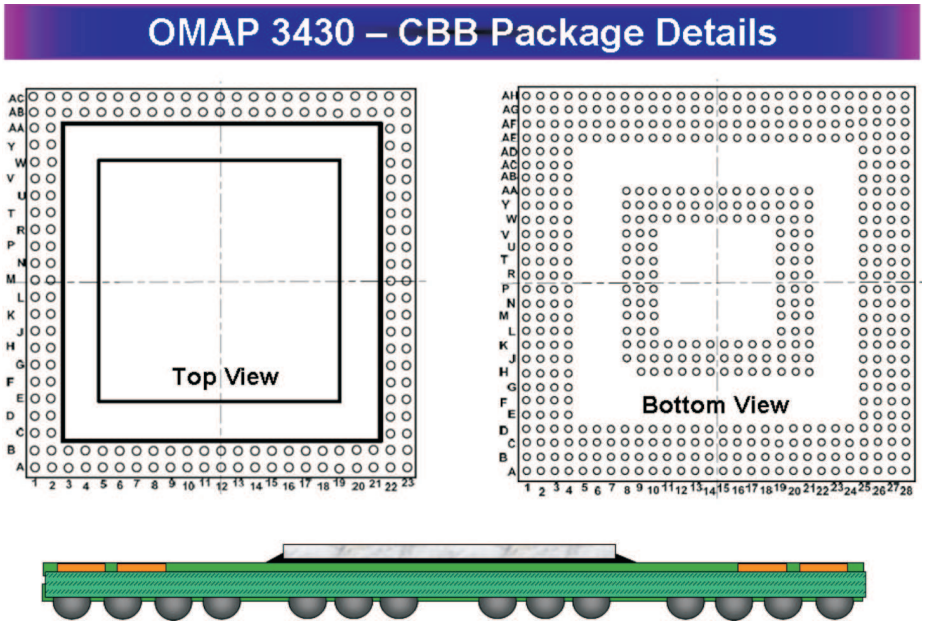

Figure 6. OMAP35x - CBB Package

10 Pad Type

It is important to understand the pros, cons, and unknowns concerning the two most common types of solder pads. Figure 7 shows the solder-mask-defined (SMD) and non-solder-mask-defined (NSMD) pads.

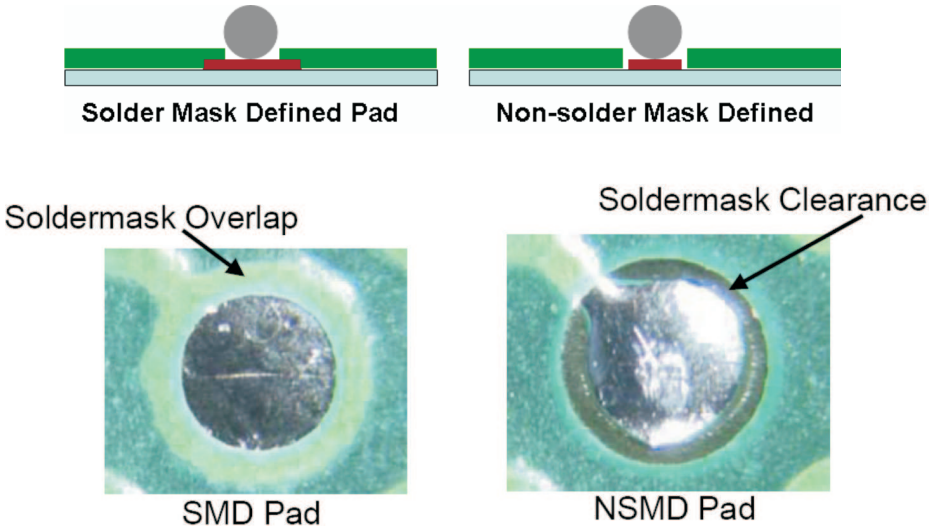

Figure 7. Solder-Mask-Defined (SMD) and Non-Solder-Mask-Defined (NSMD) Pads

Industry reliability studies have revealed that NSMD-type pads are highly recommended for most 0.5mm pitch BGA applications. However, there is a problem with this approach at 0.4mm pitch.

Real-world assembly experiments with the BeagleBoard and the OMAP35x EVM revealed a tendency for solder bridging between pads when NSMD were used. There was insufficient solder mask webbing between the pads to ward off bridging. Therefore, a SMD design was used which resulted in much better assembly yields with no solder bridging.

Talk to your board fabricator and your board assembly house and learn of their experiences and preferences before deciding which type of pad design you will use. Be prepared to change your ideas about pad definitions as your experience grows with 0.4mm pitch parts.

Note: Based on experience with both the BeagleBoard and the OMAP35x EVM, the use of solder-mask-defined pads is recommended.

11 PCB Pad Dimensions for 0.4mm BGA Package

Through several meetings with both board fabricators and board assembly houses, the following recommendation has been created for the circuit board BGA footprint for the OMAP35x having 0.4mm or 400 µm, pitch solder balls. Figure 8 shows the top layer with vias down to layer 2.

At the 0.4mm pitch, there is insufficient space between pads to allow a 3mil trace to run between pads without incurring solder bridging. Therefore, except for the outside perimeter balls, all connections are routed to the lower layers through VIP technology. With this technology, only six layers were needed for the BeagleBoard.

For the BeagleBoard design, the desired finished pad size is equal to the solder ball diameter. Since no traces run between the pads, the copper pad is enlarged to 280 µm (11mils). The solder mask opening is set to 254 µm (10 mils).

With this arrangement, there is plenty of solder webbing between pads which helps prevent adjacent ball solder bridging. For more information regarding additional parameters that impact the assembly of this package, see *PCB Assembly Guidelines for 0.4mm Package-On-Package (PoP) Packages, Part II* (SPRAAV2).

Pad Type	Solder Mask Defined	
Pad Pitch	A	400 µm (0.4mm)
Mask Opening	B	254 µm (10mils)
Pad Size	C	280 µm (11mils)
Mask Shape	Round	
Mask Web	D	150 µm
Pad to Pad Clearance	E	120 µm
Trace Allowed Between	No	

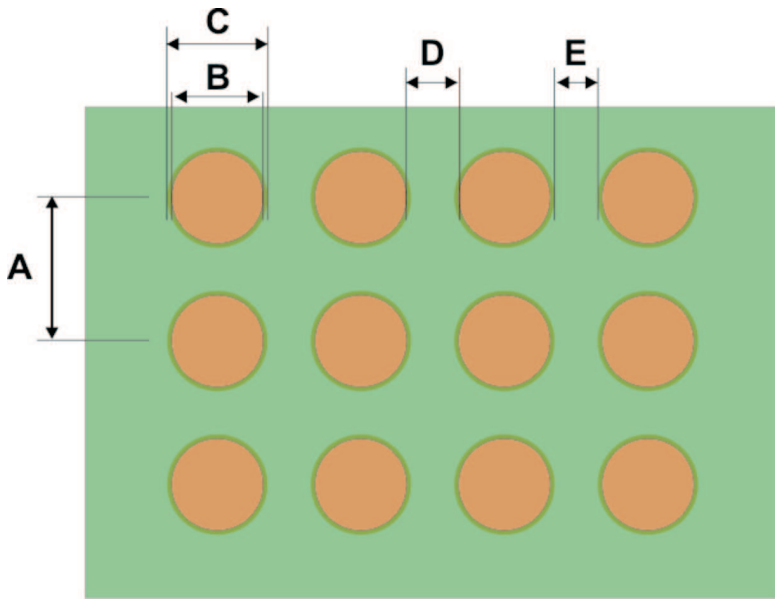

Figure 8. Recommendations for 0.4mm Pitch Packages - Top Layer

12 Multiple BGA Packages

When BGA packages are placed on the top and bottom layers, do not place one BGA package directly underneath another BGA package. The temperature cycle board level reliability degrades if overlap of package footprint occurs.

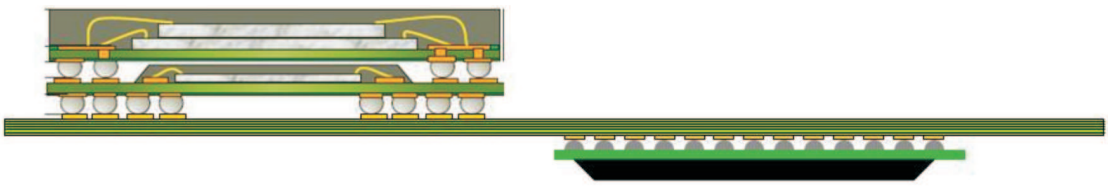

Figure 9. Multiple BGA Pacbages on PCB Should Be Off-Set

Several studies, including the one referenced here, show that temperature cycle board-level-reliability (BLR) performance degrades if there is an overlap of package footprints. A small BGA opposite a large BGA or QFP, with its footprint within the unpopulated I/O shadow of the larger package, has temperature cycle performance similar to that of a single-side board assembly.

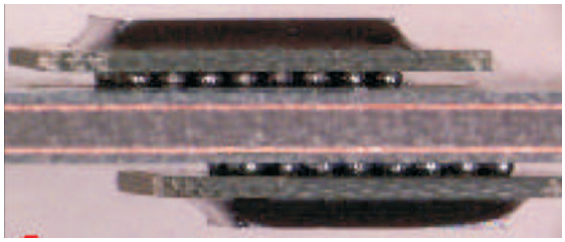

Figure 10. Multiple BGA Packages on PCB Should not Be Overlapped

For additional information on this concept, please see section 5.4, Single-Sided Soldering and Double-Sided Soldering, of NEC's, *Semicondutor Device Mount Manual*, http://www.necel.com/pkg/en/mount/.

13 Etch Traps and Heat Sinks

The challenge with fine pitch board design is to insure that traces and vias don't pull heat away from the solder ball pad. This means that common sense routing circuit board guidelines are still useable. Also beware of etch traps.

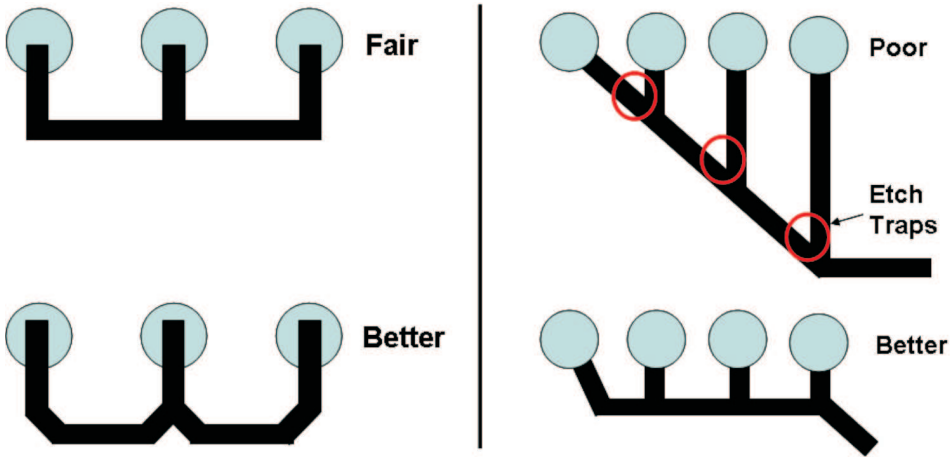

Figure 11. Common Sense Routing Circuit Board Guidelines

Small BGA pads don't have much solder and depend on uniform heating for a good joint. Here are some additional tips to insure that traces and vias don't serve as heatsinks.

- Keep the trace smaller than the pad or via.
- Do not gang up pads with a copper pour such as around a ground plane.
- Use individual traces to interconnect the pads.

The OMAP35x processors are relatively low power devices so the smaller traces are appropriate.

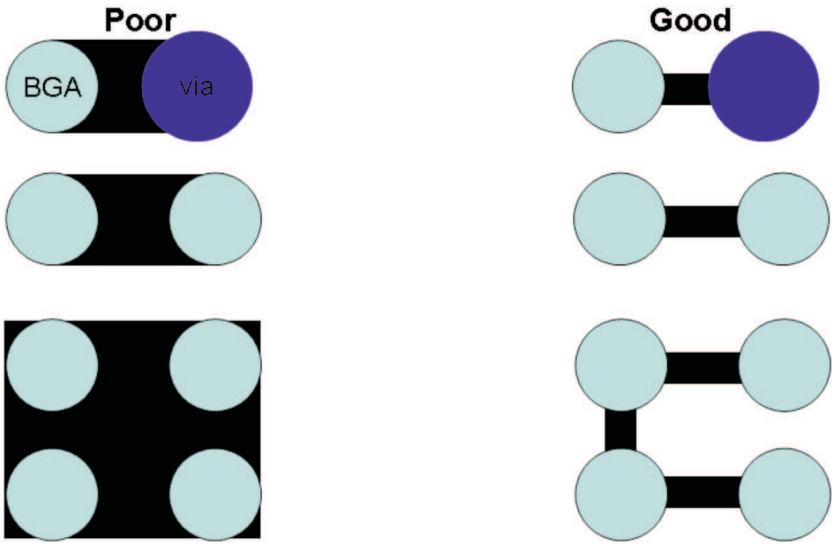

Figure 12. Common Sense Routing Circuit Board Guidelines

14 Vias and VIP

One of the greatest benefits from package-on-package technology is the elimination of the complex, expensive, and challenging task of routing high-speed memory lines from under the processor out to memory. Instead, the memory sits on top of the processor and the connections are automatically made during assembly.

Except for the outer perimeter balls, routing for the BeagleBoard is done with VIP technology. Although this was once a feared and expensive technology, recent studies and advances have eliminated nearly all of the problems. In fact, VIP is becoming the dominate technology for high density boards and is providing a cost effective alternative to conventional and offset vias.

The VIP methodology places the via directly under the device's balls. However, this requires another step to seal the via to prevent blowouts and voids. For the BeagleBoard, non-conductive, epoxy-filled vias were used.

The BeagleBoard uses only through-hole vias from top to bottom, blind vias from top to layer 2, and stacked vias from top layer to layer 3. It does not use buried vias. All vias are laser drilled.

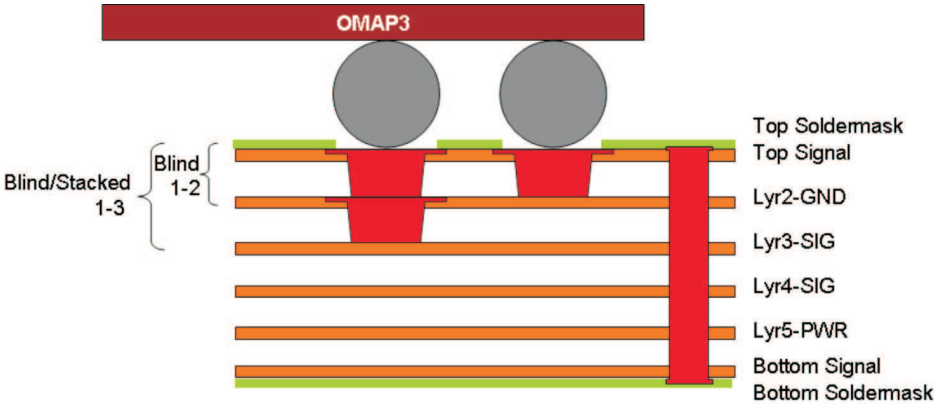

Figure 13. BeagleBoard Via Example

15 Laser Blind Vias

The BeagleBoard uses blind vias that are 6mil in diameter and are laser drilled.

Laser vias are typically drilled through reinforced FR-4 material that is 0.002” thick or less. There is standard FR-4 or laser drillable FR-4 that uses a more uniform glass weave. The *LD* glass has a cost adder to it, but produces a smoother wall hole surface which makes filling and capping easier.

The minimum average copper plating thickness for a laser blind via hole should be specified as 0.0005” or as *In accordance with IPC-6012A, class 2*.

16 Filled Vias

After drilling, and depending on the board fabricator preferences, the BeagleBoard vias were filled with non-conductive epoxy. It was used because it has a better match to the thermal expansion properties of the board material.

Once the vias are filled, cured, and planarized, they are then plated. This yields a flat copper plated cap over the vias which facilitates component attachment. The VIP technology provides two primary benefits: higher component density and improved routing.

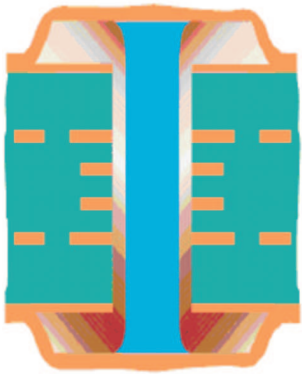

Figure 14. Plated, Filled and Capped BGA Pad

All vias must be capped or filled to prevent voids and out gassing. The images inFigure 15 show the effect of an uncapped via. The voids and damage occurs during reflow. The right picture is a failure caused by the excessive package movement during reflow, caused by out gassing.

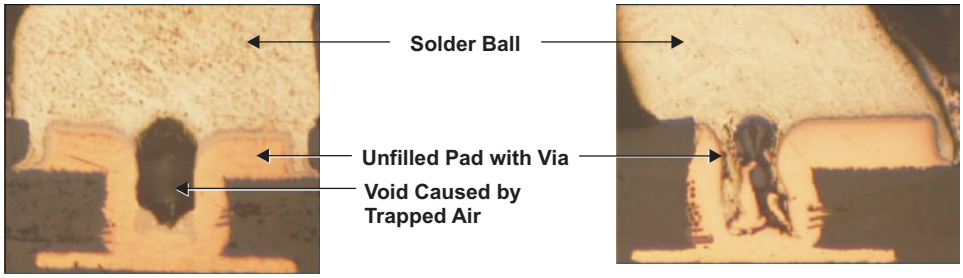

Figure 15. Effect af an Uncapped Via

It is strongly recommended that all vias be tented, filled and/or capped, especially under BGA packages.

Be sure to consult with your board fabricator prior to specifying via fill to establish their manufacturing requirements. Also, make sure your CAD system provides the required design files and the needed documentation. In some cases, additional files may be required.

Tom Hausherr, from PCLibraries (www.pcblibraries.com), has a very good presentation covering various types of vias and via coverings. His presentation, *Metric Pitch BGA and Micro BGA Routing Solutions*, can be found on their website. Please read that material since this application report only highlights the three most commonly used types of vias and via coverings.

17 Know Your Tools

Beware that your CAD program must be setup correctly to define the appropriate pad and via stacks to support different types of vias. The additional process steps may require additional gerber files.

Your CAD manual and board fabricator will be your best friends as your tools are setup, so plan to learn and use all available supporting documentation as well as your extended team members.

Here are some precautions and checks you might consider after your board has been sent through the autorouter:

- Too many vias – Power routing without constraints can result in some traces becoming overly long with too many vias. This can adversely impact the impedance of the subsequent trace, resulting in excessive noise pickup.
- Insufficient trace width – Be sure that power traces have adequate width. In the BeagleBoard example, notice the use of wide traces for all power nets, especially on the inner layers. Inner layer power traces are 10 mils on the BeagleBoard.
- Use the power planes for routing – Although not always mentioned, the power planes can be used for routing. This can be seen on the ground layer of the BeagleBoard.
- Add additional planes on other layers – The BeagleBoard has low routing density on several planes allowing for copper pours for other power planes on these layers.
- Use multiple power planes on the *power plane*. Three different power rails are routed on the power plane layer and each one is an individual copper pour. Each power rail has its own set of bypass capacitors even though they share the same layer.

Note: It is strongly recommended that all vias be covered, especially under BGA packages. In addition, the board vendor should be consulted prior to specifying via fill to establish their manufacturing requirements, required design files, and the needed documentation.

18 BeagleBoard

The BeagleBoard is an open-source hardware platform based on the Texas Instruments' OMAP35x. The platform is a complete single board computer suitable for software development and debug. Use the following link for additional information, including the hardware schematics and Gerber files: http://beagleboard.org. Also consider subscribing to the BeagleBoard RSS feed.

Figure 16. BeagleBoard.org

The BeagleBoard is used to illustrate the use of the 0.4mm PCB design guidelines and the assembly guidelines discussed in *PCB Assembly Guidelines for 0.4mm Package-On-Package (PoP) Packages, Part II* (SPRAAV2). Figure 17 shows the board layout. Subsequent sections discuss each layer as it is used to route the BeagleBoard with special attention given to the area under the OMAP35x device. The overall board dimensions are 3 inches by 3.1 inches and it is a 6 layer board.

Copies of the Gerber files and schematics from the BeagleBoard website provide an example of a real layout that has gone to production.

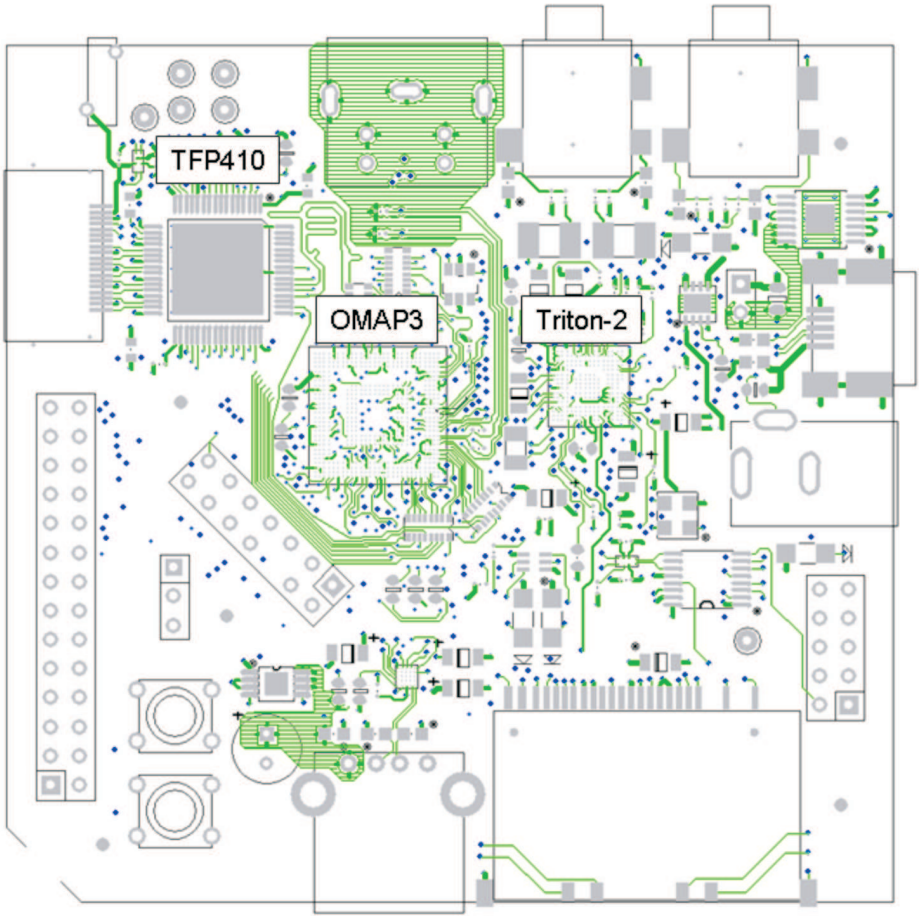

Figure 17. Top Layer BeagleBoard Layout

19 BeagleBoard Views

Each BeagleBoard layer is shown, with the image centered on the area underneath the OMAP35x.

The layer images are from the Allegro viewer with the appropriate pins, vias, and etch turned on for each layer. Except for the overall board picture shown in Figure 17, the area underneath the BGA package is the focal point. The image is always shown from the top.

The color code used is green for etch, blue for vias, gray for component pads, and blue-gray for the VIP.

The solid dark square is the OMAP35x outline and is retained for each subsequent layer.

Figure 18 is the top layer with the various pads and trace widths annotated.

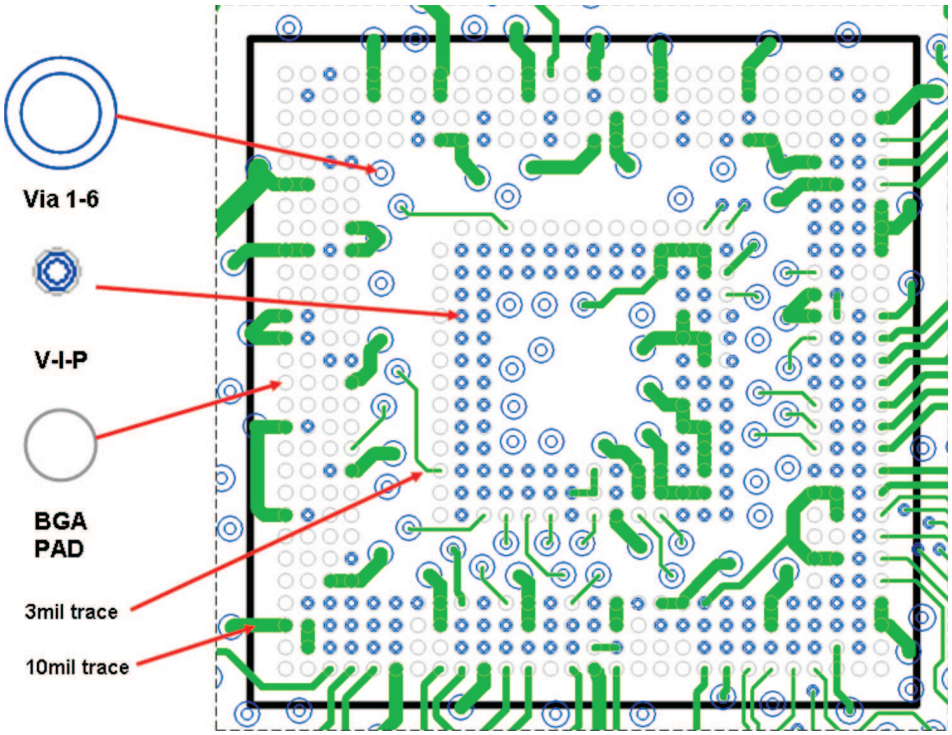

Figure 18. BeagleBoard Top Layer Underneath the OMAP35x

19.1 Top Layer – Signal - Area Underneath the OMAP35x

Things to notice on this layer:

- No traces between BGA pads
- The thin traces are all 3mil width
- Thick traces are 10mils
- The VIP are blind and go from 1-2 or 1-3 only. There are no buried vias.

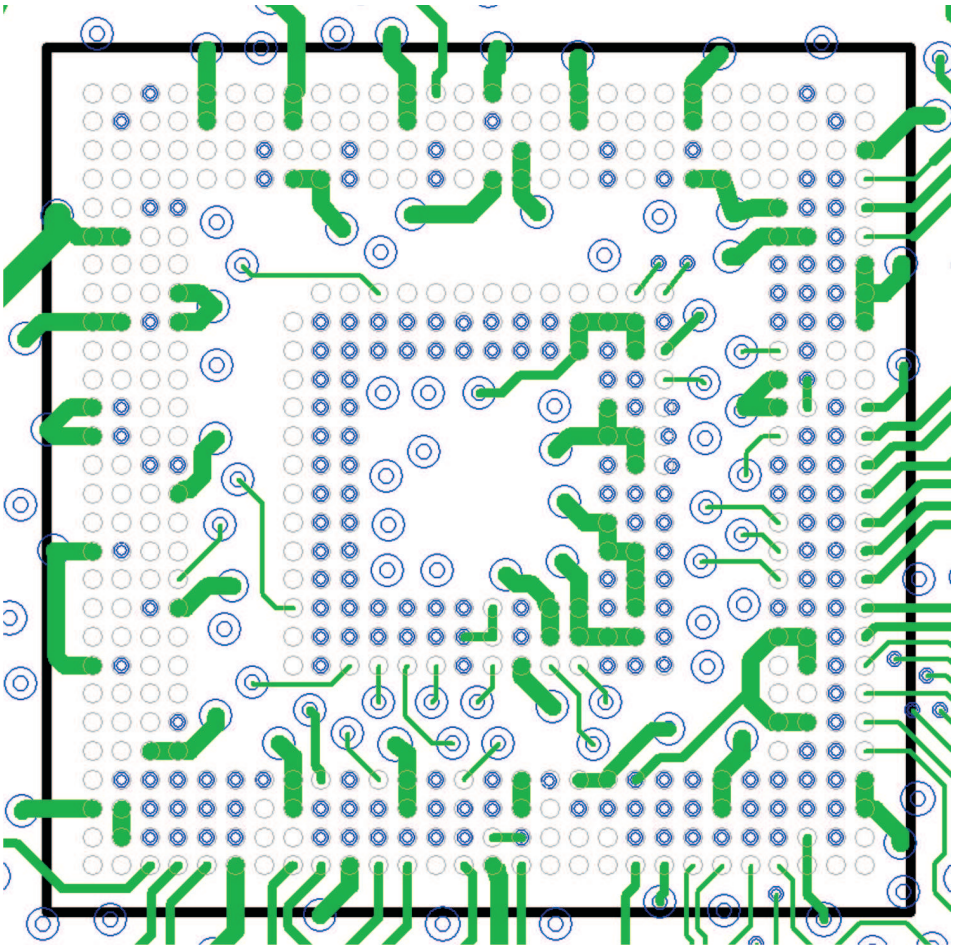

Figure 19. Close-Up of BeagleBoard Layer 1 - Top Side

19.2 Layer 2 – Ground

The ground plane is the shaded green area.

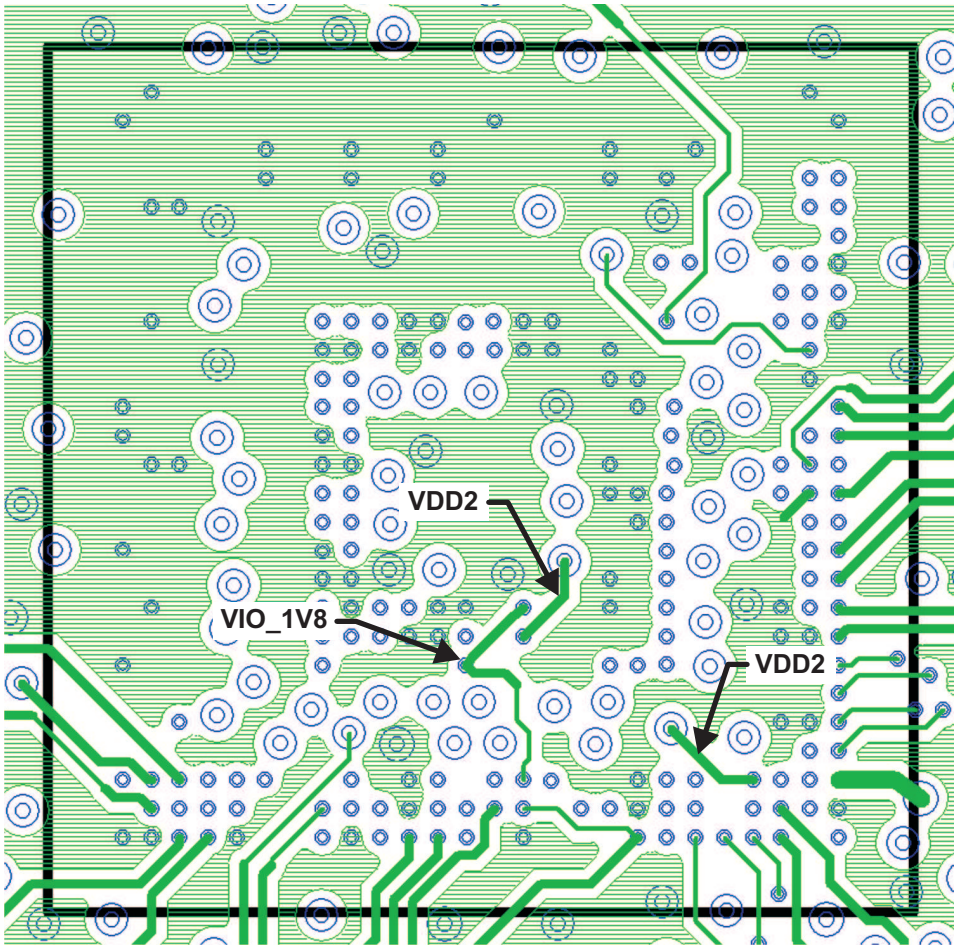

Figure 20. Close-Up of BeagleBoard Layer 2 - Ground Plane

19.3 Layer 3 – Signal

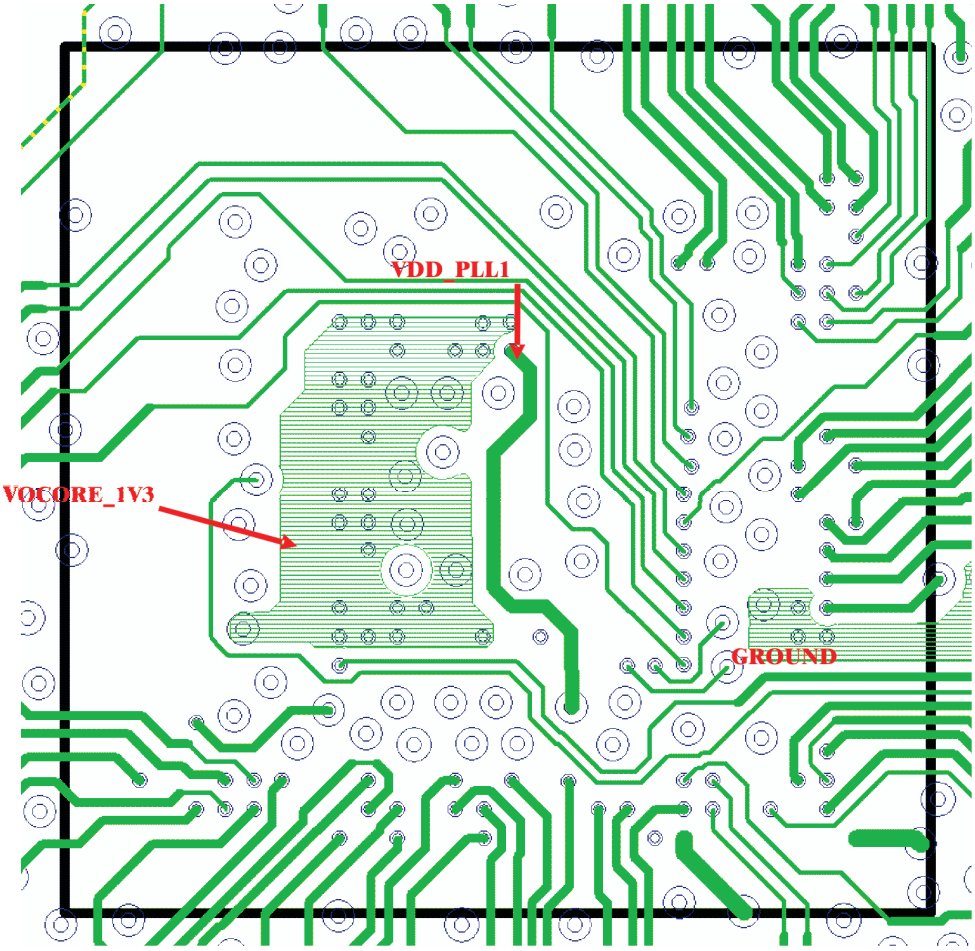

Figure 21. Close-Up of BeagleBoard Layer 3 - Internal Signal

19.4 Layer 4 – Signal

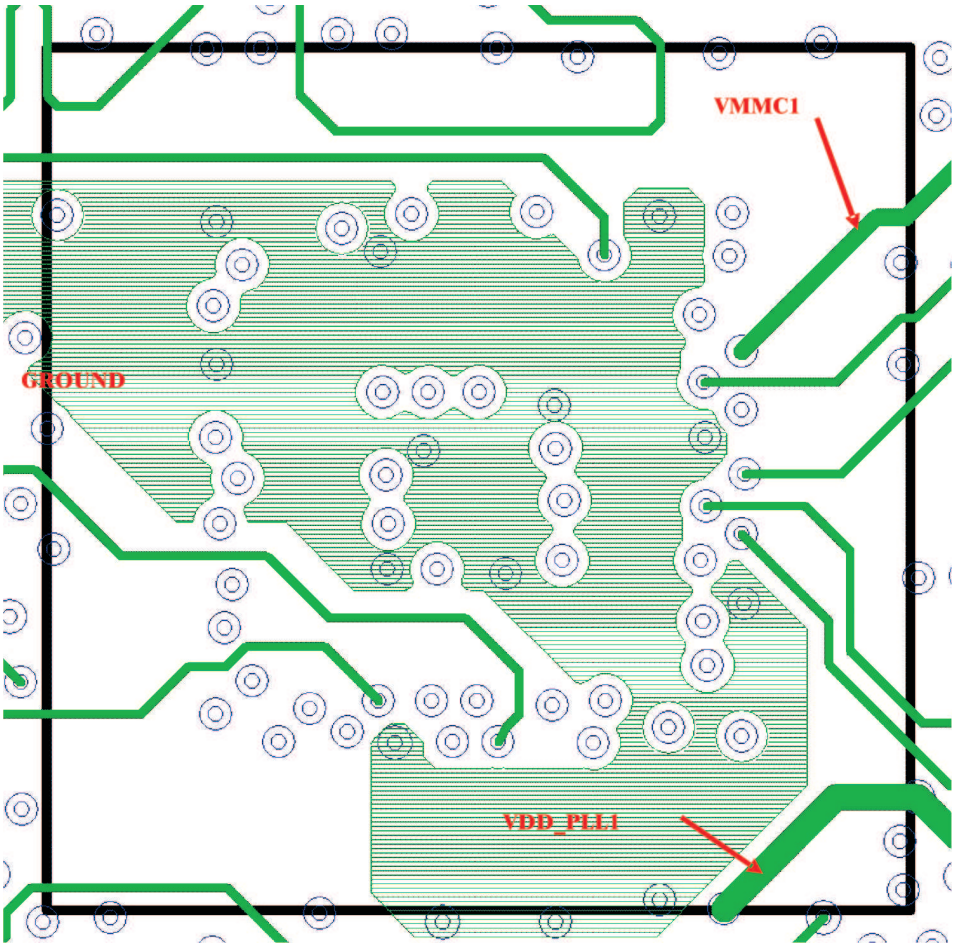

Figure 22. Close-Up of BeagleBoard Layer 4 - Internal Signal

19.5 Layer 5 – Power (V_{DD2})

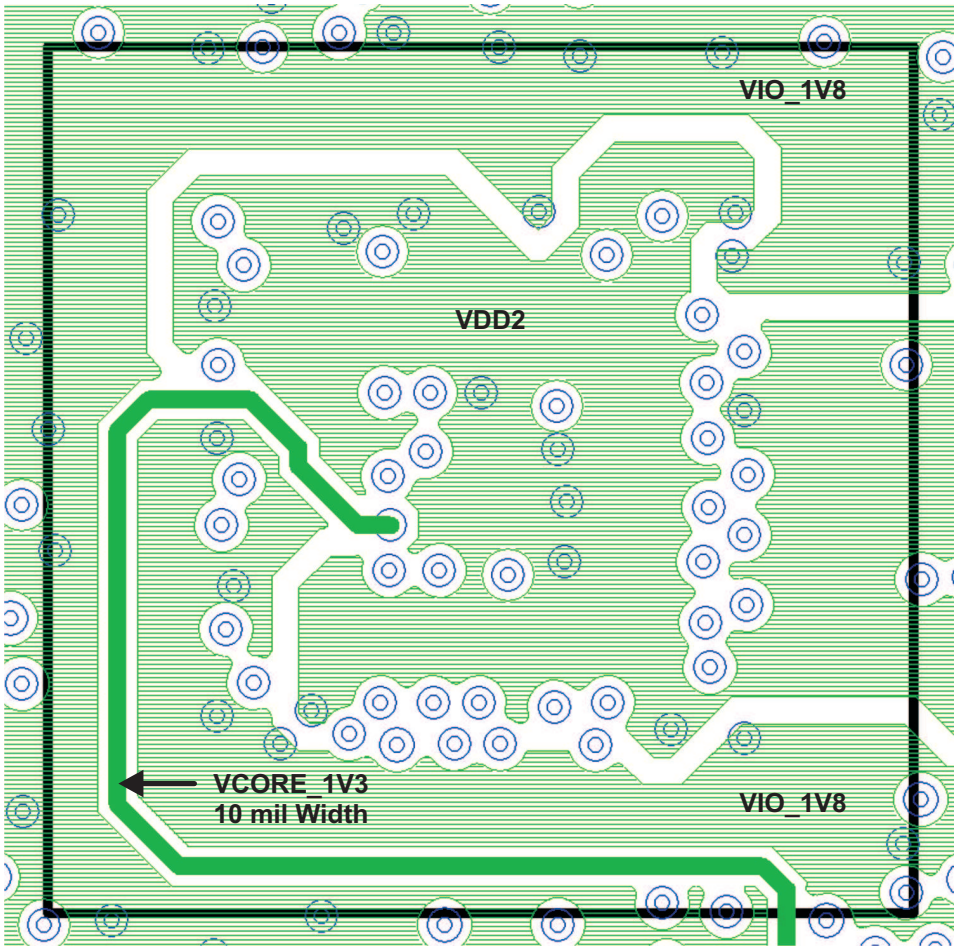

Figure 23. Close-Up of BeagleBoard Layer 5 - Power Plane

19.6 Layer 6 – Signal – Bottom Copper – Bottom Component Outlines

The bottom layer view has been enlarged in scope to show more of the board and to show most of the OMA35xx supply bypass capacitors (shown in orange.) The two small black colored items are resistors.

The X7R bypass capacitors are the smaller 0402 packages and are all rated at 0.1µF/10 V. The three larger capacitors are all 1µF and are used to bypass the OMAP3 processor's internally derived voltages and references.

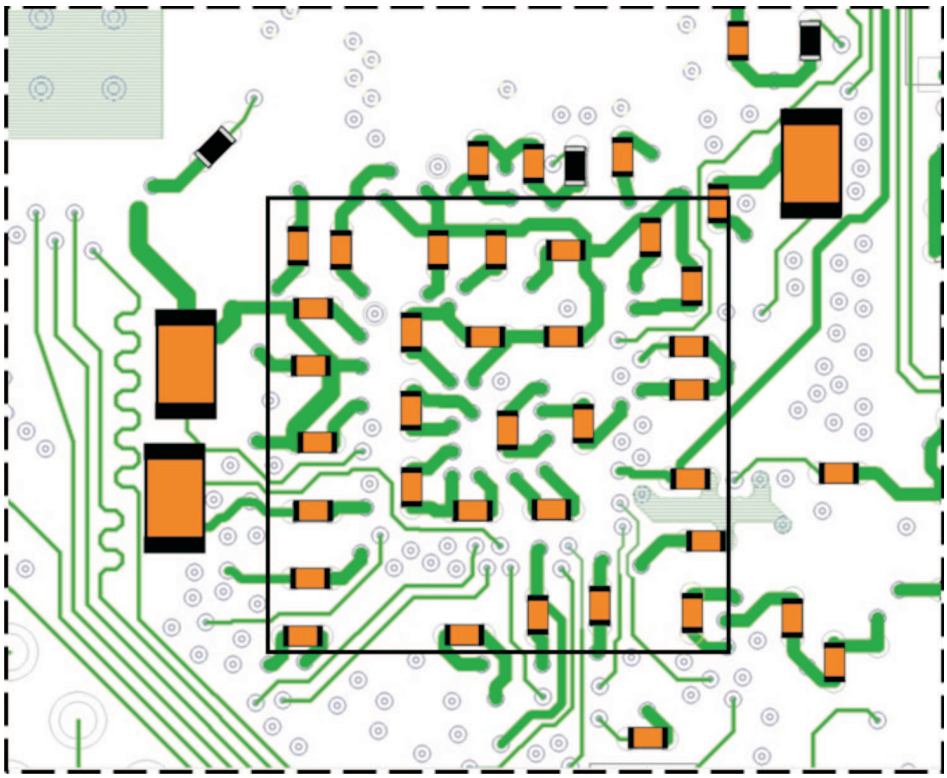

Figure 24. Close-Up of BeagleBoard Layer 6 - Bottom Side

20 OMAP35x Decoupling

There are a lot of power pins on the OMAP35x. Decoupling capacitors are required and must be placed as close to the ball connection as possible. When selecting a power and ground, choose the ground closest to the power pin for each decoupling capacitor. A single decoupling capacitor can serve up to three balls.

The BeagleBoard has almost all of its decoupling capacitors mounted on the bottom side of the board. Each capacitor connects with as many as three processor power pins through both blind vias to the power plane and thru-hole vias from top to bottom.

Figure 25 shows how the OMAP335xx's V_{DD2} rail is decoupled on the BeagleBoard. The processor outline is shown as a dotted line and the PCB design is viewed from the top side. The schematic for this area is shown to the right and the reference designators are shown on the appropriate capacitors.

The bypass capacitors are 0.1µF, 10 V, X7R type and are in a 0402 package.

There are additional voltage rails that use the remaining capacitors. A careful study of the BeagleBoard Gerbers and schematics will help you as your design is realized and illustrate what worked for this board.

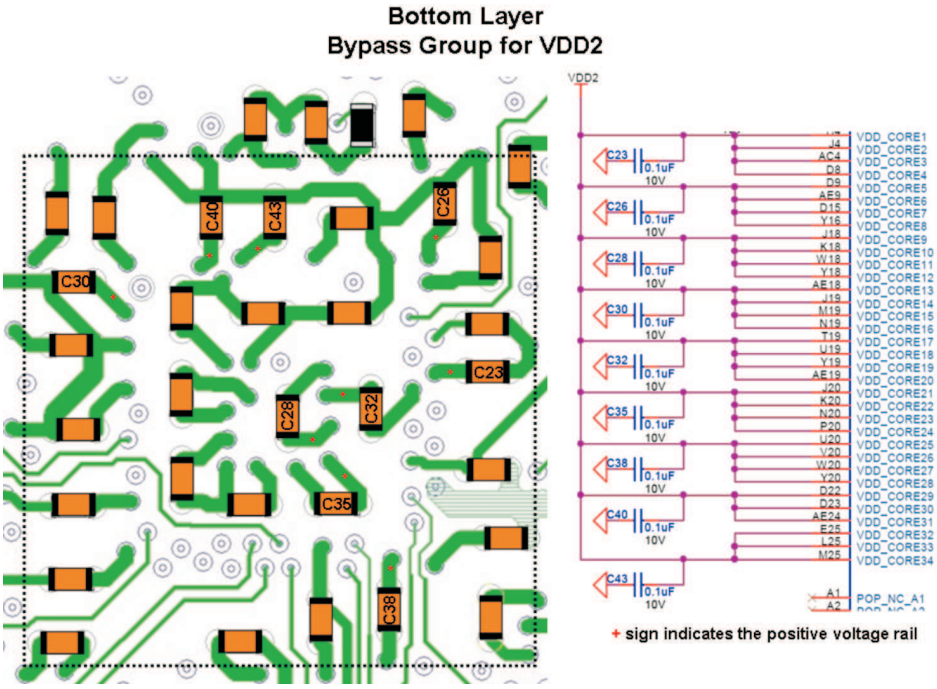

Figure 25. BeagleBoard Bypass Group for V_{DD2}

21 PCB Finishes for HDI

A surface finish provides a coating over the outer layer copper that prevents oxidation and provides an electrically conductive surface. This surface has two generic functional requirements: to provide a solderable surface for connecting components with solder and to attach a component without soldering, such as a wire bond or press-fit connector.

Organic Solderability Preservative (OSP)— This process coats a very thin coating of an organic material that inhibits copper oxidation. It is so thin that it is nearly impossible to see and measure. The organic material is removed by the assembly flux. Boards that have been OSP coated will have bright copper pad coloration. The most prevalent is ENTEK CU-106A. This is used for assemblies that will go through multiple assembly operations. PCB's that have multiple surface finishes can use the CU-106A(X) finish.

Immersion Tin (ImSn)— This process coats a thin layer of tin directly on top of the copper surface. The tin produces an extremely flat surface for mounting of surface mount components with ultra fine-pitch devices. This also provides a thicker, uniform surface that provides lubrication for press-fit pins.

Immersion Silver (ImAg)— This process plates a thin layer of silver directly on top of the copper surface. As with the other immersion surface finishes, the finished product produces a very flat surface; it is ideal for fine pitch SMD arrays. This surface finish has the ability to maintain high solderability after multiple heat cycles. This can also be used as an aluminum wire bondable surface. It is compatible with no-clean assembly processes. This is becoming popular as a HASL replacement for lead-free soldering applications. This surface finish yields a dull tarnished looking surface. There is significant industry data showing that the dullness does not affect solderability or reliability.

Other Finishes— Other finishes include hot-air solder leveling and immersion nickel-gold (ImNiAu). Table 1, from a 2003 SMTA paper, summarizes the attributes of each PCB finish.

Table 1. 2003 SMTA Paper Summary of Attributes of Each PCB Finish

Parameter	HASL	OSP	ENIG	ImAg	ImSn
Standard solder joints are predictable	P	P	P	P	P
BGA solder joints are predictable	P	P	M	P	P
Solderability shelf life is one year	P	M	P	M	M
Soldermask compatibility	P	P	M	P	M
Via plugging is safe and reliable	P	M	P	M	M
Improves overall via reliability	M	----	P	----	----
Flat surface benefits assembly	M	P	P	P	P
Conductive contact surface	P	M	P	P	P
Solderable over four heating cycles	P	P	M	P	P
Thickness variation is minimal	M	P	P	P	P
Coating is environment friendly	M	P	P	P	P
Tin whiskers are not a problem	P	P	P	P	M
P = plus, M = minus, N = neutral	8P	8P	9P	9P	7P

22 Real World Second Opinion

Our first OMAP35x EVM circuit board was designed prior to the release of these guidelines and was submitted to an assembly house. Elcotech, where they performed a DFM analysis on the gerber files. Below are their comments and Figure 26 shows this first pass at the EVM layout.

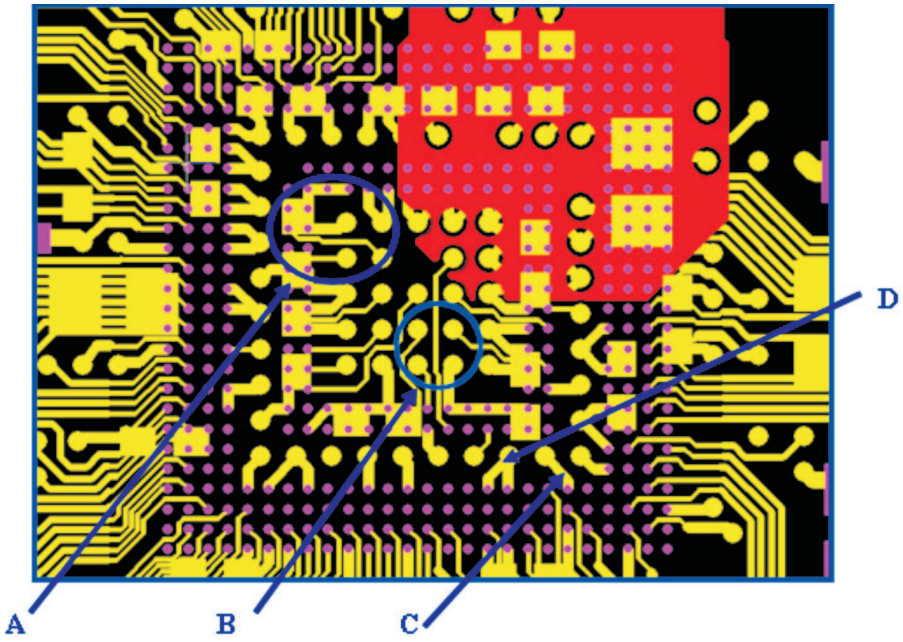

Figure 26. First Pass DFM of the OMAP35x EVM

This demonstrates how important good communication is between all members of the design team. Had this board gone into production, the yield would have been very poor. Our thanks to Elcoteq in Richardson, TX for their analysis from which this section was created. The list below has their comments tied to the various locations annotated in Figure 26.

- At location A, seven BGA Pads are ganged together. This acts as a large heatsink during reflow.
- The traces between D and the BGA pad should be narrower. A trace entering a pad should never be larger than the diameter of the pad.
- In some cases the BGA to ground plane is done like D and other it is done like A. Neither are good techniques.
- In C, the trace width exiting the BGA pad is much too large. In this case the trace acts as a heatsink during reflow.
- As in details A,B,C and D, the heat transfer from the ground planes is passing through a large via through a large trace and fanned out across 7 BGA pads ganged together.
- Do not gang BGA pads together with a copper plane as this increases the heat sink effect.

23 Acknowledgments

- Clint Cooley and Franklin Troung, CircuitCo, 675 N. Glenville #195, Richardson, TX 75081, 214-466-6690, www.CircuitCo.com
- Elcoteq, Sinimaentie 8B, P.O. Box 8, FI-02631 Espoo, Finland
- Micron Technology, Inc., 8000 South Federal Way, Post Office Box 6, Boise, ID 83707-0006

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