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No. 114

Best Layout Practices for Switching Power Supplies

— *By L. Haachitaba Mweene, Applications Manager*

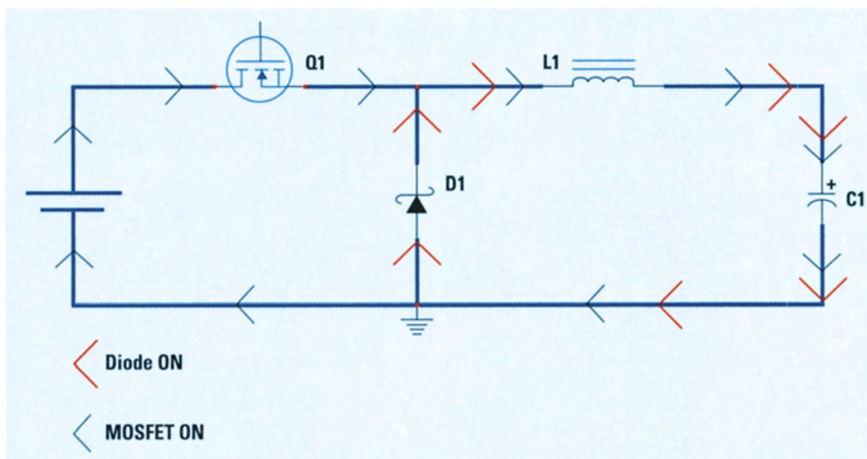

Figure 1. High di/dt Current Loops

Typical power supplies consists of a mixture of power components handling switching voltages and currents of large value and amplitude, and small signal components handling low-level analog signals, all in close proximity. Laying out a power supply board entails positioning and routing the components in such a way that the high-power signals do not corrupt the low-power signals and cause poor performance. A poor layout will lead to the generation of unwanted voltage and current spikes which will cause not only noise to appear on DC voltages in the supply, but also EMI to radiate to adjacent equipment. Thus proper layout techniques are critical to achieving optimal performance of a power supply. This article describes the most important of these techniques.

Placing the Power Components

After importing a power supply schematic into a PCB editing environment, deciding where and how to place and route many discrete components on the board can be confusing.

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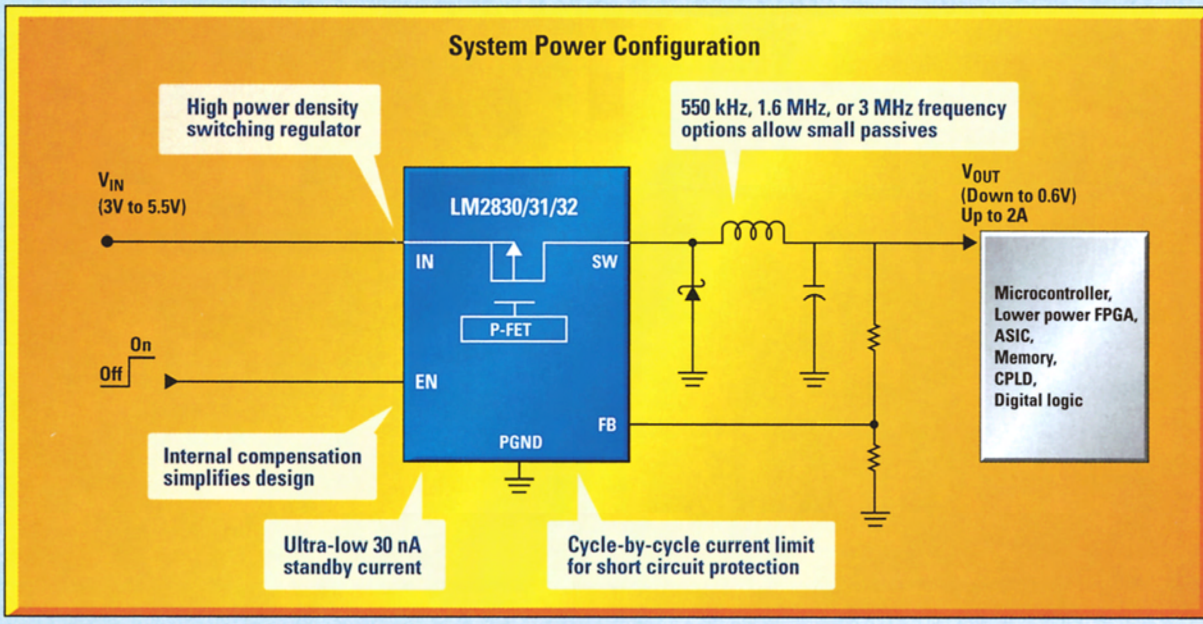

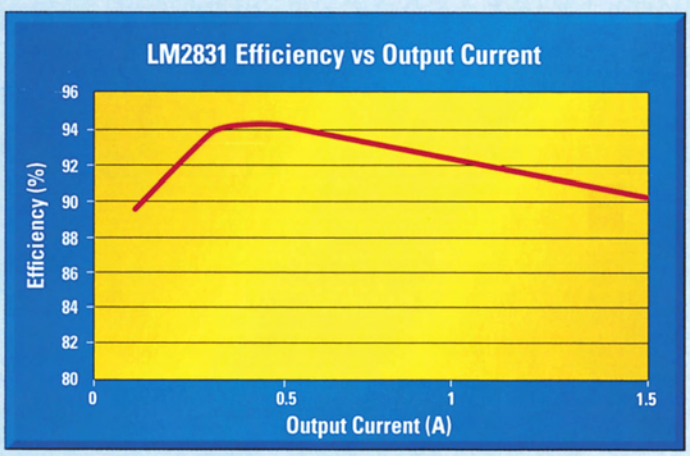

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Best Layout Practices for Switching Power Supplies

Most power supplies are laid out on multi-layer boards with four copper layers or more. Most of the board space will be occupied by the power components: input capacitors, MOSFETs, current sense resistors or transformers, rectifiers, inductors, and output capacitors. These components will pass large currents and require thick traces to connect them together. They should be laid out first.

First loops of high di/dt, where large switching currents circulate, should be identified and made as tight and compact as possible to minimize stray inductance that will otherwise lead to the generation of unwelcome voltage spikes. *Figure 1* shows how to identify these loops. In the figure, the small black arrows indicate how the current circulates when the MOSFET is on. The big red arrows indicate the current loop for when the diode is on. All the paths which have either a black or a red arrow (but not both) are the high di/dt paths.

Source currents and their return paths should flow one on top of the other or next to each other to minimize the areas of the loops they form and reduce the generation of magnetic interference. Input power should be taken by the switching circuitry from directly across the input capacitors. Similarly, the load current should be taken from directly across the output capacitor.

Circuit nodes should be sized according to the magnitude and nature of the current that passes through them. High impedance nodes with high di/dt, such as the switch node (the junction in many topologies where the MOSFET, the rectifier, and the inductor meet) should be as small as possible while being adequately large for the current flowing through them. Minimizing the size of such nodes minimizes the EMI generating area. Low impedance quiet nodes, such as ground or the output, should be made as large as possible.

Copper Thickness

The traces and copper pours carrying current from one power component to the next should be made adequately wide.

An approximate formula for the minimum trace width required to carry a given current which is accurate over a current range of 1 to 20A is

$$T = \frac{2}{CuWt}\left(-1.31 + 5.813I + 1.548I^2 - 0.0521I^3\right)$$

where T = trace width in mils; I = current in Amperes, and $CuWt$ = copper weight in ounces. The formula assumes that the current causes a temperature rise of 10 degrees Centigrade in the traces.

Using this formula, the minimum trace width for a current of 1A with 1 oz copper is 12 mils; for 5A, ½ oz copper it is 240 mils; and for 20A, ½ oz copper it is 1275 mils. If space allows, and especially where switching currents flow, these widths should be increased. Design goals of 30 mils per amp for 1 oz copper and 60 mils per amp for ½ oz copper should be striven for. Copper pours or floods should be used to connect the high current paths. Pours on multiple layers connected together with vias should be used for currents in excess of 10A.

Placing the Analog Components

Analog control components should be routed last because they take up little space and only need thin traces. One way to organize them is to create component subgroups by function and route the subgroups. For example, all the components that make up the feedback compensation network of the supply can be one subgroup. The bypass capacitors, soft-start capacitor, and frequency-setting resistor of the PWM controller can make up another subgroup. These subgroups typically connect to the PWM controller (or another IC). The subgroups should be placed as close to, and routed as directly as possible to the pin they connect to on the IC.

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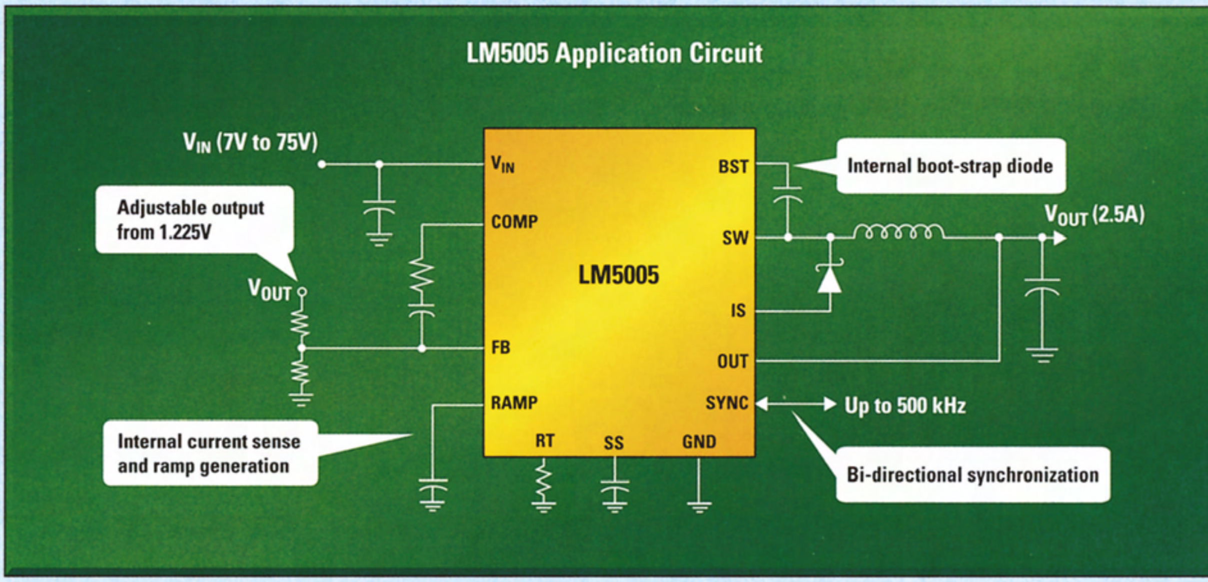

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Best Layout Practices for Switching Power Supplies

This is especially true of decoupling capacitors which must be right next to the pin that they decouple. The capacitors must connect directly to the pins, and not to any ground or power planes that are electrically part of the pins.

All the big components in the circuit, such as MOSFETs, rectifiers, electrolytic capacitors, inductors, and connectors should be put on the top side of the board so they do not fall off during reflow soldering. The bottom side of the board should contain only small components which can stick to the solder flux on the board by surface tension before they are soldered.

Grounding

When routing the circuitry around the controller IC, the analog small signal ground and the power ground for switching currents must be kept separate. It is suggested to isolate the control circuitry on a local ground island, which can then be connected to the rest of the system at only one point, preferably at the input capacitor. This stratagem helps to keep the analog ground quiet. If the creation of a ground island is not possible for all or some of these components, the ground pins of the components can be connected together as a daisy-chain, but they must still be connected to the main ground at one point.

Components which straddle high impedance and low impedance nodes must be placed close to the high impedance nodes. For example, resistors setting the output voltage will see a low impedance at the output and ground connections, and a high impedance where they connect to the input of the error amplifier. The resistors must be placed as near as possible to the error amplifier. To achieve the best possible load regulation, a separate trace that carries no load current must connect one resistor directly to the load terminal of the supply, and the bottom side of the other resistor must hook directly to the chip analog ground.

Segregating Analog and Switching Signals

Power inductors/transformers, MOSFETs, and rectifiers must be placed away from the traces and circuitry with low level analog signals to minimize the amount of noise from them that the analog circuitry picks up. If power switching and analog components cannot be segregated due to space constraints, they should be placed on opposite sides of a multi-layer board and an inner copper ground plane should be used to shield the two sets of components from each other. The ground plane must be connected to the rest of the circuit in such a manner that little or no current flows in it, so that it is electrically quiet. Only then can it be considered to be a low noise reference node. All high switching currents should be arranged to flow on wide copper pours on the top layer.

For a four layer board the layer stack-up should be as follows: all the power parts should be on the top layer, as well as the copper shapes carrying the large switching currents. This layer can also have small signal components. The second layer should be a quiet ground plane with no large currents flowing through it. Layer three and the bottom layer can have a mixture of power and signal traces, with only small components populating the bottom layer. As much of the board areas possible on all layers should be flooded with copper, to improve the thermal performance.

Vias

Though it is desirable to have all the high current paths on the top layer, this is not always possible because of board size, routing, and component placement constraints. Vias must then be used to make connections between layers and to parallel the layers to allow more current to be carried between components on the board.

Multiple vias should be used to connect high current paths on different layers. Microvias should be designed to pass a current of 1A each; 14 mil

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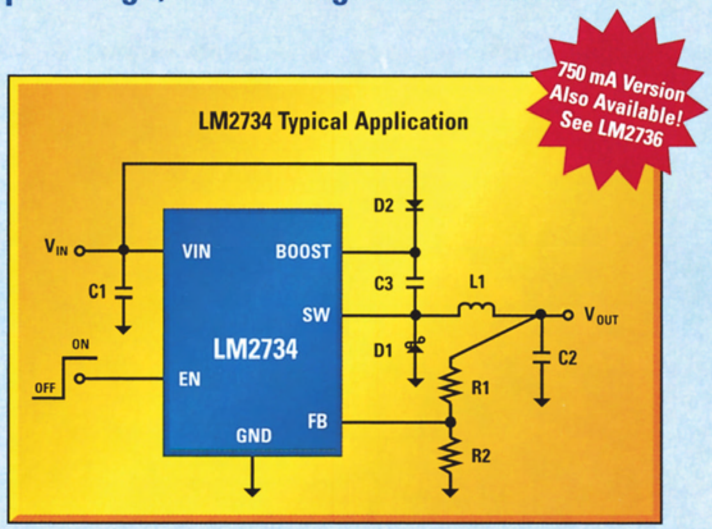

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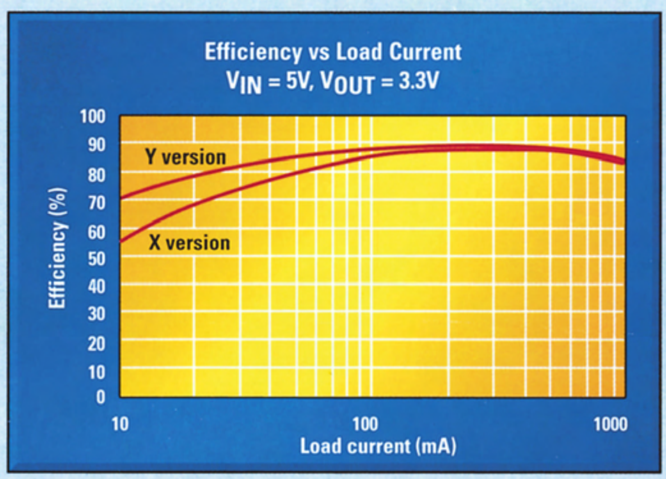

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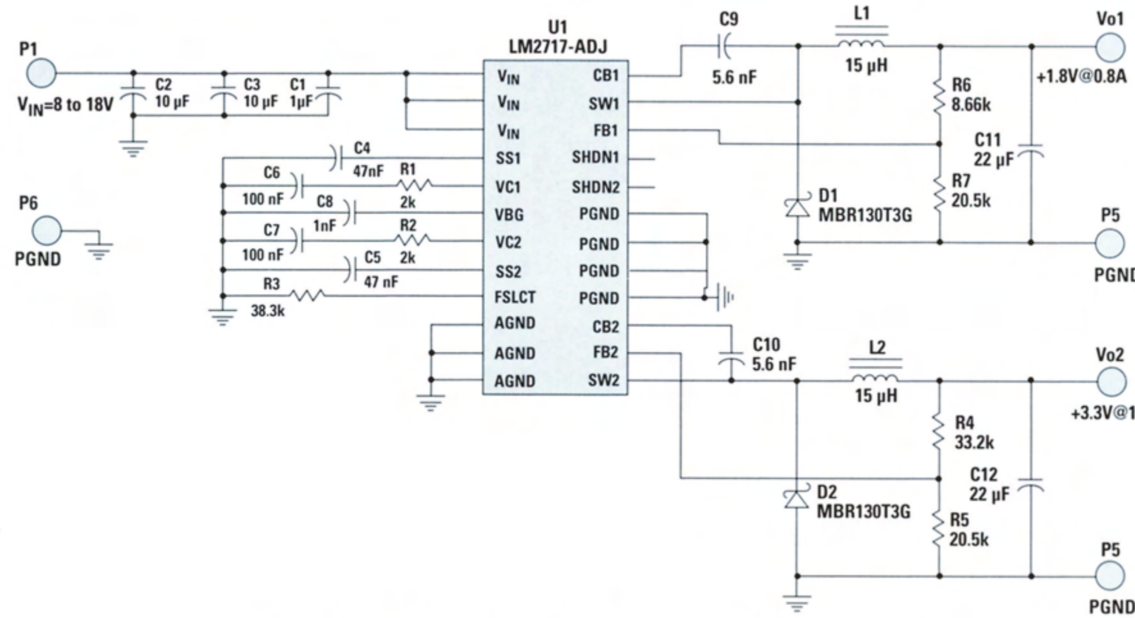


Figure 2. Circuit Schematic of a Dual Buck Converter Using the LM2717

diameter or larger vias should pass up to 2A; and 40 mil or larger vias should see no more than 5A each. Vias should be allowed to fill with solder to spread heat better, and copper alleyways in the direction of current flow should be left between them.

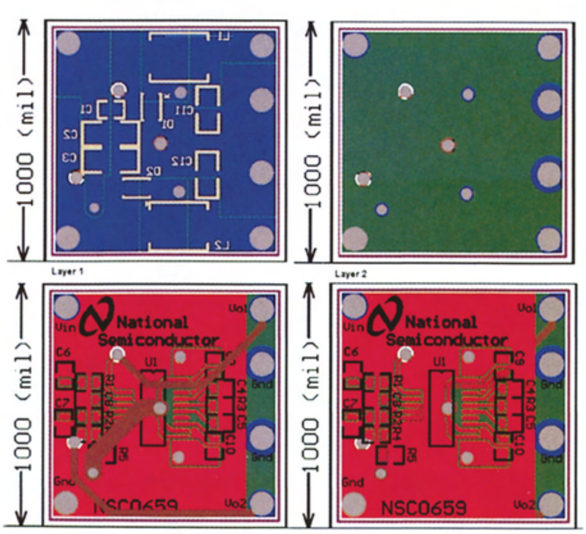


Figure 3. : A Well-Designed Four Layer Board for the Buck Schematic in *Figure 2*

Example Layout

The schematic in *Figure 2* is a dual buck converter based on the LM2717. A printed circuit board for this schematic is shown in *Figure 3* and incorporates the layout practices recommended in this article. Layer 1 contains all the power parts and thick copper pours to pass large currents. Layer 2 is a ground plane which is connected to the rest of the circuit at only one point near the input so it passes no current. Layer 3 and the bottom contain signal and power traces. All the components on the bottom layer are small. All the unused board area is flooded with copper.

More layout recommendations can be found in the references listed below, available on National's website. ■

Acknowledgement

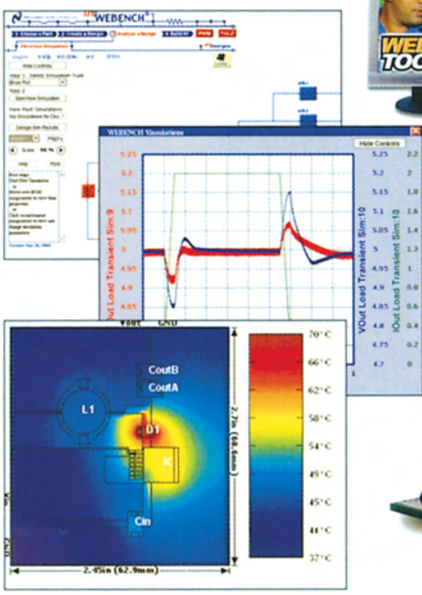
The author wishes to thank Craig Varga for reviewing this article and providing critical background material.

References

[1] "SIMPLE SWITCHER® PCB Layout Guidelines," National Semiconductor Application Note AN1229.

[2] "Layout Guidelines for Switching Power Supplies," National Semiconductor Application Note AN1149.

Power Design Tools



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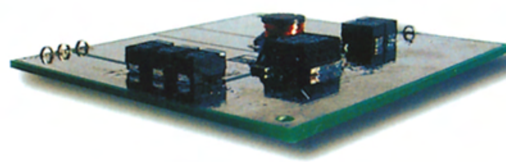

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