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IN A DESIGN IN WHICH YOU MUST REDUCE TIGHT TIMING, ROUTING ALL TIMING-SENSITIVE LINES IN BURIED STRIPLINE LAYERS MINIMIZES ONE SOURCE OF JITTER AND LOWERS THE OVERALL REQUIRED TIMING BUDGET.

Analysis of board layout helps cure jitter problems

ALL HIGH-SPEED-digital-product designers face the critical electrical-performance challenges of meeting a timing budget, meeting a noise budget, and passing an EMC (electromagnetic-compliance)-certification test. Designers need to account for a number of factors when calculating a timing budget. Most high-speed, digital products are synchronous, clocked systems, and they require that a series of operations happen within one clock cycle. These operations include all the gate-switching delays within one logic depth, the intrachip propagation delays, the interchip propagation delays, the rise time or charging delays from the interconnections, the setup-and-hold times, and the skews between the clock and the data lines. The timing budget allocates how much time is assigned for each source of delay.

"Jitter" is the variation in arrival time of a clock or data edge from cycle to cycle. The amount of jitter for a given signal may vary from cycle to cycle. Signal-propagation-delay sources can be either random, when you cannot predict the jitter, or deterministic, when you can predict the amount of jitter. Finally, you must add a "margin" to the timing budget; margin accounts for the inability to accurately predict all the other terms. The larger the uncertainty, the larger the margin you need to be confident of the product's correct operation.

As the clock frequency increases, the clock period becomes shorter. Designers try to meet the goal of ever-higher clock frequencies by minimizing each term in the timing budget. The better you can accurately predict each element of the timing budget, the smaller the margin you need. A smaller margin allows you to shorten the period and still meet the timing budget.

One type of deterministic jitter arises from crosstalk between adjacent lines in a bus even in low-loss interconnects. With models of the interconnect that allow prediction of the crosstalk and a good simulator that includes these crosstalk effects in the timing, you can accurately predict the deterministic jitter from crosstalk and minimize the jitter budget and reduce the margin. By understanding the source of the crosstalk-induced jitter, you can minimize its impact and make the cost-versus-performance trade-offs to optimize the final product.

CROSSTALK-INDUCED JITTER

Crosstalk-induced jitter occurs when the simultaneous signals on adjacent bit lines affect the arrival time of the signal on one bit line. If designers omit this form of deterministic jitter from their timing budgets, the product may fail. You can use a tightly coupled 3-bit bus as an example (**Figure 1**). In this bus, each line is a 50Ω, 9-in.-long microstrip, and the line and space are both 5 mils. You need only a 3-bit bus to understand the jitter problem because you need be concerned only with the center line and the track immediately adjacent. The effect of the tracks beyond is negligible compared with the effect from the coupling with the adjacent lines.

The center bit line is the "victim" line. You can simulate the arrival time of its signal at the receiver under three relevant conditions. You can simulate both "aggressor" lines—the adjacent bit lines on either side of the victim—to be

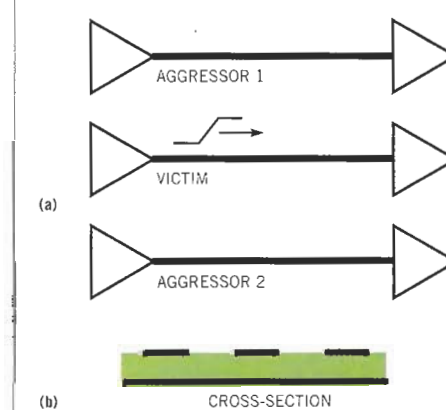

Figure 1 Two adjacent aggressor lines surround the victim line. The three microstrip traces have 5-mil lines and spaces.

When the adjacent aggressor bit lines have the opposite bit from that of the victim line, a large voltage difference occurs between the victim line and the aggressor lines, and a large fringe field exists between the lines. The higher the fraction of field lines from the victim line to the return path in the air, compared with through the bulk material, the lower the effective dielectric constant (**Figure 4**). A change in the effective dielectric constants changes the delay of the signal on the victim line, depending on the bit pattern on the aggressors. A change in the bit pattern on the aggressor lines, compared with the victim line, changes the time delay on the victim line. When the aggressors have the same bit pattern as the victim, the effective dielectric constant is higher, the propagation speed is lower, and the delay is longer. When the aggressors have the opposite bit pattern from that of the victim line, the effective dielectric constant is lower, the propagation speed is higher, and the time delay on the victim line is shorter.

One way of reducing deterministic jitter from crosstalk is to reduce the overlap of the fringe fields by spreading the traces farther apart. For example, by increasing the spacing between all the lines to twice the line width, a common design rule for acceptable near-end crosstalk, you can reduce the deterministic jitter to less than 60 psec out of 1.5 nsec, or about 4% (**Figure 5**). Too close a spacing between victim and aggressor lines may cause a crosstalk problem in addition to deterministic jitter. To decrease both crosstalk and jitter, the spacing should be as large as possible, or at least twice the line width. However, this approach means using a lower density—and, perhaps, more expensive—board. You need an EDA tool that accurately predicts crosstalk and deterministic jitter to evaluate cost-versus-performance trade-offs. A simulator that integrates a 2-D field solver should automatically take into account not only the noise effects, but also the deterministic jitter associated with crosstalk.

If variation in fringe fields in the air causes deterministic jitter from crosstalk, no deterministic jitter occurs in a structure with homogenous dielectric distributions, such as fully embedded microstrip or stripline. In a stripline geometry, the fringe fields between the victim and the aggressor lines might closely interact, but whatever the field distributions, the field lines from the victim trace always see the same dielectric constant, that of the bulk laminate (**Figure 6**). For the extreme case in which spacing is equal to the line width in a 50Ω stripline, the effective dielectric constant is always the bulk dielectric constant, independent of the bit pattern on the aggressor lines. As the bit pattern changes, no jitter occurs on the victim line (**Figure 7**). Though a lot of crosstalk voltage occurs on the victim line, no jitter occurs in the arrival time of the signal on the victim line.□

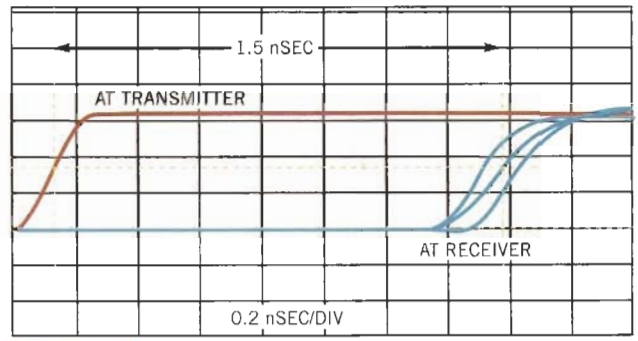

Figure 5 Doubling the spacing between victim and aggressor lines reduces jitter.

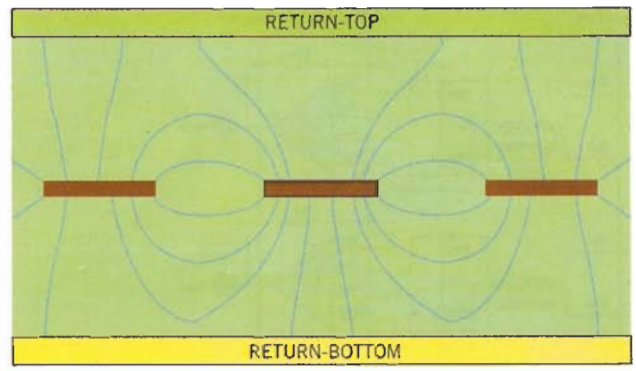

Figure 6 In a tightly coupled stripline, all field lines see exactly the same dielectric constant, independent of their distribution.

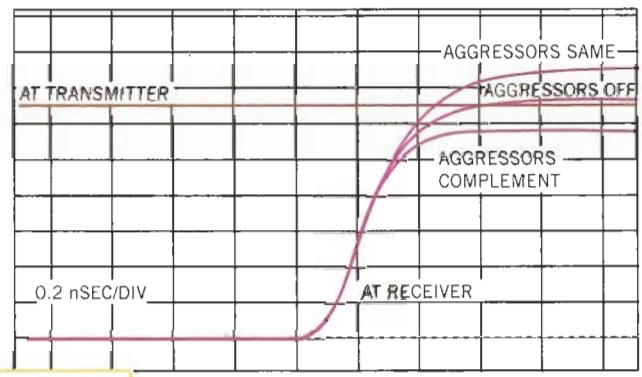

Figure 7 The signal at the receiver of a victim line in a tightly coupled stripline shows that jitter has disappeared. Though significant crosstalk exists, no deterministic jitter occurs.

AUTHORS' BIOGRAPHIES

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