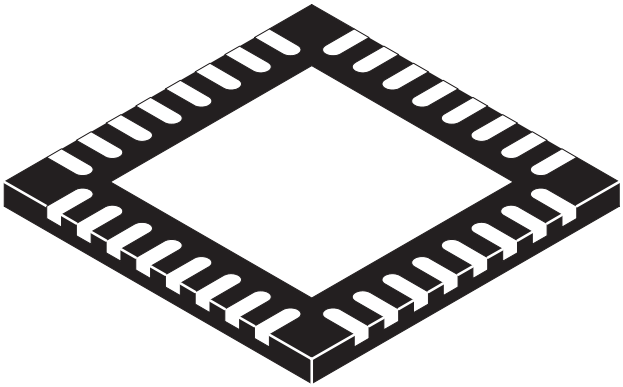
QFN/SON PCB Attachment

PMP Portable Power

ABSTRACT

Quad flatpack—no leads (QFN) and small outline—no leads (SON) are leadless packages with electrical connections made via lands on the bottom side of the component to the surface of the connecting substrate (PCB, ceramic). This application note presents users with introductory information about attaching QFN/SON devices to printed-circuit boards.



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1 Texas Instruments Quad Flatpack—No Leads and Small Outline—No Leads

1.1 Introduction

The QFNs and SONs are near-chip-scale package (CSP) plastic encapsulated packages that use conventional copper lead frame technology. This construction results in a cost-effective advanced packaging solution that helps to maximize board space with improved electrical and thermal performance over traditional leaded packages.

QFNs have solder lands on four sides of the package. SONs have solder lands on two sides of the package.

The QFN/SONs are available in a number of formats. The QFN/SONs are molded and mechanically singulated from a matrix leadframe. Package size is determined by several key factors including die size, number of terminations, etc.

All QFN/SONs are leadless packages with electrical connections made via lands on the bottom side of the component to the surface of the connecting substrate (PCB, ceramic). The standard QFN/SON package has an exposed pad that enhances the thermal and electrical characteristics, enabling high-power and high-frequency applications.

This QFN/SON PCB application note is only a guide. Precise process development and experimentation is needed in order to optimize specific applications/performance.

Inputs for this application note were supplied by several package subcontractors. More data, including board level reliability, should be available in the future.

2 Manufacturing Considerations

2.1 SMT Process

Many factors contribute to a high-yielding assembly process. A few of the key focus areas and their contributing factors are highlighted in Table 1.

Table 1. Essentials for Assembly Quality

Solder Paste Quality	Uniform viscosity and texture. Free from foreign material. Solder paste must be used before the expiration date. Shipment and storage temperatures must be maintained at the proper temperature. Paste must be protected from drying out on the solder stencil.
PCB Quality	Clean, flat, plated or coated solder land area. Attachment surface must be clean and free of solder mask residue.
Placement Accuracy	Tight tolerances are not usually required. CSP packages self-center as long as a major portion (more than 50 percent) of the lead finger is in contact with the solder paste covered land area on the board. Alignment marks (fiducials) on the PCB are helpful for verifying correct placement of parts.
Solder Reflow Profile	The solder reflow temperature is dependent on the PCB design, PCB thickness, type of components, component density, and the recommended profile of the solder paste being used. A reflow profile must be developed for each PCB type using various CSP packages. See the reflow profile in the solder reflow section (5.2).
Solder Volume	Solder volume is important to ensure optimum contact of all intended solder connections.

3 PCB Design Guidelines

One of the key efforts in implementing the QFN/SON package on a substrate motherboard is the design of the land pad. The QFN/SON has lead fingers exposed on the bottom side of the package. Electrical and mechanical connection between the component and motherboard can be made by screen printing solder paste on the motherboard and reflowing after placement. To ensure reliable solder joints, it is essential to design the pad pattern to the component exposed lead frame pattern.

3.1 Land Pad Styles

There are two basic designs for PCB land pads for the QFN/SON package—the copper defined or nonsolder mask defined style (NSMD) and the solder mask defined style (SMD). The industry has debated the merits of both styles of land pads, and, although we recommend the copper defined style land pad (NSMD), both styles are acceptable for use with the QFN/SON package.

NSMD pads are recommended over SMD pads due to the tighter tolerance on copper etching than solder masking. NSDM, by definition, also provides a larger copper pad area and allows the solder to anchor to the edges of the copper pads, thus providing improved solder joint reliability.

3.2 Land Pad Design

IPC-SM-782 is one of the industry standard guidelines for developing PCB pad patterns. As the QFN/SON is a new package style, consider this application note as a guide and use it with the IPC-SM-782 in designing an optimum PCB land pattern.

Figure 1 identifies the various QFN/SON dimensions required to design a matching substrate pad pattern. Because most packages are square with dimension D = E and the leads are along the E direction for dual packages, the side view dimensions (D, S, D2 and L) are used to determine the land length on the motherboard PCB/substrate. The motherboard PCB/substrate land pattern dimensions to be established are shown in Figure 2.

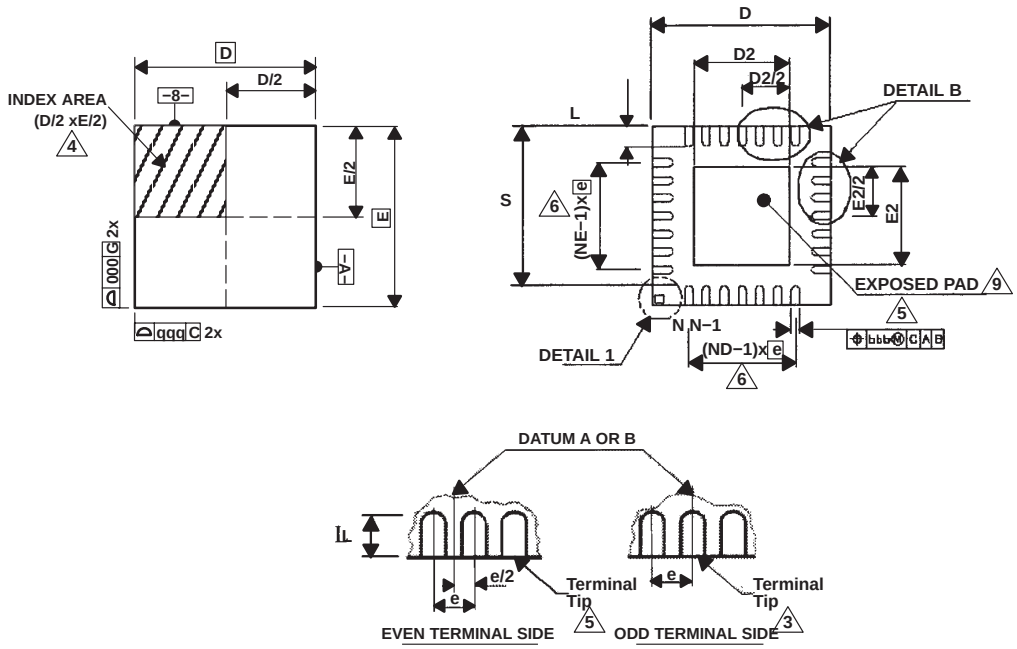

Figure 1. QFN/SON Outline Dimensions

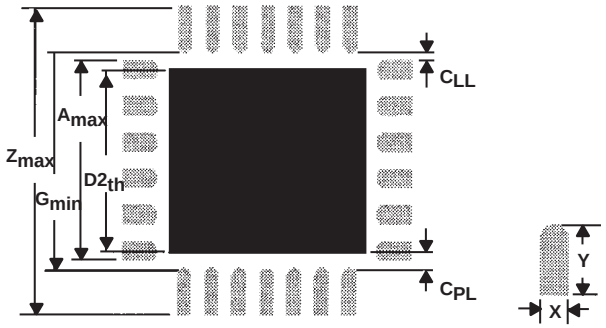

Figure 2. PCB Land Pattern

Table 2. PCB Dimension Definitions

SYMBOL	DESCRIPTION
Z_{max}	Outside pad terminal dimension
G_{min}	Inside pad terminal dimension
X	Lead pad width
Y	Lead pad height
C_{LL}	Corner pad edge to adjacent inside pad distance
C_{PL}	Central pad to inside edge of lead pad distance

The dimensions Z_{max} and G_{min} are the outside and inside pad terminal dimensions. X and Y identify the pad width and length. Clearance dimensions C_{LL} and C_{PL} are defined to prevent solder bridging.

3.3 Lead Finger Pad PCB Design

It is recommended that the PCB lead finger pad be designed a minimum of 0,1 mm longer than the package land length and be extended 0,05 mm towards the center line of the package. The width must be a minimum 0,05 mm (0,025 mm per side) (see Figure 3). However, the pad width is reduced to the dimension of the component pad for lead pitches of 0,5 mm to 0,28 mm wide to avoid solder bridging.

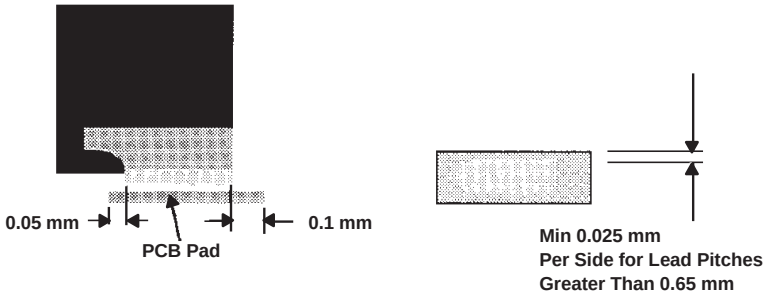

Figure 3. Substrate/PCB Lead Finger Geometry

3.4 Exposed Pad PCB Design

The construction of the exposed pad enables enhanced thermal and electrical characteristics. In order to take full advantage of this feature the pad must be physically connected to the PCB substrate with solder. The published data for thermal performance, θ_{JA}, is based on a four-layer PCB incorporating vias that act as the thermal path to the layers.

The dimensions of the thermal pad must be equal or greater than the exposed pad on the QFN/SON. Adequate clearance (Cpl) is necessary to prevent solder bridging. Experiments have concluded that a minimum clearance of 0,15 mm (0,2 mm recommended) is satisfactory for most designs.

Calculating PCB substrate pad size: $D2_{th} > D2$ but $\leq G_{min} - (2 \times Cpl)$

3.4.1 Thermal Pad Via Design

Based on thermal modeling, it is recommended that the thermal vias be placed on a pitch of approximately 1,0 mm. Per standard PCB manufacturing capabilities, 0,3 mm diameter drill holes are recommended. Vias must be plugged to prevent void formation between the exposed pad and PCB thermal pad due to solder escape by the capillary effect. This can be avoided by tenting the via during the solder mask process.

The via solder mask diameter must be 100 μm larger than the via hole diameter. Trials have shown that via tenting from the top is less likely to produce voids between the exposed pad and PCB pad.

3.5 Solder Mask

As described at the beginning of this section, non solder mask defined (NSMD) design is recommended over solder mask defined style (SMD) to produce good solder joint reliability. The solder mask can be designed around each individual lead finger for lead pitches 0,65 mm and above. Solder mask openings must be between 60 μm to 75 μm larger than the lead finger pad size. For a lead pitch of 0,5 mm, it is recommended to design the solder mask around all pads on each side. In order to maximize the solder mask between adjacent sides, it is necessary to round the inner corner on each row. This ensures sufficient solder mask in the corner of the PCB footprint design. See Figure 4.

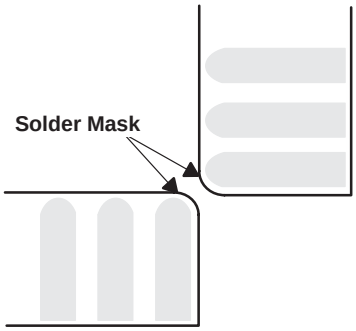

Figure 4. Substrate/PCB Solder Mask

3.6 Surface Finishes

There are a variety of surface finishes commonly available. The key factor in selecting an acceptable surface finish is to ensure that the land pads have a *uniform* coating. Irregular surface plating, uneven solder paste thickness, and crowning of the solder plating can reduce overall surface mount yields. Bare copper with an organic solderability preservative (OSP) coating, electroless nickel/immersion gold, or electroplated nickel/gold finishes have been shown to provide an acceptable land pad surface. One type of surface finish to avoid is referred to as a dry-film process. This is because the copper undercut effect caused during the dry film removal prevents optimal sidewall wetting during the reflow process.

Of the coating and plating options available, Ni/Au is the most versatile, providing the gold thickness is controlled. Typically 5 μm nickel, and between 0.05 μm and 0.1 μm gold are needed to prevent brittle solder joints.

The advantages of plating over OSPs are:

- Shelf life
- Permanent coverage of copper vias and other features not exposed to a solder process and
- Contamination resistance

A controlled assembly process for QFN/SON soldering relies on a flat uniform attachment site. Achieving this allows for greater control of solder paste print uniformity.

4 Solder Paste Screen Printing Process

4.1 Solder Paste

The quality of the paste print is an important factor in producing high-yield assemblies. The paste is the vehicle that provides the flux and solder alloy necessary for a reliable and repeatable assembly process. A low-residue, no-clean solder paste with Sn63/Pb37 is commonly used in mounting CSPs; however, water soluble flux materials are widely used as well. Typically the choice of solder paste determines the profile and reflow parameters. Most paste manufacturers provide a suggested thermal profile for their products and must be referenced prior to manufacturing. Special SMD specific solder pastes are being marketed by paste vendors that minimize voiding in the solder joint.

4.2 Solder Stencils

The formation of reliable solder joints is a necessity. The contrast between large exposed pad and small lead fingers of the QFN/SON can present a challenge in producing an even solder line thickness. To this end, careful consideration must be applied to the stencil design.

The stencil thickness, as well as the etched pattern geometry, determines the precise volume of solder paste deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow-solder processing.

Stencils are usually made of brass or stainless steel, with stainless steel being more durable. Apertures must be trapezoidal to ensure uniform release of the solder paste and to reduce smearing. Refer to Figure 5.

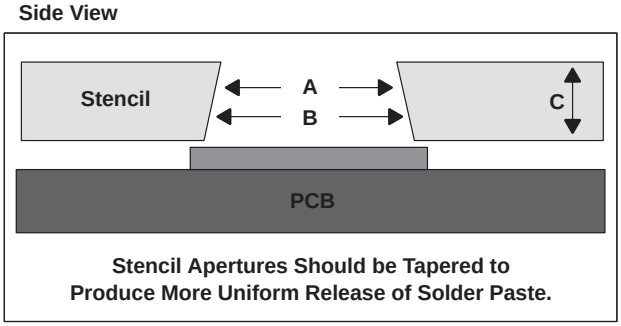

Figure 5. Solder Stencil Profile

The solder joint thickness of QFN/SON lead fingers must be 0,050 mm to 0,075 mm. Thickness of the stencils is usually in the 0,100 mm to 0,150 mm (0.004 in. to 0.006 in.) range. The actual thickness of a stencil is dependent on other surface mount devices on the PCB.

Use squeegee durometer of 95 or harder. The blade angle and speed must be fine-tuned to ensure even paste transfer. An inspection of the stenciled board is recommended before placing parts, because proper stencil application is the most important factor with regards to reflow yields further on in the process. As a guide, a stencil thickness of 0,125 mm (0.005 in.) for QFN/SON components is recommended.

4.3 Lead Finger Stencil Design

The stencil aperture is typically designed to match the PCB/substrate pad size, i.e., 1:1. For fine pitch components of 0,5 mm and below it may be necessary to reduce the stencil aperture length by 20%. This is necessary to aid solder paste printing, because a PCB pad of 0,25 mm leaves just 0,15 mm spacing between pads.

Lead finger stencil dimensions depend on the specific QFN/SON lead finger dimensions. Given a 0,5 mm pitch device with 0,28 mm wide pads a stencil thickness of 0,125 mm is needed. To get a good print, the pad length must be reduced by up to 20% at each end, with the width remaining the same.

The area ratio of the stencil is critical in order for the printing to get good paste release. For very small apertures where the area ratio is less than 0.66, the stencil must be nickel formed. This type of stencil has superior release characteristics over stencils that have been produced by laser. Experiments have shown that nickel formed stencils print with area ratios down to 0.57.

The aspect ratio relates to the manufacture of stencils. Stencil manufacturers require the aspect ratios to be greater than 1.5. See IPC7527.

AREA RATIO = Area of Aperature Opening/Aperture Wall Area

ASPECT RATIO = Aperture Width/Stencil Thickness

4.4 Exposed Pad Stencil Design

The QFN/SON package is thermally and electrically efficient—enabled by the exposed die attach pad on the under side of the package. The exposed die must be soldered down to the PCB or motherboard substrate.

It is good practice to minimize the presence of voids within the exposed pad interconnection. Total elimination is difficult, but the design of the exposed pad stencil is key. The proposed stencil design enables out-gassing of the solder paste during reflow as well as regulating the finished solder thickness. Typically the solder paste coverage is approximately 50% of the pad area.

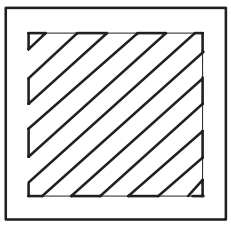

Figure 6. Exposed Pad Stencil Design

5 Package to Board Assembly Process

5.1 Placement and Alignment

The pick and place accuracy governs the package placement and rotational (theta) alignment. This is equipment/process dependent. Slightly misaligned parts (less than 50 percent off the pad center) automatically self-align during reflow (see Figure 7).

Grossly misaligned packages (greater than 50 percent off pad center) must be removed prior to reflow, as they may develop electrical shorts resulting from solder bridges, if they are subjected to reflow. There are two popular methods for package alignment using machine vision:

- Package silhouette. The vision system locates the package outline.
- Lead frame recognition. Some vision systems can directly locate on the lead frame pattern.

Both methods are acceptable for QFN/SON placement. The pad recognition type alignment tends to be more accurate, but is also slower since more complex vision processing is required of the pick and place machine.

The package silhouette method allows the pick and place system to run faster, but is generally less accurate. Both methods are acceptable and have been successfully demonstrated by major pick and place equipment vendors and contract assembly houses.

5.2 Solder Reflow

There are no special requirements necessary when reflowing QFN/SON components. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile must be checked at different locations on the board. Component temperatures may vary because of surrounding components, location of the device on the board, and package densities.

To maximize the self-alignment effect of QFN/SON (see Figure 7), it is recommended that the maximum reflow temperature specified for the solder paste not be exceeded. A good guide is to subject the PCB to a temperature ramp not exceeding 4°C per second.

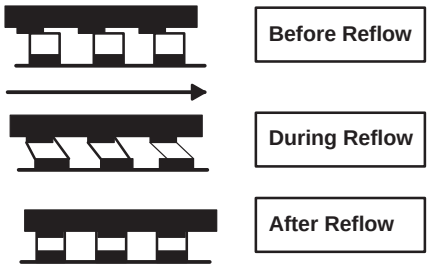

Figure 7. Package Self-Alignment at Reflow

The reflow profile guidelines are based on the temperature at the actual solder-pad-to-PCB-land-pad solder-joint location. The actual temperature at the solder joint is often different than the temperature settings in the reflow/rework system due to the location of the system thermocouple placement used to monitor the temperature.

Specific production reflow and rework systems vary depending on manufacturer and model. Therefore, system specific profiles must be established using thermocouples at the actual solder joint locations.

TI has tested and qualified QFN/SONs for a maximum of three reflow operations. This allows one reflow operation per side of the PCB (assuming the use of a double-sided PCB) and one rework operation if necessary.

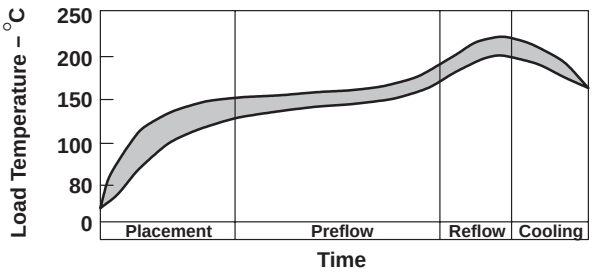

Figure 8. QFN/SON Load Temperature vs Reflow Profile

5.3 PCB Cleaning

If a low-residue, no-clean solder paste is used, PCB cleaning is not required, and has little effect on QFN/SONs. With the elimination of materials containing CFCs, most companies have moved to a no-clean or aqueous flux-based system. *No clean* fluxes and solders simply mean that there are no harmful residues left on the board that could cause corrosion or damage to the components if left on the board. This residue has sometimes been shown to be a collection point for outside contamination on the board surface. Because there are so many different types of no-clean solder pastes available, application specific evaluations must be performed to identify any remaining residues still needing to be removed from the boards in final production.

5.4 Inspection

Inspection of QFN/SONs on a PCB is typically accomplished by using transmission type X-ray equipment.

In most cases, 100 percent inspection is not performed. Typically, X-ray inspection is used to establish process parameters and then to monitor the production equipment and process. Transmission X-ray can detect bridging, shorts, opens, and solder voids. There are many different types of X-ray inspection equipment available and functionality varies. X-ray inspection system features range from manual to automated optical inspection (AOI). Different systems also provide single-dimensional or multidimensional inspection capabilities.

As explained in the *Solder Reflow* section of this guide, QFN/SONs self-align to the land pad using surface tension during the solder reflow process. As a result, it is very unlikely that a QFN/SON will be marginally misaligned. If a misalignment does occur, it is likely to be by an entire pad. This effect makes it possible to do a gross visual alignment check after the reflow. Fiducial marks on the PCB can aid visual checks of the PCB and are also useful for manually placing units during any rework.

6 Rework

Rework equipment has continued to progress rapidly to address chip scale packages. Many manufacturers use a single rework station to incorporate multiple rework process steps, such as component removal, site redress, solder paste/flux application, alignment, component placement and reflow. The advancement of beam-splitting imaging for alignment/placement and other areas such as characterizing and storing individual component reflow profiles has greatly simplified the rework process.

With the direction of QFN/SONs allowing more functionality/features on smaller products, one of the areas of concern is thermal separation of adjoining components during the rework process. Some manufacturers have addressed this concern by designing hot gas nozzles which maintain the keepout zone area around the rework component to thermally isolate adjacent components during the reflow process.

Original equipment manufacturers have differing requirements when it comes to solder paste and flux-only applications during the rework process. For those who require solder paste, microstencils and squeegees have been developed. These microstencils are aligned using the same beam-splitting imaging as the component placement. Microsqueegees allow for a simple, uniform solder paste coverage across the microstencil.

6.1 Component Removal

Removing the component is by far the easiest part of the rework process. Once the thermal profile is optimized, the process parameters are used to remove the device.

The gas nozzle used during this process surrounds the device and seals against the board. The QFN/SON is heated from the top side with hot gas while residual heat is exhausted up and away from adjacent components. The anticrushing feature in the nozzle prevents excessive topside force from being applied to the QFN/SON. The entire assembly is also heated from the bottom side with an under-board heater to help prevent warpage. Preheating the board to a fixed temperature before the component is heated also helps to ensure process repeatability. Once the reflow process is complete, the nozzle vacuum cup is automatically activated and the component is slowly lifted off the pads. The vacuum cup in the nozzle is designed to disengage if the component has not fully reflowed for any reason. This prevents the potential for lifting pads. The application of flux is recommended for QFN/SON removal.

6.2 Site Redress

Once the QFN/SON has been removed, the residual solder that remains on the pads must be removed. The QFN/SON PCB site is very fragile due to its extremely small pad sizes. To avoid damaging the pads or solder mask, the site redress process must be performed very carefully. No clean paste flux is applied to the site after component removal. Using a temperature controlled soldering iron fitted with a small flat blade, gently apply solder braid that has been presoaked in flux over the PCB PADS.

Residual flux is removed from the site with alcohol and a lint-free swab. The site is then inspected prior to the replacement process.

6.3 Component Replacement and Reflow

A component insertion tool is used to ensure proper registration of lightweight QFN/SONs in the nozzle. In addition, the insertion tool eliminates manual handling of the component, which can deposit unwanted skin oil on the component pads.

Optical systems used for alignment consist of a beam-splitting prism combined with an inspection microscope or video camera fitted with a zoom lens. This optical system allows the operator to see a magnified image of the bottom side of the QFN/SON superimposed over the corresponding PCB land pattern.

Alignment and placement of the QFN/SON must be accurate to within 0,1 mm.

When the QFN/SON is correctly aligned, the X-Y table is locked to prevent further movement.

The nozzle is lowered until it lightly contacts the board. The nozzle vacuum is automatically deactivated and the thermal reflow cycle begins. PC-based software provides the process control necessary to ensure repeatable results. Once the cool down stage is complete, the nozzle is raised and the assembly is removed for inspection.

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