

PCB DESIGN PERFECTION: THE CAD LIBRARY SERIES PART 1: MOLDED BODY COMPONENTS

CONTENT ACKNOWLEDGEMENT: TOM HAUSHERR, DEVELOPER OF THE LP WIZARD (NOW XDM LAND PATTERN CREATOR), AND FORMER EDA LIBRARY PRODUCT MANAGER AT MENTOR GRAPHICS.

ABSTRACT

The CAD library is the starting point that affects every process from PCB layout through PCB manufacturing and assembly. There are dozens of things to consider when creating a CAD library. Each can directly affect the quality of the part placement, via fanout, trace routing, post processing, fabrication and assembly processes. Yet, they are often overlooked.

This paper, the first in a series dedicated to CAD library quality, describes each aspect you should consider when creating Molded Body Component library parts. It also describes the impact each feature has in the PCB process.



P A D S

W H I T E P A P E R

CAD LIBRARY PARTS

There are three types of CAD library parts; plated throughhole (PTH), surface mount devices (SMD), and a combination of the two technologies. SMD and PTH CAD libraries are distinctively different but the same basic rules apply to both technologies: "snap" and "round-off" CAD library land (pad) shapes to 0.05 mm increments. All of the component land patterns represented in this document are included in the xDX Land Pattern Creator that comes free with every seat of PADS® PCB design software.

THE UNITS

Today, 90% of all component manufacturers list their component package dimensions in metric units. For example, Texas Instruments only provides metric units for their component packages. TI is following the metric mandate by all world standards organizations and 99% of all world governments. Accordingly, this paper utilizes metric units for CAD library development.

THE CALCULATIONS

The examples in this document are calculated utilizing the nominal environment as defined in IPC-7351B's standard 3-tier CAD library system: See Figure 1.

1. Level A = Most – for military and medical applications.
2. Level B = Nominal – for controlled environment desktop.
3. Level C = Least – for cell phones and hand-held devices.

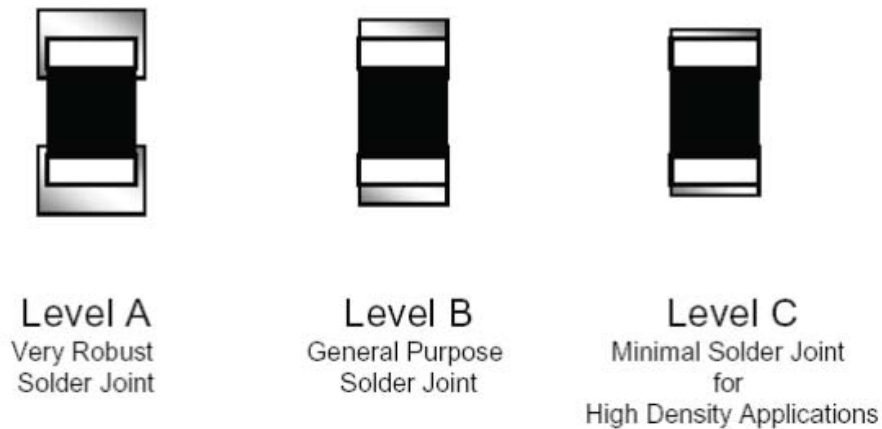


Figure 1: IPC-7351B's 3-tier solder goal density levels

MOLDED BODY COMPONENTS

With the exception of chip components, the next most-popular component family on a PCB design layout is the molded body tantalum capacitor (CAPM). The CAPM components have an “L-Bend” component lead form. Most molded body tantalum capacitors are metric by default, including their standard EIA names:

- 3216 – 3.2 mm X 1.6 mm
- 6032 – 6.0 mm X 3.2 mm
- 7243 – 7.2 mm X 4.3 mm
- 7343 – 7.3 mm X 4.3 mm

The common component families that use the molded body package are:

- Non-polarized capacitors
- Polarized capacitors
- Diodes
- Resistors
- Inductors
- Fuses
- LEDs

Figure 2 provides the 6032 component and land pattern dimensions. A rule was broken to create this land pattern. Instead of a 1.0 mm land placement round-off, a 2.0 mm land placement round-off was used to snap the land centers on a 0.5 mm grid from the center of the land pattern. When the land pattern is placed on a 0.5 mm grid, the land centers fall on a 0.5 mm grid. This improves the via fanout seen in Figure 4.

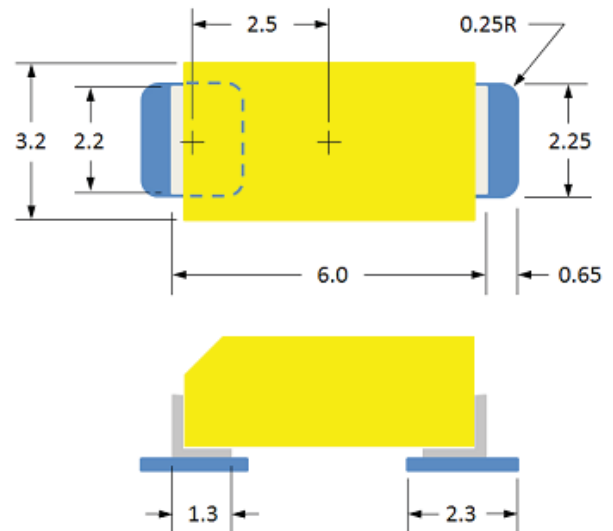


Figure 2: 6032 component and land pattern dimensions

Figure 3 illustrates the silkscreen and placement courtyard rules and sizes. The illustration shows the component leads on top of the lands for graphic representation.

Figure 4 illustrates the via fanout for a 6032 tantalum capacitor. If you are going to use the same-size via to maintain trace/space compatibility with the rest of the PCB layout, at least two vias are recommended.

Placement of these vias is critical for reducing impedance and increasing capacitance. It's important that the vias be placed as close as possible to the capacitor terminal leads. In Figure 4, the two vias coming out the side are 0.15 mm away from the terminal lead. The vias coming out the ends on the land pattern are 0.75 mm away from the terminal leads. Although that's five times farther away than the vias coming out the sides, some EE engineers will request all four vias. Since all the traces and vias are snapped to a 0.5 mm grid, this makes copy/paste much easier to manually fan out all of the 6032 molded body capacitors. The dot grid display is 1 mm and the land pattern is placed on a 0.5 mm grid. All the vias in this illustration fall on a 1 mm snap grid.

For the 7343 molded body tantalum capacitor, Figure 4, it is recommended that a larger via size, with a 1 mm land, 0.55 mm hole size, and 1.3 mm plane anti-pad, be used. The larger via can carry more current and you only need two (but the EE will ask for a 3rd one).

The illustration in Figure 5 snaps all the vias to a 1 mm grid system. These vias are twice the size of the previous vias but the same trace/space rules apply. The display grid is 1 mm. Because the land pattern, traces, and vias are on a 1 mm snap grid, this improves the copy/paste feature for manual fanout of all of the 7343 molded body components in your PCB layout.

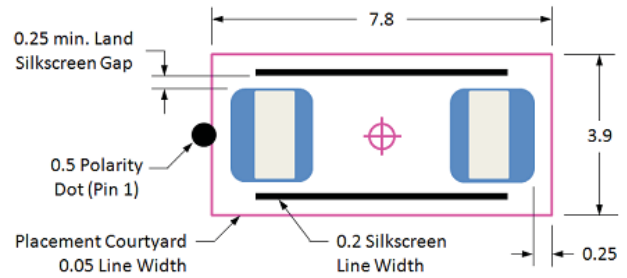


Figure 3: Typical 0603 silkscreen and placement courtyard

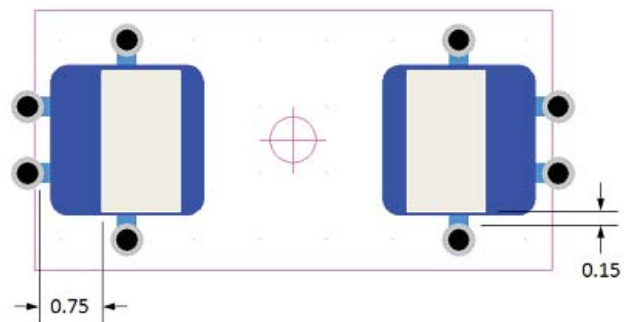


Figure 4: Typical 0603 via fanout

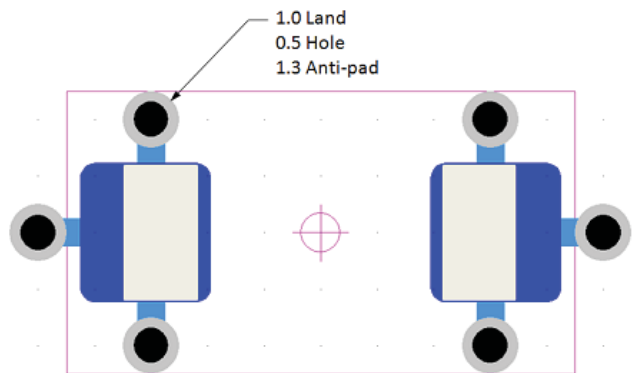


Figure 5: Typical 7343 via fanout

SOME MOLDED BODY COMPONENT FAQ'S

Q: Do multiple and larger vias affect CAPM soldering?

A: The GND & PWR vias have a direct plane connection (no thermal pattern in the via hole). The thermal relief in this fanout is the trace between the Land and the via so you can have as many vias as you want as long as the total sum of the trace widths + via hole diameters connecting the land and vias does not exceed 60% of the land diameter. This is noted in the IPC-2221 and 2222 documents where it says that the total "spoke widths" should not exceed 60% of a hole diameter for a through-hole lead to prevent a cold solder joint. So be careful that you do not use multiple vias with wide trace widths.

Two vias are typically recommended for bulk tantalum capacitors. Three vias are shown in Figure 5 to illustrate the preferred via locations. Having two vias that come out of the sides of the land pattern is common because they are closer to the component leads. It is not recommended to have the vias come out of the ends of the land pattern because they are further away from the component leads. The closer the via is to the component lead, the greater the capacitance and reduced inductance. This via location tip only applies to bypass decoupling capacitors and discrete parts that are attached to the planes. It is also typical to see trace widths that are the same width as the via diameter. A 1.0 mm via diameter would have a 1 mm trace width. The picture shows a 1 mm via with a 0.5 mm trace width.

Q: For a square land, what "diameter" should be used for calculating the 60% maximum spoke width?

A: There are no rules for calculating spoke width for SMD lands. The 60% rule is in relation to the "hole diameter."

Q: Do the two vias on the sides (Figure 3) leave a solder web between the via and the pad?

A: The vias coming out the "side" (rather than the top and bottom) of a chip capacitor to get the via as close to the component lead as possible to increase capacitance and decrease impedance. Ultimately, via-in-pad under the component lead will result in the best high-speed performance and highest component-packing density.

"Bottom only" component leads (like all the grid arrays: LGA, BGA, CGA) and fine pitch will drive via-in-pad to become more popular. The fact is that if you put via-in-pad on one part, you might as well do it on all parts because the fabrication cost does not change. i.e.: once you start to use via-in-pad, the fabrication cost automatically goes up, but it does not increase with the number of via-in-pads (unless you exceed several thousand holes). Each manufacturer is different.

Q: If there were no solder mask between the via and the pad, would solder migration be a concern?

A: All vias, on the same layer as the components, should be "tented" with solder mask. If there are only components on the top layer, then only the top-layer vias need to be tented. If there are components on both sides, then both sides should have tented vias.

CONCLUSION

Every design aspect should be considered when creating molded body components and the impact that each feature of the land pattern has in the PCB design process. The land pattern is the starting point that affects every process from PCB layout through PCB manufacturing and assembly. There are dozens of things to consider when creating a CAD library that are often overlooked; this paper discussed the factors to consider when creating molded body component library parts. Each factor can directly affect the quality of the part placement, via fanout, trace routing, post processing, and fabrication and assembly processes.

DID YOU KNOW?

PADS, Mentor Graphics' Personal Automated Design System, includes everything you need in order to create your component library. PADS provides a highly integrated library and component management environment that meets designers' and engineers' needs in creating and maintaining PCB design libraries.

PADS LIBRARY MANAGEMENT COMBINES:

- A starter library containing more than 10,000 ready-to-use, IPC-compliant, proven parts provided by Optimum Design Associates for a quick start to new design projects.
- Web access to component supplier data with an ability to load contents into PADS
- A central library for maintaining up-to-date design data. The central library contains all library elements in the same location, and is available at all design stages. PADS makes it possible to maintain an up-to-date library in real time, without any compilation, and includes all library elements (e.g., symbols, part data, footprints, simulation models, drawing items, and part common-property definitions).
- A component management system, integrated with schematic design and library management environments.
- A built-in consistency check of library data to make sure your library is constantly in-sync.
- Live verification of symbols placed in your schematic against the latest component and library data to eliminate costly redesigns and quality problems that might otherwise go undetected until late in the design cycle.
- A land pattern creator for quick creation of IPC-standard footprints.
- A migration path for 3rd-party libraries and component databases.

For the latest product information, call us or visit: www.pads.com

©2015 Mentor Graphics Corporation, all rights reserved. This document contains information that is proprietary to Mentor Graphics Corporation and may be duplicated in whole or in part by the original recipient for internal business purposes only, provided that this entire notice appears in all copies. In accepting this document, the recipient agrees to make every reasonable effort to prevent unauthorized use of this information. All trademarks mentioned in this document are the trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

