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Stacked-chip-scale-package-design guidelines

DESIGN OPTIMIZATION HELPS TO AVOID MANUFACTURING PROBLEMS, TO MAXIMIZE PRODUCT PERFORMANCE, AND TO ACHIEVE LOWEST PACKAGING COST.

You can configure the die stack for S-CSPs (stacked-die chip-scale packages) in multiple ways. However, using design guidelines can help you use die stacking for laminate-based and wire-bonded S-CSPs with more than 200 I/O pins. These packages typically find use in handheld products. When stacking mixed-technology dice, such as ASICs and memory, the challenge is often how to deal with wire-bond density. Wire-bond design must maximize the space between adjacent wires and minimize wire sweep—that is, wire misalignment in the horizontal plane. Wire sweep is undesirable because it can affect the inductance of adjacent wires, create noise, or cause a short when wires touch. Wire-sweep problems can occur at various stages during the wire-bonding process.

The two most common wire-bonding- and wire-loop-control methods in S-CSP assembly are conventional ball bonding and "reverse" SSB (standoff-stitch bonding). In conventional ball bonding, the first bond is to the die pad, and the second is to the substrate finger. In SSB, the first bond is to the substrate finger, and the second is to a stud on the die pad. SSB addresses die-to-die bonding and provides higher wire loops. However, SSB is by nature more prone to wire-sweep problems occurring at heat-sensitive zones, raising the risk of wire breakage. Also, the longer SSB wires are more prone to stitch misplacement and wire sagging.

In general, longer wires increase the risk of wire sweep. For a given distance between a die pad and a substrate finger, SSB results in a longer wire than that for conventional ball bonding. You should avoid SSB in S-CSP design, instead using conventional wire bonding whenever possible. Conventional wire bonding is also advantageous because it has a throughput approximately 1.5 times higher than SSB, helping to lower manufacturing cost. Overall, S-CSP design should minimize wire length by optimizing the substrate's bonding-finger location to minimize pad-to-finger distances.

With S-CSP, wire crossing can create the risk of yield loss from wire shorts, and you must take care to minimize wire crossing through the die and the substrate. Proper management of wire crossing at package design means that you will avoid wire crossing. However, when you cannot avoid wire crossing, place crossing wires within a design-safety zone. In a design-safety zone, you can, for example, maximize the spacing between crossing wires and maintain reasonably high wire loops. You can achieve these design goals by proper bond-finger placement.

In **Figure 1**, some of the lower (green) wires cross under the upper (purple) wires at points close to second-bond termination, at which the upper wires bond to the die pads. This situation creates a risk of wire shorts from wire sweep. To optimize this design, designers relocated the bonding fingers for the lower wires closer to the die edge. Although wire crossing still exists, the modified design puts the crossing points close to the middle span of the upper wire tier, thus increasing wire spacing where the wires cross.

In many cases, staggered rows of bond fingers, rather than one row, help reduce wire crossing: Bond fingers on the substrate for the lower die reside on the inner row, and bond fingers for the upper die reside on the outer row. The loop height of both wire tiers must then achieve sufficient spacing between both tier wires.

DIE LOCATION AND STACKUP

The location of one die with respect to the other is critical in many respects. For example, a designer may be able to significantly shorten bond wires just by shifting die location or achieve more die-to-die bonding by moving one die respective

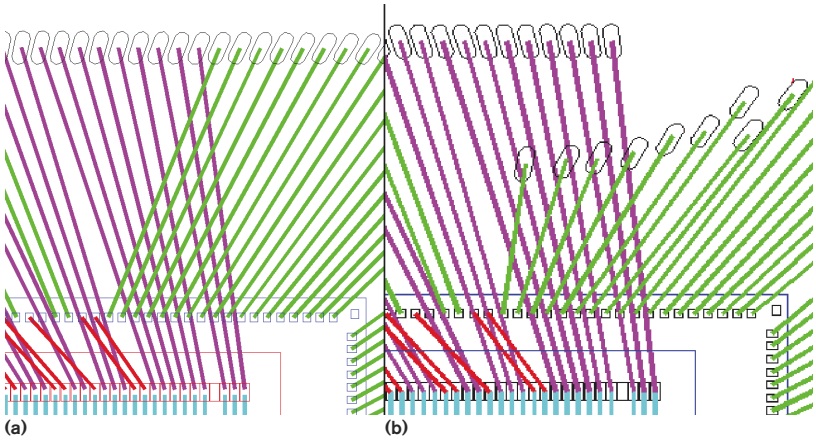

Figure 1 A substrate-design change minimizes wire crossing by placing touch-prone wire crossings close to the second bond termination (a) and moving them to the midspan of the upper wire (b).

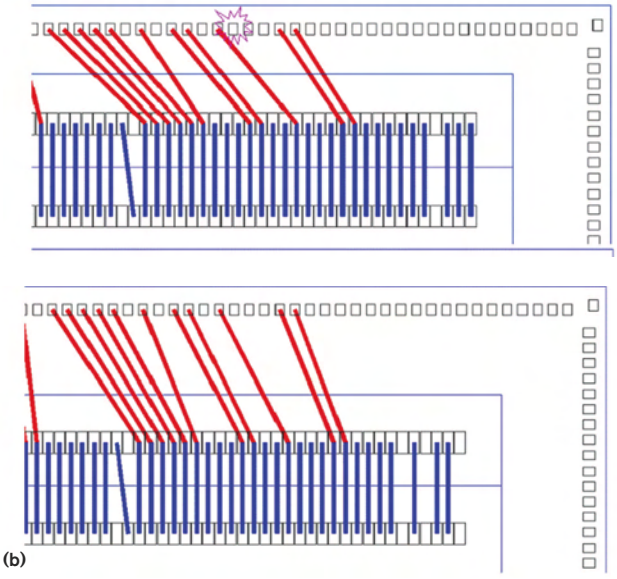

Figure 2 You can avoid a shorted wire (a) by shifting relative die location (b).

to another (**Figure 2**). During the bonding operation, the trajectory of the wire-bond capillary often swings backward—that is, opposite from the direction of the second bond—to create the desired loop in the wire. With S-CSP, die-to-die bonds often exist, as does a risk that capillary movement might interfere with previously bonded wires. You can avoid such interference through wire-loop and wire-bonding-sequence design.

Several three-die stack-wiring options exist. The options in **Figure 3a** and **b** result in capillary interference. You can avoid this interference with the wire loops and bonding sequences (**Figure 3c** and **d**). In addition, wire-loop and -bonding sequence influences die-pad size, so you must consider these factors early in the die-design stage of IC development. Wireless-system applications typically dictate aggressive low-profile S-CSP specifications. It is critical to perform a die-stackup analysis during package design to understand wire-bonding requirements. Low-loop wires ensure a sufficient wire-to-mold-top surface and good mold flow. Sufficient mold-compound thickness above the die avoids yield loss from incomplete fill, mold void, and excessive wire sweep during molding.

The effect of wire length on electrical performance is critical. Resistance increases from wire length are dramatically higher than increases in substrate-trace lengths. In addition, using smaller diameter wire results in higher resistance. Stacked-die packages, especially those with pyramid die stacks—that is, smaller die on larger die—have longer wire runs that you must carefully consider. By optimizing bond-finger placement and adopting chamfered corners on bond fingers, you can reduce wire resistance by reducing wire length. In addition, die-to-package orientation may help to alleviate wire-length issues, but you must carefully consider this orientation to avoid creating other problems. Designing for high performance requires consideration of critical nets as constraints; you should optimize the pinout, finger placement, and routing of the critical nets before those for noncritical nets. A co-design effort is critical for optimized package electrical performance.

STACKING SEQUENCE

Design issues to consider for die stacking include trade-offs between pyramid stacking and same-size-die stacking—that is, stacking equal-sized or larger die on another die when an inter-die spacer enables access to pads on the lower die. When a small ASIC die has strict performance requirements, you should locate it at the bottom of the stack, so that it can use shorter wires (**Figure 4**). A fundamental goal of stacked-die packaging is to lower cost to the end user by reducing board space and component count. For the end customer, the objective is to create more integrated packaging using methods, such as stacked-die packaging, that translate into lower cost and a smaller form factor for the product. However, stacked-die packaging is not inherently less costly. Advanced package suppliers face a number of issues surrounding die stacking, including die and assembly yields, additional assembly costs, increased logistical costs, and increased material costs. You must carefully manage these items so that the end products both work correctly and provide adequate profit margins.

Die and assembly yields are the most critical factors when estimating the cost feasibility of multidie packaging. However, other factors also can have a significant impact on the total-cost model. These factors, which tie closely to the concept of design for manufacturability, center on the substrate: the main component of the package. Rigid CSP substrates commonly find use in wireless- and handheld-system applications because of their versatility in routing and density capabilities. Over the last several years, significant improvements have emerged in laminate-substrate technologies to adapt to the developing needs of handheld systems. Single-die laminates have focused on improving bond-finger pitch, and the silicon designers have targeted improving the bond-pad pitch. With greater I/O counts and

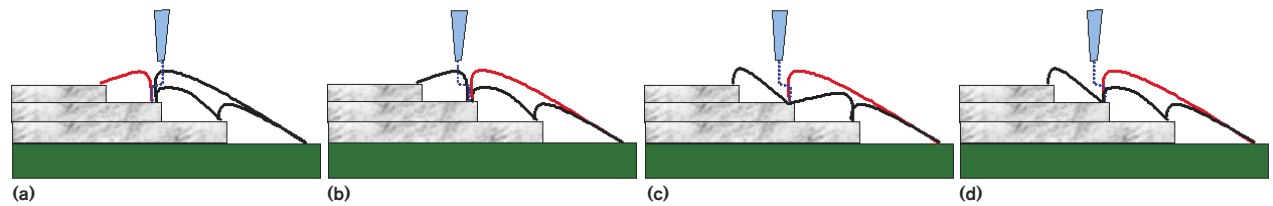

Figure 3 In a three-die stack, wire-loop-sequence options include those with capillary movement (a and b) and those without capillary interference (c and d).

smaller package-substrate areas, all the main-substrate technological parameters have improved. These parameters include metal lines and spacing, via diameter and capture-pad sizes, substrate-core thicknesses, multilayer advancements, metal-plating improvements, and solder-mask enhancements.

When using rigid laminate substrates for die stacking, several factors drive the need for and use of advanced technology rules that can ultimately drive up final substrate cost. With a good understanding of these design considerations and cost trade-offs, you can ultimately minimize the total package cost and bring it close to that of a single-die approach. Stacked-die-substrate designs with unique individual dice generally require increased routing density on the top metal layer of the substrate. You can control this increased trace density through a carefully managed co-design effort for each die in a stack. For example, with co-design, you might use the signal layout on one of the two dice as a foundation for die layout. In the best-case scenario, you can die-to-die wire-bond all of the same signals between dice, thus eliminating the need to use the substrate to interconnect the two dice. Ultimately, this approach enables the lowest cost substrate design and simplifies manufacturability when other key design factors are in place.

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As it becomes more difficult to directly bond stacked-die signals to each other, you may need additional bond fingers to relay a signal from one die to the other. Increased bond-finger density often implies increased substrate cost. In addition, you may be able to use a smaller diameter wire. This approach will increase resistance per millimeter run of wire and tighten overall wire-length constraints. For designs in which having multiple rows of bond fingers is not feasible, designers must consider the effects of narrower finger pitch on substrate cost, wire size, wire length, and wire electrical effects.

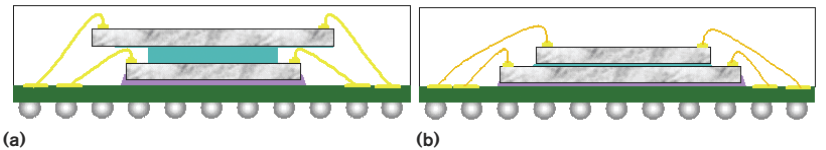

Figure 4 When the performance of the smaller die is important, the same-size stacking option (a) gives better performance than the pyramid-stacking option (b).

DIE-STACKING SEQUENCE

When stacking two die of approximately the same size, you might use a spacer to avoid interference between the top die and wires on the bottom die. However, the die-stacking sequence in-

volves trade-offs. First, when you place the die with significantly more wires on the bottom of the stack and place its associated bonding fingers in the inner row, you can expect small bonding-finger pitch. On the other hand, when you place the die with significantly fewer wires on the bottom, you can expect greater bonding-finger pitch because the bond fingers for the die with denser wires are in the outer row, which allows placing bond fingers at a more desirable larger pitch (**Figure 5**).

Overall, S-CSP-design approaches maximize yield, performance, and reliability and minimize cost. These approaches include choosing conventional wire bonding over SSB, optimizing substrate-bond-finger placement to minimize wire length and reduce the risk of wire sweep, and reducing the risk of wire shorts by moving wire-crossing points to the midspan of upper tier wires. These approaches also include optimizing critical nets before routing other nets, avoiding capillary interferences with adjacent wires, placing higher performance die at the bottom of a stack, and placing die with fewer wires at the bottom to allow greater bond-finger pitch and lower substrate costs. EDN

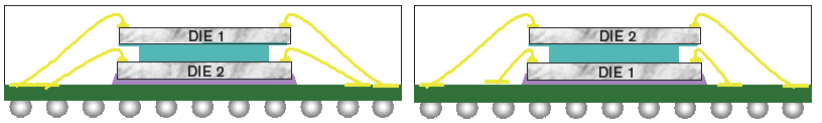

Figure 5 Die 1 requires significantly fewer wires than Die 2. Placing Die 2 on the bottom (a) results in smaller bond-finger pitch, but placing Die 1 on the bottom results in a larger bond-finger pitch (b).

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