Circuitry for Single Cell Operation

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Portable, battery powered operation of electronic apparatus has become increasingly desirable. Medical, remote data acquisition, power monitoring and other applications are good candidates for battery operation. In some circumstances, due to space, power or reliability considerations, it is preferable to operate the circuitry from a single 1.5V cell. Unfortunately, a 1.5V supply eliminates almost all linear ICs as design candidates. In fact, the LM10 op amp-reference and the LT1017/LT1018 comparators are the only IC gain blocks fully specified for 1.5V operation. Further complications are presented by the 600mV drop of silicon transistors and diodes. This limitation consumes a substantial portion of available supply range, making circuit design difficult. Additionally, any circuit designed for 1.5V operation must function at end-of-life battery voltage, typically 1.3V. (See Box Section, "Components For 1.5V Operation.")

These restrictions are painful, especially if complex linear circuit functions such as data converters and sample-holds are needed. Despite the problems, designing such circuits is possible by combining considerable attention to component characteristics with unusual circuit methods.

10kHz V→F Converter

Figure 1, an example of this approach, is a complete 1.5V powered 10kHz V→F converter. A 0-1V input produces a 25Hz to 10kHz output, with a transfer linearity of 0.35%. Gain drift is 250ppm/°C and current consumption about 205μA.

To understand circuit operation, assume C1's positive input is slightly below it's negative input (C2's output is low).

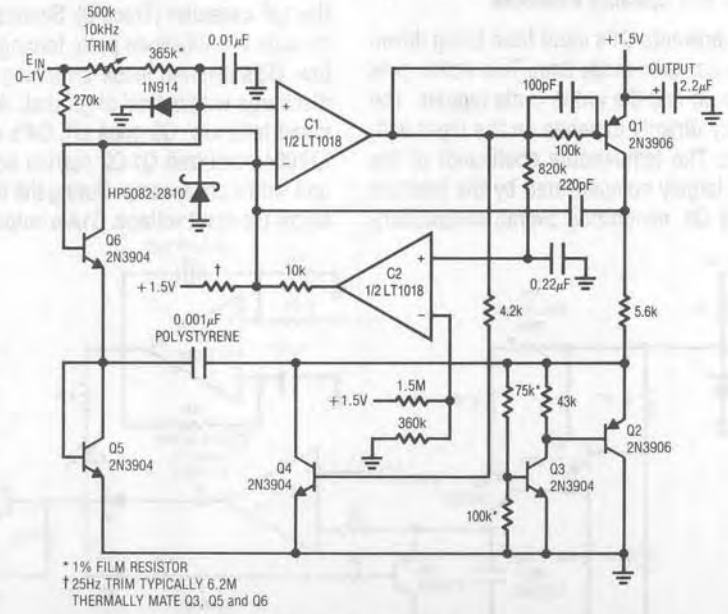

Figure 1. 10kHz V→F Converter

The input voltage causes a positive going ramp at C1's positive input (Trace A, Figure 2). C1's output (Trace B) is low, biasing Q1 on. Q1's collector current drives the Q2-Q3 combination, forcing Q2's emitter (Trace C) to clamp at 1V. The 0.001μF capacitor charges to ground (0.001μF unit's current waveform is Trace D) via Q5. When the ramp at C1's positive input goes high enough, C1's output goes high, cutting off Q1, Q2 and Q3. Q4 conducts, pulling current from C1's positive input capacitor via Q6. This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output low. The 100pF capacitor at Q1's collector furnishes AC positive feedback, ensuring that C1's output remains positive long enough for a complete discharge of the 0.001μF capacitor.

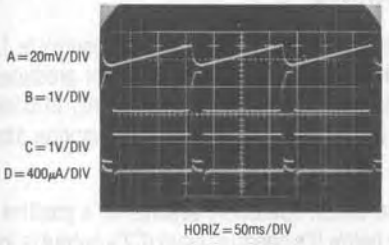

Figure 2. V–F Operating Waveforms

The Schottky diode prevents C1's input from being driven outside its negative common-mode limit. This action cuts off Q4, Q1-Q3 come on and the entire cycle repeats. The oscillation frequency directly depends on the input voltage derived current. The temperature coefficient of the Q2-Q3 1V clamp is largely compensated by the junction tempcos of Q5 and Q6, minimizing overall temperature drift. The 270kΩ resistor path provides an input voltage derived trip point for C1, enhancing circuit linearity performance. This resistor should be selected to achieve the quoted linearity.

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback loop to latch. If this occurs, C1's output goes high. C2 detects this, via the 820k-0.22μF lag, and also goes high, lifting C1's negative input towards +1.5V. Because C1's positive input is diode clamped at 600mV, its output switches low, initiating normal circuit behavior.

To calibrate this circuit, select the 100k value for V_{CLAMP} = 1V. Next, apply 2.5mV at the input and select the resistor value indicated at C1's input for a 25Hz output. Then, put in exactly 1V and trim the 500kΩ potentiometer for 10kHz output.

10 Bit A→D Converter

Figure 3 is another data converter circuit. This integrating A→D converter has a 60ms conversion time, consumes 460μA from its 1.5V supply and maintains 10 bit accuracy over a 15°C to 35°C temperature range.

A pulse applied to the convert command line (Trace A, Figure 4) causes Q3, operating in inverted mode, to discharge the 1μF capacitor (Trace B). Simultaneously, Q4 is biased through the 10k-diode path, forcing its collector (Trace D) low. Q3's inverted mode switching results in a capacitor discharge within 1mV of ground. When the convert command falls low, Q3 goes off, Q4's collector lifts, and the LT1004 stabilized Q1-Q2 current source charges the 1μF unit with a linear ramp. During the time the ramps value is below the input voltage, C1A's output is low (Trace C). This

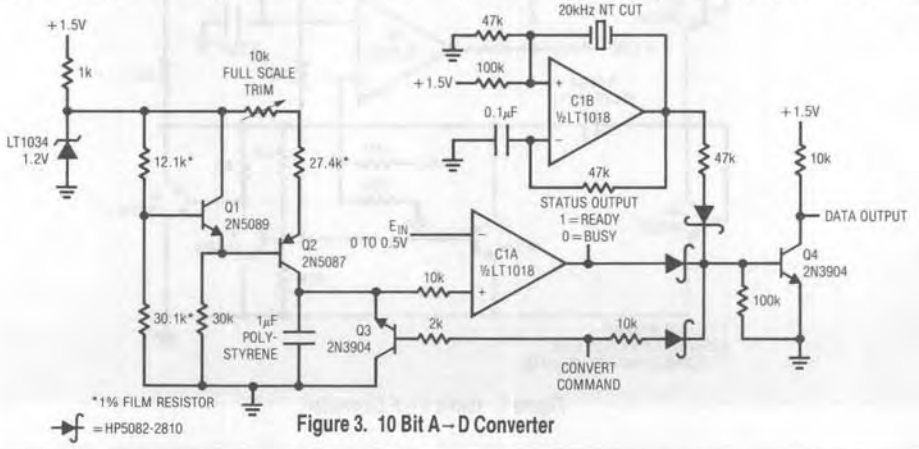

Figure 3. 10 Bit A→D Converter

allows pulses from C1B, a quartz stabilized oscillator, to modulate Q4. Output data appears at Q4's collector (Trace D). When the ramp crosses the input voltages value C1A's output goes high, biasing Q4 and output data ceases. The number of pulses appearing at the output is directly proportional to the input voltage. To calibrate this circuit apply 0.5000V to the input and trim the 10k potentiometer for exactly 1000 pulses out each time the convert command line is pulsed. No zero trim is required, although Q3's inverted 1mV saturation voltage limits zero resolution to 2 LSBs.

Sample-Hold Amplifier

A logical companion to the A–D converter described is a sample-hold amplifier. A sample-hold is one of the most difficult circuits to design for 1.5V operation, primarily because FET switches with low enough pinch-off voltages are not available. Two methods are presented here. The first circuit gets around the switch problem with an approach that eliminates the switch. Although an unusual way to implement a sample-hold, it requires no special components or trimming, is easy to build and has a 4ms acquisition time to 0.1%. The second circuit, a more conventional design, requires specially selected and matched components and is more complex, but offers 125μs (0.1%) acquisition time—a 30× improvement over the other design.

When a sample command (Figure 5, Trace A) is applied to the circuit of Figure 6, Q1, operating in inverting mode, discharges the 1μF capacitor (Trace C). When the sample command falls, Q1 goes off and C1A's internal output pull-up current source (Trace B) charges the capacitor via Q2, connected as a low leakage diode. The capacitors charging ramp is followed by the LM10, which biases C1B's positive input. When the ramp potential crosses the circuit's input voltage, applied to C1B's negative input, C1B's output goes high (Trace D).

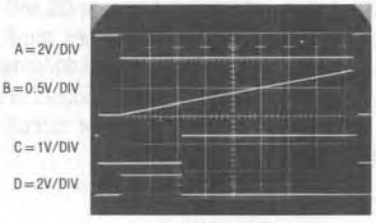

Figure 4. A–D Converter Waveforms

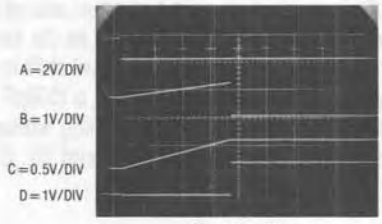

Figure 5. Sample-Hold Waveforms

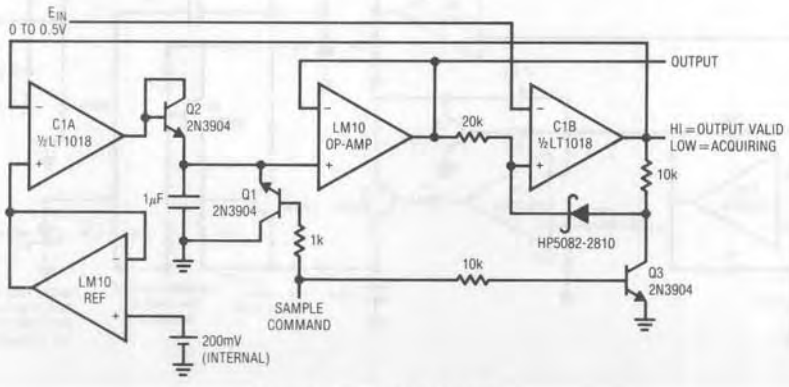

Figure 6. Sample-Hold Circuit

This forces C1A's output low, and the 1μF capacitor stops charging. Under these conditions, the circuit is in the "hold" mode. The voltage the capacitor sits at is the same as the input voltage, and the circuit output is taken at the LM10. The 10k diode path at C1B provides a latch, preventing input voltage changes or noise from affecting the value stored in the 1μF capacitor. When the next sample command is received, Q3 breaks the latch and circuit action repeats.

Acquisition time is directly proportional to input value, with 4ms required for full-scale (0.5V). Although faster acquisition is possible, the delay in shutting off C1A's output will degrade accuracy. The circuits primary advantages are elimination of the FET switch requirement and relative simplicity. Accuracy is 0.1%, droop rate specs at 10μV/ms and current consumption is 350μA.

Fast Sample-Hold Amplifier

Figure 7, a more conventional approach to a sample-hold, is significantly faster, but also more complex and has special construction requirements. Q1 serves as the sample-hold switch, with Q6 and Q7 providing a level shift to drive the gate. To minimize power consumption, a 1500pF feedforward path is used for fast gate switching without resorting to high operating currents in Q6 and Q7. C1A, a simple squarewave oscillator, drives Q4. C1B inverts C1A's output and biases Q5. The transistors serve as synchronous switches and charge is pumped to the 2.2μF capacitor at Q5's collector, resulting in a negative potential there.

Q1's low pinch-off voltage is obtained at the expense of on resistance. The typical R_{ON} of 1.5-2kΩ means the circuit's hold capacitor must be small if fast acquisition is desired. This mandates a low bias current output amplifier, or droop rate will suffer. Q2, Q3 and A2 meet this need. Q2 and Q3 are set up as source followers, with the resistors used as level shifters to keep A2's inputs inside the LM10's common-mode range. A2's output diode ensures clean dynamic performance for voltages close to zero by setting the LM10's output bias point well above ground. The 180pF capacitor compensates the composite amplifier.

Several special considerations are required to use this circuit. Q1, an extremely low pinch-off device, must be further selected for a pinch-off below 500mV to enable proper turn-off. Also, any V_{GS} mismatch between Q2 and Q3 will contribute offset error, and these devices must be selected for V_{GS} matching within 500μV. Additionally, the Q2-Q3 V_{GS} absolute value must be inside 500mV or A2 may encounter common-mode limitations for circuit inputs near full-scale.

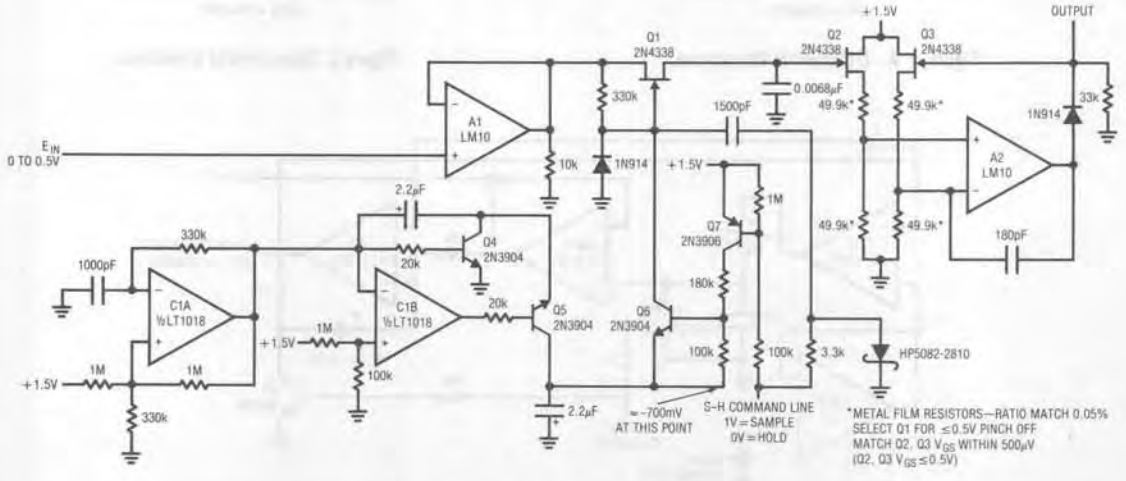

Figure 7. Fast Sample-Hold

Finally, mismatches in the resistor level shift contribute a gain error. To hold 0.1% circuit accuracy, the resistors should be ratio matched within 0.05%.

Once these special provisions have been attended to, the circuit delivers excellent specifications for a 1.5V powered sample-hold. Acquisition time is 125μs to 0.1% with a droop rate of 10μV/ms. Current consumption is inside 700μA.

Figure 8 shows the circuit acquiring a full-scale input. Trace A is the sample-hold command, while Trace B is the circuit's output. Trace C, an amplitude expanded version of B, shows acquisition detail. The input is acquired within 125μs and sample-to-hold offset is within a millivolt.

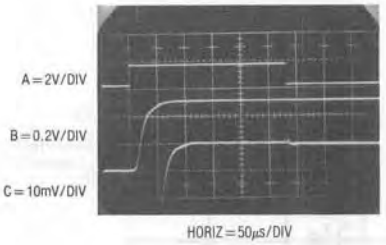

Figure 8. Fast Sample-Hold Waveforms

Temperature Compensated Crystal Clock

Many systems require a stable clock source and crystal oscillators which run from 1.5V are relatively easy to construct. However, if good stability over temperature is required, things become more difficult. Ovenizing the crystal is one approach, but power consumption is excessive. An alternate method provides open loop, frequency correcting bias to the oscillator. The bias value is determined by absolute temperature. In this fashion, the oscillator's thermal drift, which is repeatable, is corrected. The simplest way to do this is by slightly varying the crystal's resonance point with a variable shunt or series impedance. Varactor diodes, the capacitance of which varies with reverse voltage, are commonly employed for this purpose. Unfortunately, these diodes require volts of reverse bias to generate significant capacitance shift, making direct 1.5V powered operation impossible.

Figure 9's circuit accomplishes the temperature compensation function. The transistor and associated components form a Colpitts class oscillator which runs directly from the 1.5V supply. The varactor diode, in series with the crystal, tunes oscillator frequency as its DC bias varies. An ambient temperature dependent DC bias is generated by the remaining circuitry.

The thermistor network and the LM10 amplifier are arranged to produce a temperature dependent signal which corrects the thermal drift of the crystal type specified. Normally, the 1.5V powered LM10 could not provide the output levels required to bias the varactor. Here, however, a self-exciting switching up-converter (T1 and associated components) is included in the LM10's feedback loop. The LM10 drives the switching converter's input to generate whatever output voltage is required to close the loop. The thermistor-bridge network and amplifier feedback resistor values are scaled to produce appropriate temperature dependent varactor bias. The LM10's reference portion stabilizes the temperature network against 1.5V supply variations. The 100pF positive feedback forces the LM10's output into switched mode operation, conserving power.

Figure 10 plots compensated versus uncompensated oscillator drift. The compensation improves drift performance by more than a factor of ten. The residual aberrance in the compensated curve is due to the first-order linear correction used. Current consumption is inside 850μA.

Voltage Boosted Output Amplifier

In many circumstances, it is desirable to have 1.5V powered circuitry interface to higher voltage systems. The most obvious example is 1.5V driven, remote data acquisition apparatus which feeds a line-powered data gathering point. Although the battery powered portion may locally process signals with 1.5V circuitry, it is useful to address the monitoring high level instrumentation at high voltage.

Figure 11's design borrows from the method used in Figure 9 to generate high voltage outputs. This 1.5V powered amplifier provides 0-10V outputs at up to 75μA capacity. The LM10 drives the self-exciting up-converter with whatever energy is required to close the feedback loop. In this case, the amplifier is set-up with a gain of 101, although other gains are easily realized. The sole restriction is that

the 1.5V powered LM10's common-mode input range not be exceeded. The Schottky diode bypasses the up-converter for low voltage outputs, aiding output noise performance. Overlap between the up-converters turn-on threshold and the diode forward breakdown ensures clean dynamic behavior at the transition point. To increase efficiency the 0.033μF capacitor provides AC positive feedback, forcing the LM10 output to pulse-width modulate the up-converter.

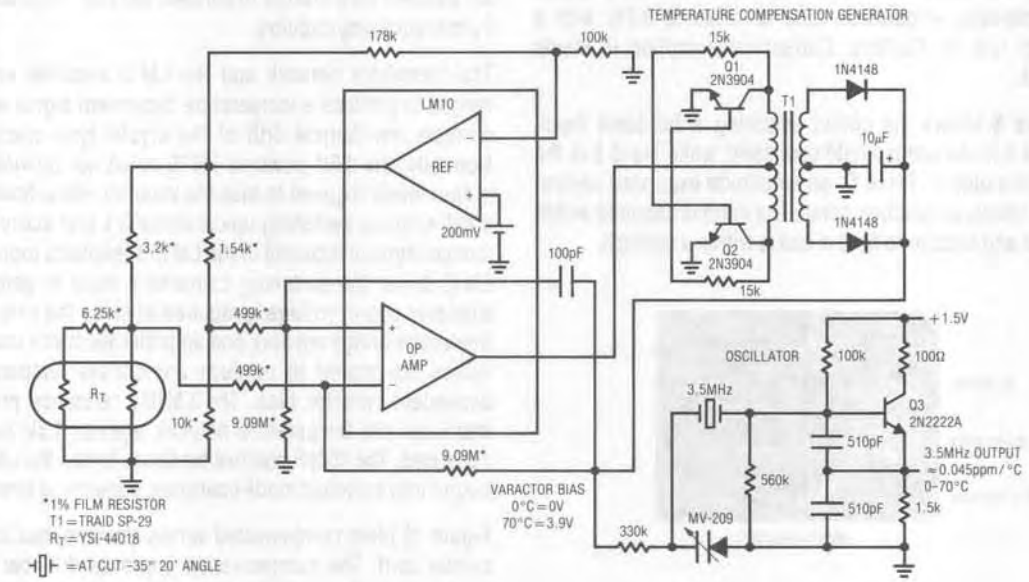

Figure 9. Temperature Compensated Crystal Oscillator

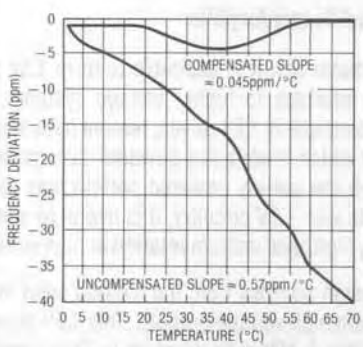

Figure 10. Compensated vs Uncompensated Oscillator Results

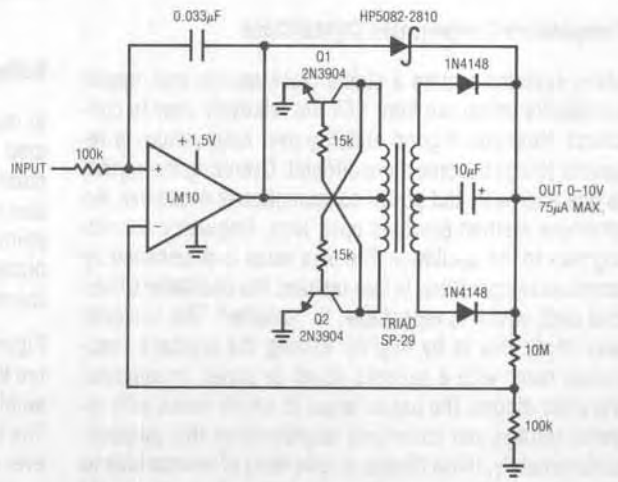

Figure 11. Voltage Boosted Output Op-Amp

Figure 12 details operation. The circuit's output (Trace A) decays until the LM10 switches (Trace B), starting the up-converter. The two transistors alternately drive the transformer (transistor collectors are Traces C and D) until the output voltage rises high enough to shut-off the LM10 output. This sequence repeats, with repetition rate dependent upon output voltage and loading conditions.

5V Output Switching Regulator

No commercially available logic, processor or memory family will operate from 1.5V. Many of the circuits described previously normally work in logic driven systems. Because of this, a way to permit use of standard logic functions from a 1.5V battery is necessary. The simplest way to do this is a switching regulator specifically designed for 1.5V input operation. Figure 13's flyback configuration, a variant of a design by R. J. Widlar, gives a 5V output. C1A serves as an oscillator, providing a ramp (Trace A, Figure 14) at C1B's DC biased negative input. C1B compares a divided version of the output to a reference point derived from the LT1034. The ramp signal, summed with the reference point, causes C1B's output to width modulate (Trace B). During the time C1B is low, current builds in its output inductor (Trace C). When the ramp at C1B goes low enough, C1B's output goes high, and the inductor discharges into the 47μF capacitor. The diode from C1A's output to C1B's positive input supplies a pulse (Trace D) on each oscillator cycle, ensuring loop start up.

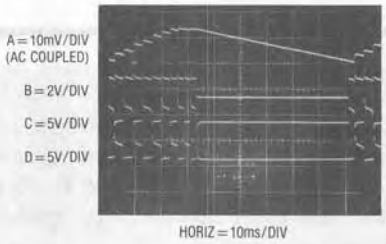

Figure 12. Boosted Op-Amp Waveforms

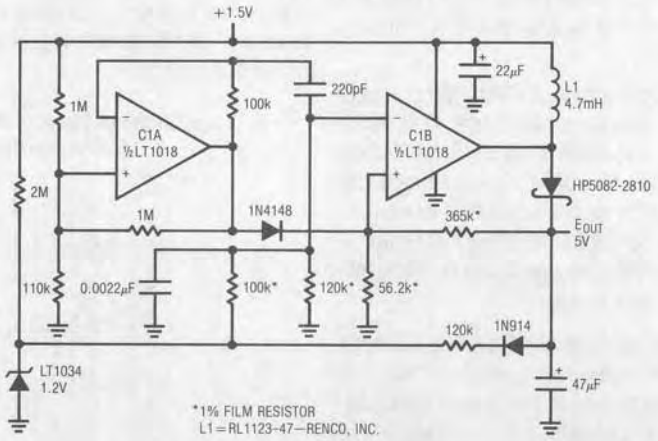

Figure 13. Flyback Regulator

The 120kΩ diode path from the output bootstraps LT1034 bias, aiding overall regulation.

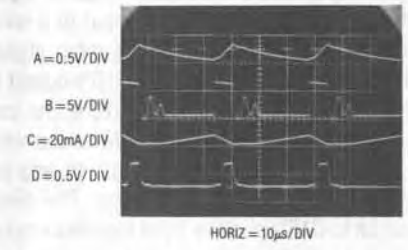

Figure 14. Flyback Regulator Waveforms

Figure 15 plots regulator efficiency. Small loads produce lowest efficiency because of fixed losses in the regulator, although 80% efficiency is achieved above 1500μA.

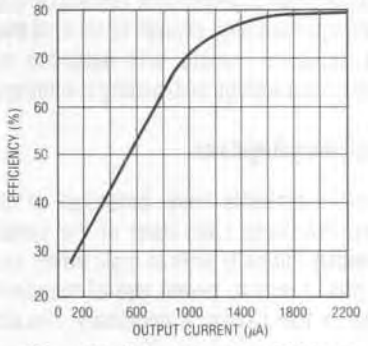

Figure 15. Flyback Regulator Efficiency

Components for 1.5V Operation

Almost all commercially available linear ICs are not capable of 1.5V operation. Two that are capable include the LM10 and LT1017/LT1018. The LM10 op amp-reference runs as low as 1.1V; the LT1017/LT1018 comparator goes down to 1.2V. The LM10 provides good DC input characteristics, although speed is limited to 0.1V/μs. The LT1017/LT1018 comparator series features microsecond range response time, high gain and good DC characteristics. Both devices feature low power consumption. The LT1004 and LT1034 voltage references feature 20μA operating currents and 1.2V operation.

Standard PN junction diodes have a 600mV drop, a substantial percentage of available supply range. At currents below 10-20μA, this figure reduces to about 450mV. Schottky diodes typically exhibit only 300mV drop, although reverse leakage is higher than standard diodes. Germanium diodes are lowest, with 150-200mV drop, even at relatively high currents. Often, though, the significant reverse leakage of Germanium precludes its use.

Standard silicon transistors have a 600mV V_{BE}, although this figure comes down somewhat at very low base currents. The V_{CE} saturation of silicon transistors is well below 100mV at reasonable currents, and judicious device selection and use can reduce this figure below 25mV. Inverted mode operation allows V_{CE} saturation losses below 1mV, although beta is often below 0.1, necessitating substantial base drive. Germanium transistors have 2-3 times lower V_{BE} and V_{CE} losses, although speed, leakage and beta are generally not as good as silicon types.

Perhaps the most important component is the battery. Many types of cells are available, and the best choice varies with the application. Two common types are Carbon-Zinc and Mercury. Carbon-Zinc offers higher initial voltage, but Mercury units have a much flatter discharge curve (e.g., better supply regulation) if currents are controlled (see figure).

Typical Discharge Curves of Similar Size (AA) Mercury and Carbon Zinc Cells (1mA Load)