Analysis can take the heat off power semiconductors

Designing for thermal requirements with good electrical isolation ensures stability and reliable performance of these devices

by Forest B. Golden, *General Electric Co., Auburn, N. Y.*

☐ Cost-conscious design engineers, well aware that a 1% component-failure rate during the warranty period can easily add 50 cents to a product's cost, are eager to reduce device temperatures. To put it simply, the cooler a device operates, the more reliable it is. Generally, if an engineer can lower its temperature by 20%, he will reduce the device's failure rate by a factor of three. This concept applies to such discrete devices as the power transistor, diode power rectifier, and thyristor family, which includes the silicon-controlled rectifier and the triac.

Thus, keeping semiconductors cool, while often thought of as a necessary evil and a chore to the design engineer, is really an intimate part of the design process. It is not enough for the designer merely to select a device that meets circuit requirements. He must follow up with a systematic thermal analysis to enable him to select a heat sink and mounting technique that will hold device temperature low and thereby assure reliable operation for a long time.

These factors should be considered in making the thermal analysis:

- Determine power dissipation and temperature limits so that the case-to-ambient thermal resistance can be calculated and the proper heat-transfer techniques selected.
- Evaluate electrical-isolation requirements of the device package.
- Ensure that the thermal resistance of the device interface is minimal.
- Verify the calculations by careful temperature measurements under operating conditions.

The thermal circuit

Semiconductor-design engineers learned early to translate heat-transfer units to understandable circuit units—watts for heat and degrees per watt for thermal resistance. Thermal resistance—the inverse of thermal conductance—is the key to selection of the cooling hardware, such as a heat sink, for a semiconductor device.

A thermal circuit (Fig. 1) includes thermal capacitor elements to account for thermal storage. However, since power dissipation of most device designs can be calculated as rms values, thermal capacitance can usually be ignored.

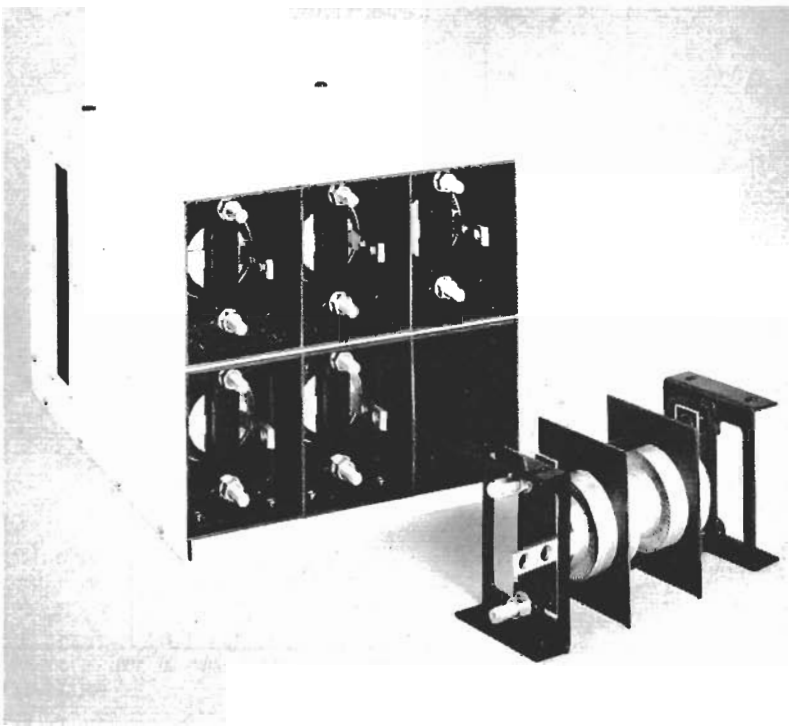
The thermal equation resembles Ohm's law because heat in watts is analogous to electrical current, and temperature difference is comparable to potential difference:

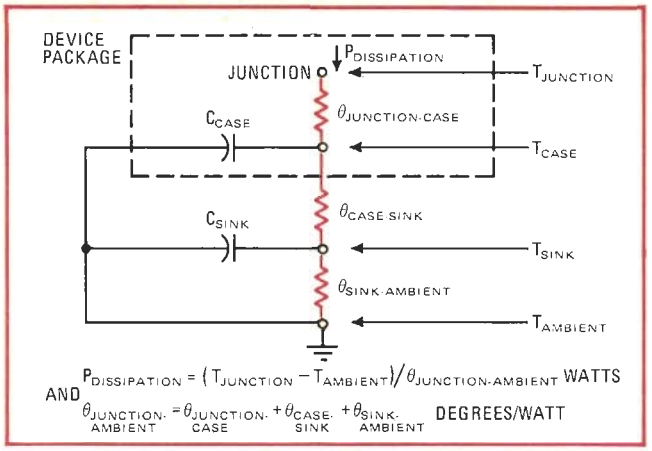
$$\theta_{JA} = (T_J - T_A)/P_D$$

where θ_{JA} is the thermal resistance of the junction in degrees per watt, T_J is the temperature of the semiconductor junction, T_A is the temperature of the ambient, and P_D is the power dissipation in watts.

To calculate the all-important thermal resistance—from junction to ambient—the designer must determine three thermal parameters: the maximum allowable

Kilowatt cooler. This cooling package is typical of some of the highly efficient thermal packages recently developed to cool power-semiconductor rectifiers and SCRs. The enclosure, developed by Thermalloy, is 13 inches high, 14 in. wide and 16 in. deep. It can dissipate approximately 3.5 kilowatts. Devices shown are three-phase full-wave rectifiers that can handle 1,000 amperes. Each of the six modules provides a thermal resistance of 0.07°C/watt from sink to air. Assembly requires 300 cubic feet per minute of air at a pressure drop of 0.9 in. of water to achieve this low thermal resistance.





1. Thermal circuit. Circuit analogs enable the designer to analyze the thermal paths. Resistors represent the thermal resistivities of the various components. Capacitors account for storage capabilities, but are usually omitted in steady-state calculations.

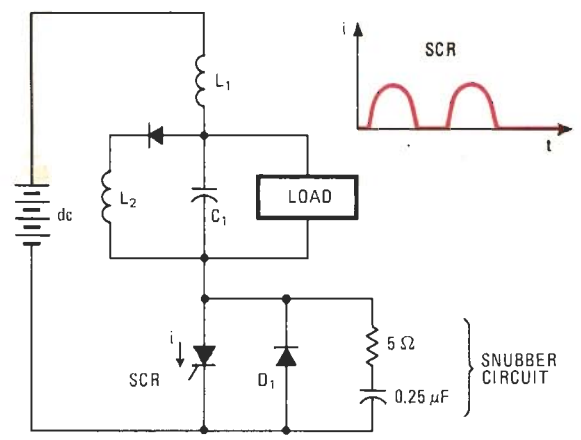
temperature of the semiconductor junction, the maximum ambient temperature, and the maximum power that the device will dissipate.

Applying thermal parameters

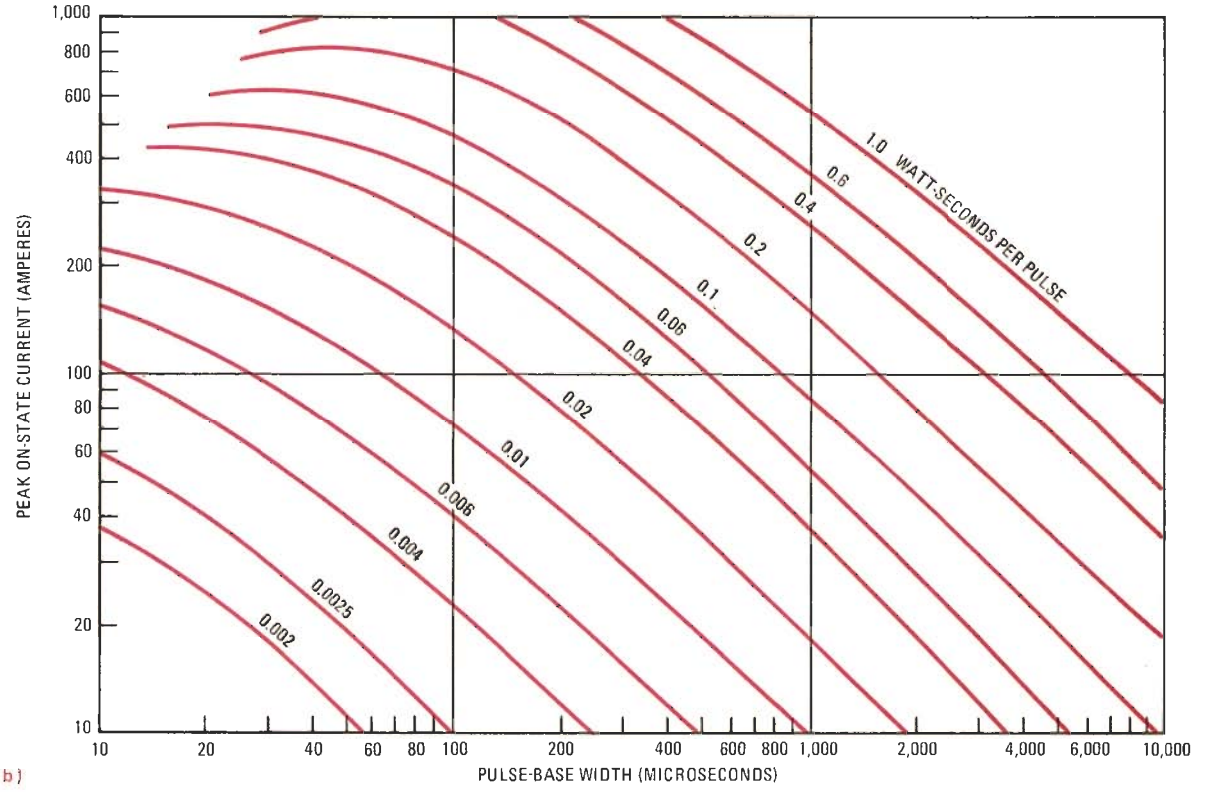
Determining the power dissipation of a thyristor or a semiconductor rectifier is not difficult because worst-case values are specified by manufacturers' data sheets. Application of this data is illustrated by calculation of dissipation for a high-frequency inverter circuit to be used in pulse operation. The term inverter applies to a circuit that converts dc to a periodic waveform. The inverter circuit (Fig. 2a) develops a near-sinusoidal current through the SCR. A typical rating curve for such an SCR (Fig. 2b) provides the maximum watt-second loss per pulse for any sinusoidal pulse the SCR can handle.

The worst-case anode-power dissipation is determined by multiplying the repetition rate by the watt-second loss per pulse. This value will be accurate if the values of the gate drive and snubber circuit are comparable to those specified in the data sheets. (A snubber circuit is a low-pass-filter network that prevents spurious thyristor triggering.)

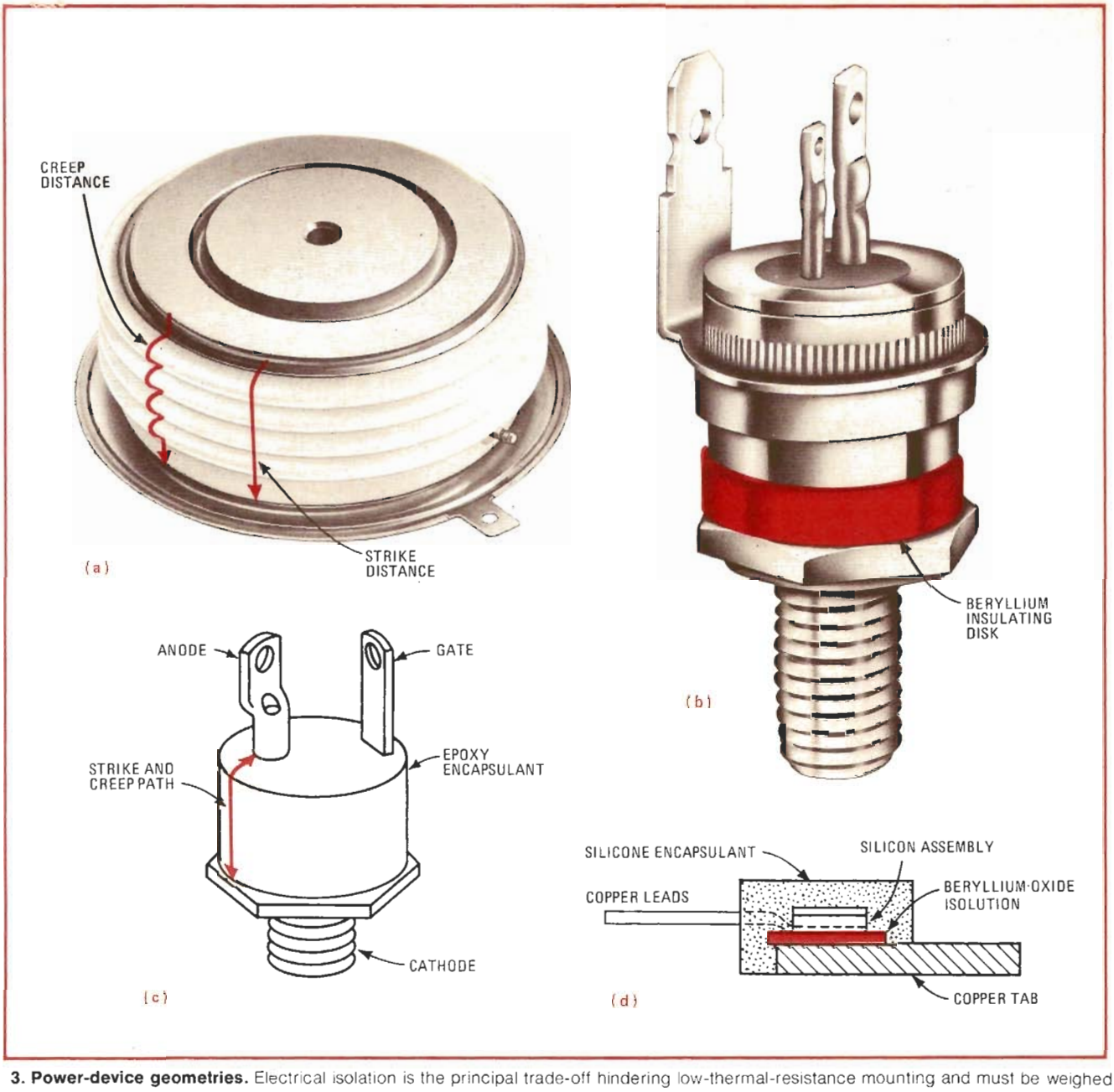
2. Pulse power. The inverter circuit (a) delivers a near-sinusoidal-shape pulse current through the SCR. Curves in (b) provide the watt-second power loss per pulse. Multiplying this value by the pulse-repetition rate yields the power dissipation.



(a)



(b)



3. Power-device geometries. Electrical isolation is the principal trade-off hindering low-thermal-resistance mounting and must be weighed against the thermal resistance values in manufacturers' data sheets. The designers of the pressure-mounted disk in (a) assure adequate creep and strike distances by ribbing the surface. Thickness is 26 mm. Device can operate at 480 volts rms, and current-handling ability exceeds 500 amperes. Such devices as the stud-mounted unit shown in (b) pose an electrical-isolation problem because thickening the ceramic or increasing the diameter of the ceramic increases the thermal resistance on one hand and develops an interference with the hex-shaped base on the other. Adding an encapsulant to a stud-mounted device (c) greatly enlarges creep and strike distances required to meet NEMA and U/L requirements. By putting a thin beryllium-oxide insulator within the TO-220 package (d), electrical isolation can be obtained at minimal thermal expense. Designer can then attach the copper tab to a mounting surface with good thermal properties, thus doing away with the added cost of purchasing and mounting an independent heat sink.

However, determining dissipation data for switching transistors is considerably more difficult because the required data is seldom available. As a result, the designer has no choice but to determine the wave shapes and amplitudes of the collector-to-emitter voltages and currents, develop graphic plots of the product, and then integrate over an operating cycle to arrive at the rms power dissipated.

To ensure an accurate evaluation, these guidelines should be followed:

- Assume worst-case parameters—that is, figure on maximum voltage and current, lowest and slowest drive conditions, stiffest snubber networks, and highest frequency of operation.
- Include all power components, notably base power and blocking power.
- Test a number of devices to calculate a worst-case figure.
- To avoid measurement error caused by inductive shunting in high-frequency drive circuits, use a coaxial-

Thermal runaway

It is commonly believed that if the duty cycle of a semiconductor device is low, a heat sink is not required. But this dictum simply isn't true. Because semiconductor blocking characteristics are highly temperature-dependent, thermal runaway can develop. Blocking current is the current that flows during the off portion of the duty cycle, and, despite the fact that it may be no more than microamperes, it can contribute to a runaway condition. Runaway describes the positive-feedback chain reaction in which temperature rise causes a temperature-dependent current to increase. This, in turn, further heats the device to cause a still larger current. If unchecked, the current increases until the device destroys itself.

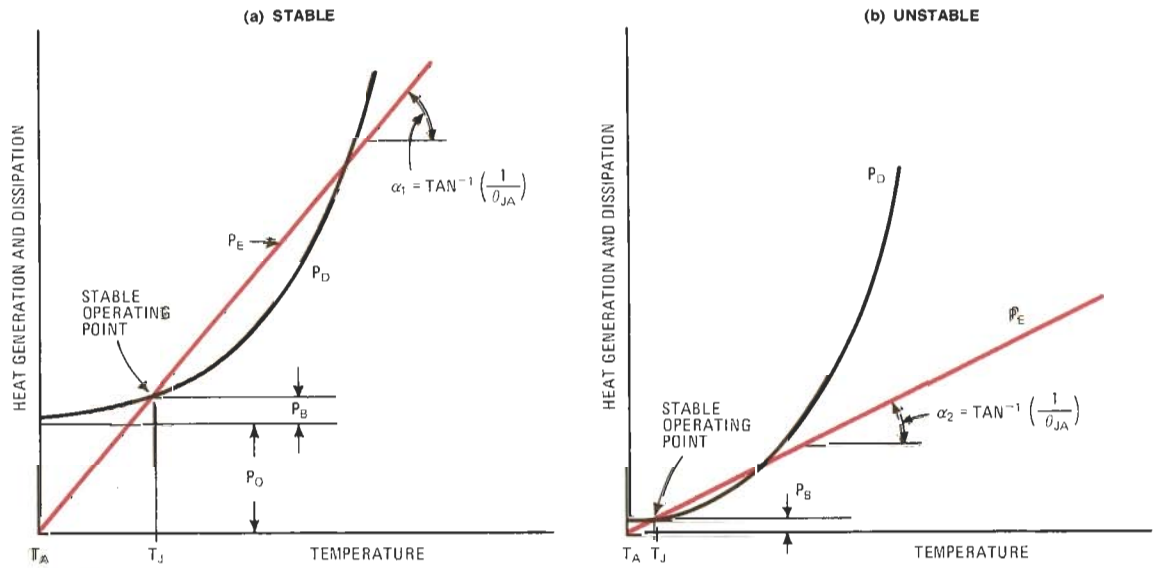
As an example, the peak off-state current (I_{DRM}) of a thyristor doubles for every 10°C rise in junction temperature. This doubling in current means a doubling of blocking-power loss (P_B). Such an increase under adverse temperature conditions can lead to a runaway that culminates in catastrophic failure.

Stability is not solely a function of blocking current; it is also highly dependent on the thermal resistivity of the entire junction-to-ambient path. Thus, a low-resistance heat sink can play a crucial role in assuring stable operation.

The plots below depict both stable and unstable device operation. In each case, the thermal resistivity is superimposed on the power-dissipation curve for the device. In (a), a stable thermal situation is depicted. It is stable because the dissipation capability of the over-all thermal path (P_E)—including the sink and interface—exceeds the power developed (P_D), which is the sum of the on-state conducting losses (P_O) and the off-state blocking losses (P_B). If the ambient temperature were to rise, the (P_E) line would shift slightly to the right, but, since this line would still lie above and to the left of the P_D curve, operation would remain stable. The reason is that the dissipation capability (P_E) still exceeds the power dissipated (P_D). Note that, for stable operation, the blocking losses (P_B) are assumed to be only a small percentage of the total losses (P_O and P_B). However, in such low-duty-cycle operation as a crowbar circuit, the exact opposite may be true. That is, the on-state losses may be negligible, compared to the blocking losses.

Now, suppose a designer attempts to mount a semiconductor on a bracket that has a high thermal resistance and he makes no attempt to enhance the thermal circuit with a heat sink. This situation is depicted graphically in the unstable plot. Because of the high thermal resistance, the power-dissipation curve has a much lower slope (α_2). The designer might assume that the thermal requirement is ample because the operating temperature is lower. However, a small upward shift in the ambient temperature will shift the entire (P_E) line to the right and beyond the (P_D) plot. If this happens, the device dissipation exceeds the dissipation capability of the system, and runaway develops; that is, temperature and current rise until catastrophic failure occurs.

The prudent design engineer will want to adhere closely to the guidance contained in the data sheets for each device regarding maximum thermal case-to-ambient resistance ($\theta_{C\text{-}A}$), for which maximum blocking ratings apply. If such data is not specified, the designer should consult the device manufacturer.

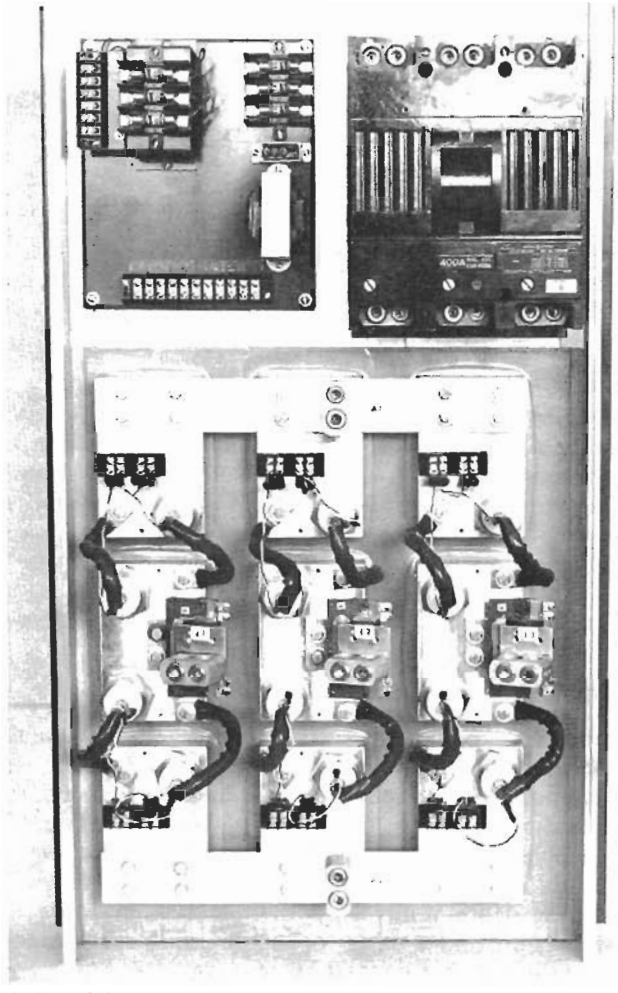


current shunt or a quality current-measuring device that has adequate bandwidth.

Worst-case junction and ambient temperatures should be found. The maximum junction temperature, shown on the device's data sheet, should not be exceeded, except where such other parameters as transistor collector-to-base voltage or thyristor anode-to-cathode voltage can be lowered, thereby raising the limit of the junction temperature.

This method of derating makes possible low-voltage SCRs having a junction temperature of 150°C. The normal maximum is 125°C. To assure optimum reliability, design engineers will usually derate junction temperature according to a derating curve furnished by the manufacturers.

The ambient temperature may be specified in advance, or it may have to be determined. When equipment is enclosed in an unventilated cabinet, the ambient encountered by the semiconductor's heat sink may be considerably higher than the ambient outside of the



4. Big sink. Thyristors rated at 480 amperes rms are attached to large heat-spreader blocks, which are attached to the cabinet by an epoxy adhesive. The epoxy provides the required electrical isolation; yet, because of the large heat-transfer surface area, it does not materially hinder the thermal path to the equipment structure.

enclosure, so there is no substitute for careful temperature measurement inside the enclosure. Although papers have been published on the subject of determining ambient temperature inside of enclosures, these design guidelines produce only first-order approximations, rather than final design values.

Evaluating isolation requirements

After power and temperature values have been determined, the designer must examine carefully the system's electrical-isolation requirements. Generally, the shorter the thermal path, the better. However, the requirement for adequate electrical isolation is diametrically opposed—isolation requires a longer path.

The electrical path must be designed to prevent breakdown that might be caused by arc-over or current leakage along the surface between terminals. Sufficient air gap—known as strike distance—must be provided to prevent arcing, and a minimum surface-resistance path, called creep, must be provided between terminals by the intervening insulator surface.

Adequate electrical isolation for a large thyristor with a 500-A rms rating and up with a silicon-pellet diameter from 33 to 40 mm (Fig. 3a) is provided by designing it as a pressure-mounted disk package with a 26-mm height to prevent strike and ribbing the surface as shown to prevent creep. As indicated in Table 1, a package 26 mm thick has more than adequate creep and strike isolation for line voltages as high as 480 V rms.

A tougher problem is posed by stud-mounted semiconductors in the range of 1 A to 50 A (Fig. 3b). Problems develop if the dimensions are altered to improve the strike and creep distances because thickening the beryllium-oxide disk increases the thermal-path length, thereby raising the thermal resistance. And if the diameter of the disk is increased, it interferes with the hexagonal base.

One way to lengthen the creep and isolation distances is to add an epoxy encapsulant (Fig. 3c). The epoxy develops adequate creep and strike distances from both anode to cathode and anode to stud to permit operation at 230 V, which is adequate to qualify the device for approval by Underwriters' Laboratories.

However, electrical isolation inside the TO-220 package shown in Fig. 3 (d) is provided internally by inserting a beryllium-oxide layer between the chip and the copper tab. Thanks to low thermal resistivity, the beryllium-oxide provides a good thermal path for the heat to travel from the chip to the copper tab. Although the chip-insulator interface has a small area that tends to degrade the thermal path, that tendency is offset by making the insulator relatively thin. This is possible because electrical strike and creep requirements are greatly reduced by the protection of the semiconductor package.

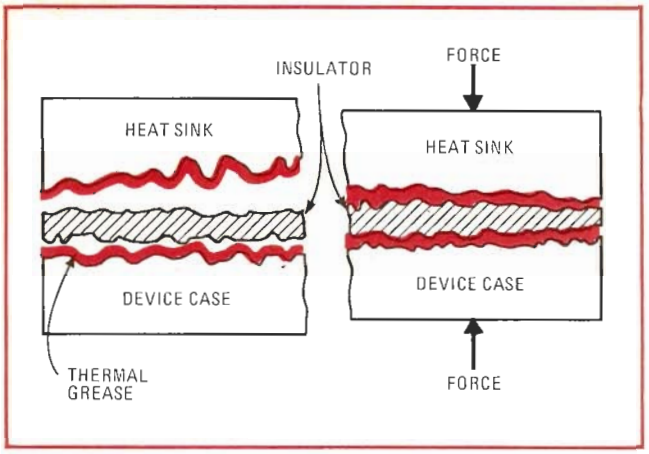
The result is roughly equivalent to the externally isolated package in respect to both electrical isolation and thermal dissipation. Because the copper tab is electrically isolated, the device can be mounted directly on an enclosure wall that can serve as the heat sink. Thus, the additional cost of a discrete heat sink can be eliminated, along with the additional labor required for its assembly.

Spreading heat through a sink is the only effective means that has been developed thus far to cope with the thermal requirements of high-current SCRs. Avtek Corp., Burlingame, Calif., has used this method to advantage (Fig. 4). The large 480-A rms thyristors are mounted on thick heat-spreader blocks that are at-

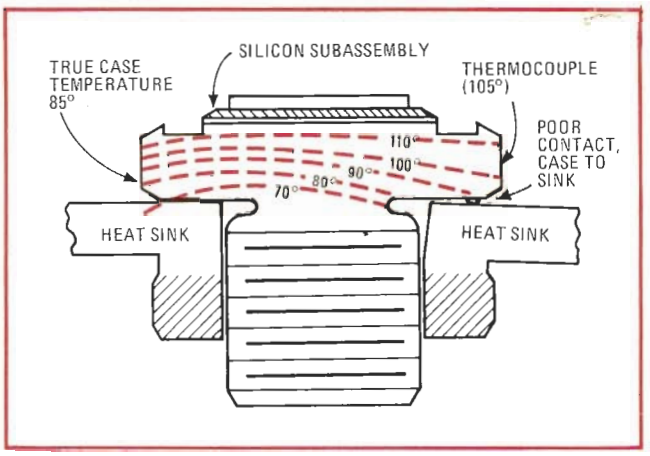
TABLE 1. STRIKE AND CREEP STANDARDS

Voltage (rms)		Distance (mm)	
		U.L.[1]	NEMA[2]
130	Strike	5.08	3.18
	Creep	6.35	6.35
240	Strike	7.62	6.35
	Creep	10.16	9.53
480	Strike	10.16	9.53
	Creep	12.7	12.7

Notes: 1. Proposed U.L. standard for appliance and consumer equipment – May 1973
2. Standards for semiconductor converters – Nov. 16, 1972



5. Mountainous. Exaggerated profile shows the thermal interfaces between a semiconductor device, an insulator, and the sink before and after engagement. Thermal grease helps to offset poor thermal path between materials that are microscopically rough.



6. Poor contact. If a device's contact heat sink isn't uniform, eccentric temperature profile develops, which cause erroneous temperature measurements. Mating surfaces must be smooth so that the thermal interface will be uniform about the device's circumference.

tached by epoxy to a common convection-cooled heat sink. This sink, in reality the rear portion of the equipment enclosure, also provides a mounting surface for the fuse blocks and circuit-breaker shown. The blocks enlarge the heat-transfer area and thus offset the high thermal resistance of the epoxy.

Knowledge of the thermal-resistance limit and the constraints imposed by electrical isolation equips the designer to select the heat sink and coolant requirements. However, he must also consider carefully the thermal resistance at the interface between the semiconductor device and the heat-exchanger hardware.

The interface

The interface between the semiconductor device and the heat sink is a crucial thermal path. If the interface's thermal resistance is too high, it can render worthless the heat-transfer capability of a good heat sink.

As an example, the thermal-resistance values for the 10-32-thread, stud-mounted device listed in Table 2 range from 0.09°C/W at best to 1.2°C/W at worst—a spread of more than a full order of magnitude. In fact, 1.2°C/W is a far greater thermal resistance than that provided by a good heat-exchanging system (see illustration, p. 106).

Figure 5 illustrates the profile of the mating surfaces making up a typical interface. The roughness of the surface has been exaggerated to dramatize the mechanics of the interface. Applying force to the surfaces brings them into contact, but the net contact area is highly dependent on the ductility of the contacting metals, the surface finish, and the flatness, as well as the amount of force applied. A large void (Fig. 5) can be caused by a non-parallel fit between the device case and the sink. Thermal grease can help fill that void. And, as indicated in Table 2, an insulator would raise thermal resistance.

Although semiconductor manufacturers' guidebooks provide specific instructions, these guidelines can serve for all but the largest pressure-mounted disk packages:

- Mating surfaces should be flat to within 0.001 inch, and surfaces should be finished to a tolerance of 63 microinches or less.
- All paint and other impurities should be removed completely by a treatment with #000 fine steel wool and silicone oil.
- The surfaces should be cleaned and wiped free of foreign matter immediately before assembly.

Measuring temperature

Initial calculations should be confirmed by actual temperature measurements. However, if results are to be meaningful, a number of pitfalls must be avoided. It is crucial to determine the actual power dissipation of the semiconductor because temperature data that overlooks this factor will lead to false calculations of thermal resistance. More is involved than merely inserting a thermocouple and waiting for the device to reach thermal equilibrium before taking a reading.

During the design and prototype stages, the designer should verify his calculations by measurements in the operating environment, according to these guidelines:

- The semiconductor device should be mounted on the heat sink in the actual enclosure intended to contain the manufactured version of the equipment. Merely rotating an air-cooled heat sink 90° can make a vast difference in its thermal properties.
- Follow manufacturer's mounting instructions carefully.
- Limit thermocouple wire diameter to 12 mils to avoid localized cooling.
- Avoid placing high-dissipation elements, such as ballast resistors and transformers, near a semiconductor. If this juxtaposition is unavoidable, make sure that both devices are dissipating their full design-power levels during temperature runs.
- Block off local air currents.
- Prevent direct sunlight from contributing to the heat measurement.
- Make sure that electromagnetic fields do not couple to thermocouple leads and destroy measurement accuracy.

Consider the problem involved in measuring the case temperature of a stud-mounted rectifier or SCR. Assume that the thermal resistance—junction-to-case—is specified at 0.3°C/W maximum and that the ambient temperature is 45°C. Assume further that the device-case

TABLE 2. SOME THERMAL INTERFACE RESISTANCES

Stud-mounted devices

Stud size	Hex size across flats or flat base (diameter)	Thermal resistance-case-to-sink θc-s °C/watt					
		With thermal grease			Dry		
		Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
10–32	7/16"	0.09	0.3	0.8	0.2	0.5	1.2
1/4"–28	9/16"	0.07	0.25	0.6	0.15	0.4	0.9
1/4"–28	11/16"	0.05	0.15	0.4	0.10	0.25	0.6
3/8"–24	1-1/16"	0.02	0.06	0.15	0.05	0.1	0.25
1/2"–20	1-1/16"	0.02	0.065	0.2	0.05	0.12	0.3
3/4"–16	1-1/4"	0.025	0.08	0.2	0.06	0.15	0.35
3/4"–16	1-5/8"	0.015	0.04	0.10	0.03	0.07	0.15
Flat Based	1-7/8"	0.01	0.025	0.07			
Stud-mounted devices insulated with 5-mil mica washer							
10–32	7/16"	1.2	2.5	4.5	—	—	—
1/4"–28	9/16"	0.9	2.0	3.5			
1/4"–28	11/16"	0.7	1.5	2.5			

Pressure-mounted disk packages — lubricated

Interface diameter (inches)	Nominal clamp force (lb)	Thermal resistance-case-to-sink θc-s °C/watt		
		Minimum	Nominal	Maximum
3/4	800	0.04	0.06	0.20
1	2300	0.02	0.03	0.10
1-1/4	2300	0.015	0.022	0.08
1-1/3	4000	0.014	0.02	0.07

temperature must not exceed 85°C, in accordance with the manufacturer's data sheet. This amounts to a power dissipation of:

$$P = (85°C - 45°C)/0.3°C/W = 133.4\ W$$

Assume that the case temperature is actually measured to be 80°C. At first glance, the device appears to be below its maximum temperature, and all appears to be well. However, if the true dissipated power during the temperature measurement is less than the 133.4-W value, the actual case-to-ambient temperature is, in fact, too high. To illustrate why, assume that the power actually dissipated during the temperature measurement is 110 W. Then:

$$\theta = (80°C - 45°C)/110\ W = 0.318°C/W$$

Therefore, at full rated power of 133.4 W, the true case temperature would be:

$$\begin{aligned} T_{case} &= (P \times \theta) + T_{ambient} \\ &= (133.4\ W \times 0.318°C/W) + 45°C \\ &= 88°C \end{aligned}$$

or 3°C above the maximum rated case temperature at full power dissipation.

To avoid this pitfall, the designer should make sure that the device is dissipating the maximum power during the temperature measurement. To do this, a direct current is applied to the device, and the junction dissipation is adjusted by controlling the volt-ampere product.

An alternative method is to obtain a limit cell from the device manufacturer. This device, selected for worst-case power dissipation, is suited for thermal evaluation because, under actual circuit-operating conditions, its power dissipation provides a worst-case power-dissipation value.

Another factor can inhibit accurate temperature evaluation. As shown in Fig. 6, a local interface distortion can create a path of high thermal resistance directly under the thermocouple, thereby generating a false reading. If the maximum rated power dissipation and the ambient are the same as in the previous example, but the measured case temperature is 105°C, it does not necessarily mean that the heat sink is defective. It may be the local interface distortion.

To avoid this possible error, it is a prudent technique to use two or three thermocouples and to mate the semiconductor device carefully to the heat-exchanging surface to assure a uniform interface having low thermal resistance. □