The stalling power supply

A few years ago, a co-worker complained that he didn't know how he was going to get his project, a radar processor, through qualification testing due to a power-supply problem. The system used two identical 5V, 300A power supplies in a shared configuration for redundancy and reliability, although either supply could handle the full load. During the prequalification testing in the lab, however, he noticed that the unit's LED indicated that one of the power supplies had shut off after a couple of minutes of operation and that the remaining power supply was carrying the full load. Although the system carried on without missing a beat, the team categorized this power-supply shutdown as a system failure.

After the power-supply vendor failed to duplicate the phenomenon at its facility, my co-worker referred the problem to a couple of power-supply engineers, who opined that the fault was with a poorly designed unit and that we would be better off going for a redesign. The program had neither the time nor the money to do this redesign. I was intrigued but first wanted to hedge my bets and asked the qualification-project engineer whether a hard failure in the power supply had occurred after the incident. He responded that no hard failure had occurred: "We just recycle power, and both power supplies come back up," he said. With that assurance, I offered to take a shot at the problem.

I instrumented and observed a power supply in the system—which, surprisingly, no one had done before. I noticed that the problem occurred once the processor applied the system clock, which phase-locked the switching frequency and caused an overvoltage in one or the other power supplies, causing it to shut down. Now that I understood more of the scenario, a trip to the vendor's site was in order. The vendor's engineer and I discussed the design. With no solutions, I recalled my bench-testing days and asked to witness an ATP (acceptance-test procedure). The technician set up a unit, and I witnessed him perform the ATP. Halfway through the test, the procedure called for applying a clock to the power supply and verifying normal operation. I noticed that, after applying the clock, the technician toggled a switch. When I asked him about it, the technician replied: "Sometimes, the clock application makes the unit latch off. I just recycle it at that point." Aha! We were able to duplicate the problem and then called the engineer over to observe the effect, which astonished him. He seemed genuinely unaware of what the technician was doing.

Schematic analysis showed that the clock input drove a PLL that free-runs in the absence of an input. Because the vendor had limited experience with PLLs, they accepted my offer of trying to solve the problem. We discovered that the power supply exhibited a frequency-to-voltage-converter effect from the input clock to the output voltage. We then discovered that the PLL was severely underdamped and would overshoot severely when we applied the input clock. We changed a couple of values and added an extra resistor in the PLL filter, damping the loop and reducing its speed to less than that of the power-supply voltage-control loop, which allowed the loop to remove the input-clock-frequency-induced changes.

We retrofitted two power supplies with these changes and put them into the qualification system. When the system applied the clock, both power-supply lights remained green, and all was well. For the cost of a couple of resistors and a capacitor, the power supplies passed qualification testing, and the production lot also operated satisfactorily. EDN

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