

Low-voltage reset operates below 2.7V

BOB KELLY, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

New personal digital assistants, pagers, and other battery-powered systems operate at or below 2.7V, but power-on resets with thresholds below 2.6V are not commonly available. You can resolve this problem using a circuit that combines a 1.2V reference and a micropower regulator (**Figure 1a**). IC₁ integrates these two functions in a tiny SOT-143 package. A power-on-reset function must become active before the supply voltage reaches its nominal value, and IC₁

operates properly for supply voltages above 1.21V.

The R₁/R₂ divider and internal 1.204V reference establish a threshold that determines when the circuit asserts an active-low at the output. For the values in the **figure**, this threshold is 2.25V (**Figure 1b**). IC₁ has an open-drain output, so R₃ and C₁ control the length of the active-low pulse, RESET. In this case, the pulse length, or reset interval, is approximately 54 msec, which is sufficient reset time for

most μCs and other digital circuits.

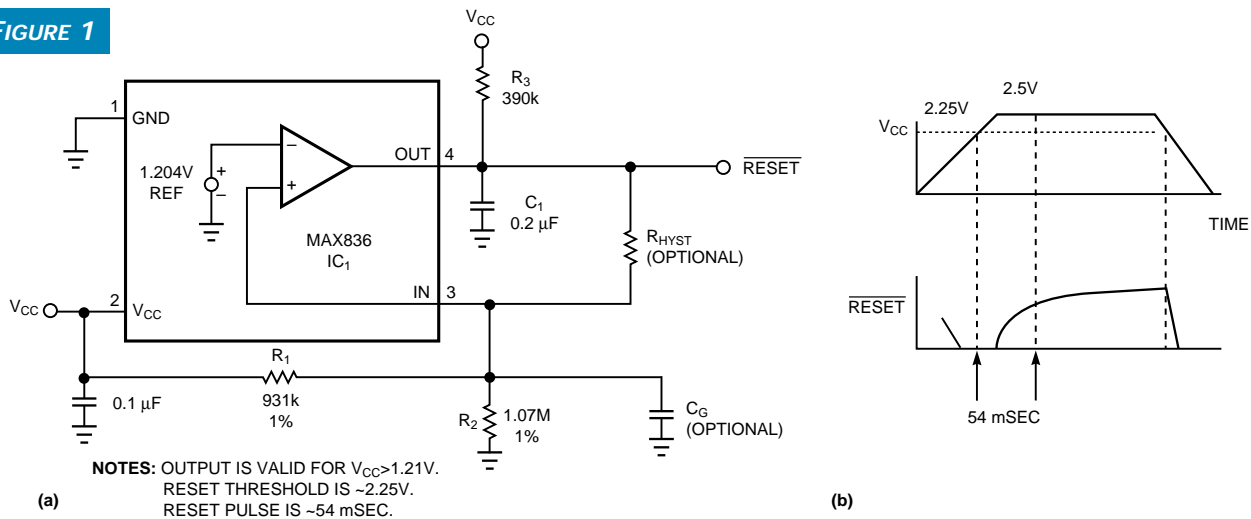
Low power consumption distinguishes this circuit. The IC typically draws only $5\ \mu\text{A}$, and the R_1/R_2 divider draws slightly more than $1\ \mu\text{A}$ in a 2.7V application. Pullup resistor R_3 consumes power only when the supply voltage droops out of tolerance, so the power loss is minimal in normal operation.

To prevent erratic behavior, IC_1 offers approximately $6\ \text{mV}$ of built-in hysteresis. For more hysteresis, you can add a large-value resistor, R_{HYST} , between the IC's input and output;

to reject short transients, IC_1 has an inherent glitch immunity of $35\ \mu\text{sec}$ with $100\ \text{mV}$ of overdrive. The input capacitance works with R_1 and R_2 to provide some lowpass-filter action. For further immunity from transients, which is unnecessary unless the power bus is noisy, you can form an additional lowpass filter by adding a small-value capacitor, C_G , to the input pin. (DI #2174) EDN

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FIGURE 1



A 1.2V reference and micropower regulator in IC_1 (a) provide an active-low reset pulse of approximately $54\ \text{msec}$ at power-up or when V_{CC} dips below 2.25V (b).