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## LOW-COST EPROM PROGRAMMER BYDANVINCENT

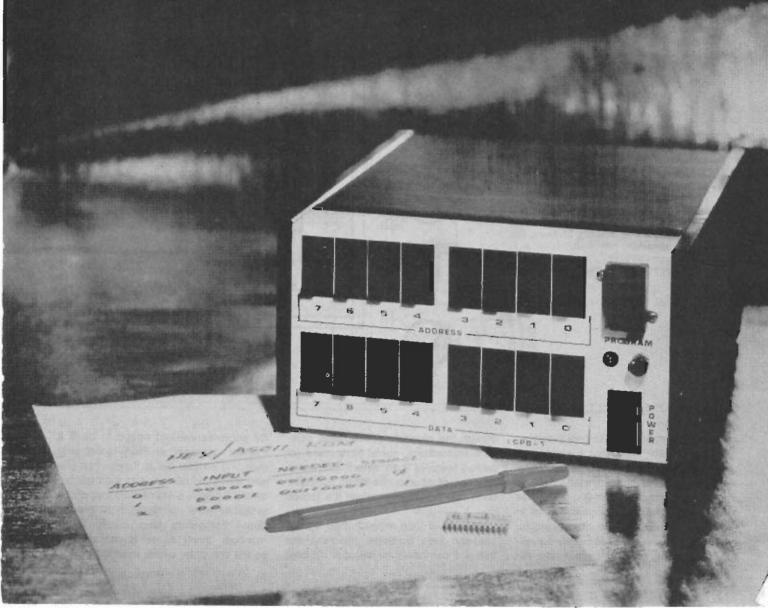
PROGRAMMING erasable readonly memories (EPROM's) has generally been beyond the reach of most electronics experimenters owing to the high cost of the machine required to do the job. Thus experimenters have been virtually limited to PROM's, in which fuse links are burned out and which, therefore, can never be reprogrammed. Now, with the low-cost EPROM Programmer presented here (\$40 without power supply, \$80 com-

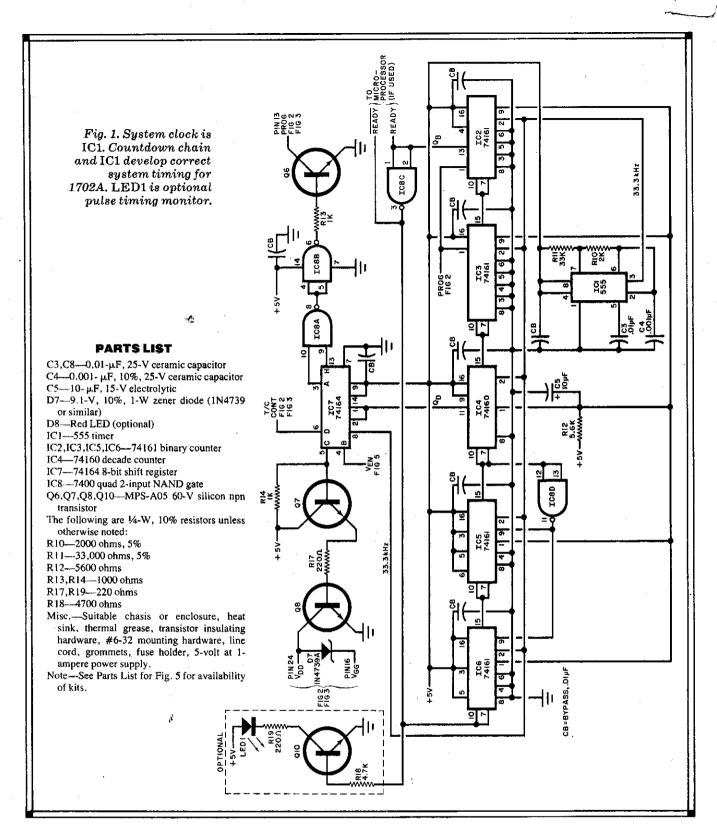
plete), it's anticipated that more and more efectronics enthusiasts will use erasable (and reprogrammable) ROM's, where mistakes can be corrected as well as an entire program changed should this become necessary.

The EPROM Programmer is designed to operate with the highly popular 256-word-by-8-bit 1702A, and associated family (4702A, 8702A), EPROM's Note that it is not compatible with other similar devices such as a 1701 or 1702. Also,

Now, you can program 1702A, 4702A, and 8702A EPROM's inexpensively.

PART 1





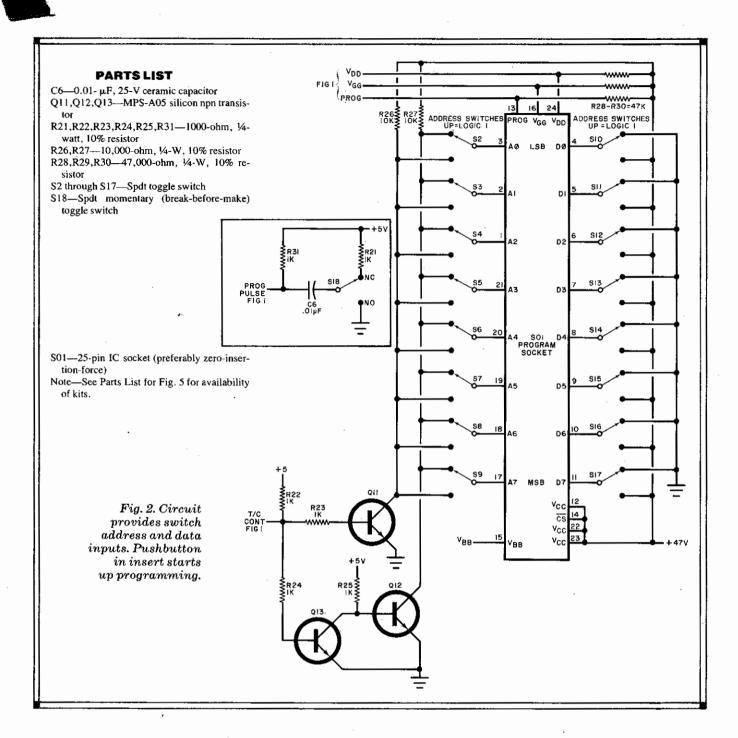
the programmer is a write-only machine, the assumption being that, if you're programming the device, you already have some type of reading provision.

Perhaps the greatest utility for EPROM's among experimenters is in the microcomputer field. For example, there is a host of different monitors available for every microprocessor chip. Al-

though the monitors share some common instructions, some have more (or better) features than others. Without a monitor, of course, the basic computer can't "do something" when it's turned on.

One could load monitor data from a cassette tape machine, naturally, but this is a cumbersome method. It's best

for convenience and speed to have a monitor program in ROM (read-only memory) so that it's all there when you turn the computer on, and data will not be lost if there's a momentary loss of line power or when computer is turned off. Some computers have built-in ROM monitors; many do not have monitors, so the computer owner must either buy



a ROM monitor, have a supplier prepare ROM's or program his own.

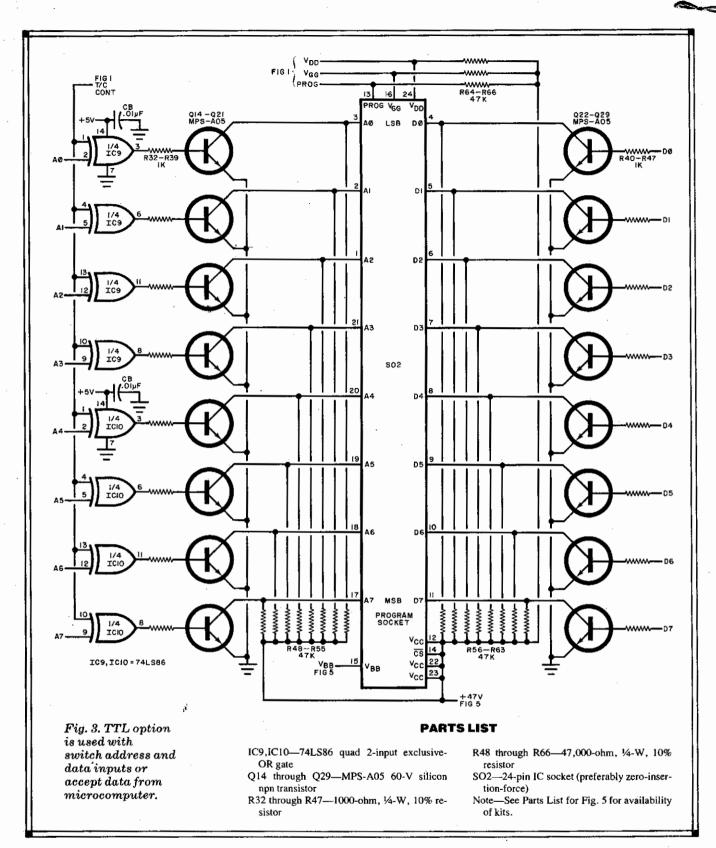
The latter route, using EPROM's could be the least expensive in the long run if a person continually upgrades his system whenever a better program or monitor comes along. An EPROM can be erased and reprogrammed very easily. The device's bit pattern can be erased (all set to "zero") by exposing the chip's transparent quartz window to ultraviolet light. In essence, the UV light's photons displace electrons that were induced in the silicon gate to form the equivalent of "1's" in the bit pattern. Then, using the EPROM Programmer,

the memory can be electronically reprogrammed. Once programmed, it will maintain data when power is removed, but unlike a fuse-link ROM, it can lose data if exposed to strong UV light.

The EPROM Programmer described here—which costs about ½ to ¼ of commercial models—complements the appealing economic picture of the popular 1702A. The device's original tag was about \$100, where today its cost ranges from \$3 to \$12, depending on quantity purchased and source. In addition, since commercial houses charge as much as \$40 to program an EPROM, doing it yourself can represent a substantial saving.

**Circuit Operation.** The 1702A EPROM itself is fully static, easily interfaced, requires no clocks, and is input/output TTL compatible. The three-state output buffers are rated for one full TTL load. However, it does require a -9-volt supply in addition to the conventional 5-volt operating supply.

The Programmer can be built as a stand-alone device using switches for address and data selection, or as a TTL-compatible peripheral for use with either switches or microprocessor ports. The circuit shown in Fig. 1 provides all the timing necessary for the Programmer. The 33.3-kHz clock, generated by *IC1*,



is routed to 8-bit shift register *IC7* and to a synchronous counter chain consisting of *IC2* through *IC6*. Integrated circuits *IC4*, *IC5* and *IC6*, in conjunction with *IC8D*, form a divide-by-430 counter whose carry output enables a divide-by-32 counter formed by *IC2* and *IC3*. Capacitor *C5* and resistor *R12* provide

the power-up initialization for the chain.

Circuit action begins with the programming command (PROG), a negative-going pulse used to asynchronously clear *IC2* and *IC3*. The pulse width should be limited to less than five milliseconds. The *Qb* output of *IC2* (pin 13) is inverted by *IC8C* to control the opera-

tion of the divide-by-430 counter. The output of this divider is taken from pin 11 of *IC4* and is a 77.52-Hz (33.3 kHz/430) signal having a 20% duty cycle with 2.58 ms on and 10.32 ms off. This waveform meets the VDD /VGG programming duty cycle restrictions of the 1702A EPROM. Also, the 2.58-ms pulse falls

under the 3-ms maximum specified for the 1702A programming pulse.

This signal is applied to the serial input of IC7 and causes its eight outputs to sequence high in 30-us intervals, the period of the clock. Output B of IC7 begins the programming cycle by turning on the +47-volt supply through Q2 of the power supply. This action sets the address and data lines to their proper levels. The address is complemented at this time. Thirty microseconds later, VDD and VGG move to their negative levels controlled by output C of IC4 driving transistors Q7 and Q8. Output D (T/C or true/ complement) of IC7 follows on the next clock pulse and inverts the address lines to their true state. Outputs E, F, and G of IC7 are not used. When output H goes high, it is AND'ed with output A by IC8A. This output is inverted by IC8B to drive Q6 and provide the program pulse to SO1 (Fig. 2 or 3).

These conditions are stable until the termination of the 2.58-ms pulse. At this point, output A of *IC7* goes low, thus ending the program pulse. Then output B disables the +47-volt supply. The shift register ( *IC7* ) is completely cleared in six more clock pulses.

During the last 30 microseconds of the 2.58-ms pulse, a carry is generated by *IC4*, causing the divide-by-32 counter ( *IC2*, *IC3*) to advance. This sequence repeats until the end of the 32nd iteration, when pin 13 of *IC2* goes true and shuts down the counter through *IC8C*. The total elapsed time for programming one 8-bit word is therefore about 413 ms. This period can be monitored by the optional status indicator (formed by *Q10*, *R18*, *R19* and *LED1*) shown in Fig. 1.

**Switch Option.** Address and data selection during programming are provided by the 16 spdt switches shown in Fig. 2. A logic 0 on the address lines is accomplished by switching the line to the collector of *Q11*. Using the V<sub>C</sub>C as a reference, this will result in a level of –47 volts during the program pulse when the address true/complement (T/C) signal from *IC7* is high, thus selecting the true address. Placing the address switch in the 1 position ties that line to the complement of the signal present at the collector of *Q12*, resulting in a logic 1.

For data input, connecting an output line to ground through the data switch results in a -47-volt level during the program cycle. This programs a logic 1 on the selected address output. Connection to the VCC line will leave the bit un-

22 Vac PROG VBB VCC Vcc no n Fig. 4. ns Illustration ADDRESS DATA shows READ 1702A D4 pin out 45 D.F for 1702A. Fξ 46 De (7 D2  $V_{DD}$ ENABLE READ CONNECTIONS

changed-a logic 0 during read.

The small insert schematic in Fig. 2 is used to manually generate the program-

## **HOW AN EPROM WORKS**

The 1702A belongs to a family of electrically programmable, ultraviolet-light-erasable, read-only memories. Each memory cell in the ROM has the appearance of a flip-flop with a new element—a "floating gate," that is isolated from the silicon substrate by a narrow band of silicon dioxide (glass). This element is not connected to anything electrically. The output signal from each flip-flop, a 1 or a 0, depends on the charge (or lack of it) on the gate.

The application of a train of electrical pulses to a cell "charges" the floating gate, and causes the associated flip-flop to produce a 1 at its output. This charge on the floating gate leaks off after many ten's of years. Since there is no electrical connection between the floating gate and the remainder of the ROM internal circuit, the charge is not affected by the removal of the chip's operating power.

The upper surface of the chip has a quartz window that is transparent to ultraviolet (UV) fight. If strong UV light is allowed to pass through the window, it will displace the electrons from their shallow energy levels on the floating gate and cause them to migrate to the silicon substrate where their charge is neutralized. Typically, it takes several minutes of strong UV exposure to erase a device, and conventional room lighting will not do the job—though exposure to direct sunshine may. After the UV exposure, all the cells go to a 0 output.

ming command through pushbutton switch S18.

TTL Input Option. The circuit shown in Fig. 3 is similar to the switch option circuit shown in Fig. 2, except that the switches are replaced by 16 transistors and 8 exclusive-OR gates. Programming voltage levels are the same as those described in the switch option. The transistors provide logic inversion as well as high-voltage isolation so that conventional TTL logic levels can define address and data selection.

The gates in *IC9* and *IC10* are turned on by the T/C signal to invert the address at the proper time. Resistors *R48* through *R66* provide leakage-current paths and insure good dynamic response.

The address lines present one "LS"-load to the driving circuit and should be no problem to interface to a microcomputer. The data lines must be driven by circuits capable of sourcing at least 1 mA at 1.7 V. Standard TTL devices will handle this, as well as many of the LSI I/O chips designed for microprocessors. Switches, connecting the inputs to the +5-volt line or ground, may be used.

1702A Data. The read connections for the 1702A (and family) are shown in Fig. 4. The EPROM may be erased by exposure to high-intensity short-wave ultraviolet radiation of 2537 angstroms. The recommended integrated dosage is 6W-sec/cm₂. Depending on the ultraviolet light source, the erasure may take from 10 to 20 minutes. ♦

Note: Part 2 of this article, next month, will describe the power supply, pc board, and construction.