Selectors squeeze data into random-access memories

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In interfacing a random-access memory (RAM) with a computer or a central processing unit, it is hard to utilize the maximum space available in the RAM because its word and bit organization is incompatible with the structure of the data bus. For example, a RAM might be configured as a 16-word-by-8-bit device, whereas the data bus might be configured to accept data organized in 8 words by 16 bits. Worse yet, no standard-sized RAM may exist for a desired data-block organization. Although there is no hard-and-fast scheme for interfacing, the circuit shown in the figure, which in this case configures data in a 128-word-by-1-bit block although accepting the same data from an 8-word-by-16-bit bus, will yield insight on how to solve similar problems.

Since no 128-word-by-1-bit RAMs exist, two 7489 16-word-by-4-bit devices are used. One stores 64 even-addressed 1-bit words; the other stores the remaining odd-addressed words. Two two-to-one-line data selectors (74157s), driven by a 7-bit system counter, assign data on the bus to their corresponding RAMs.

The bus line is wired into the 74157s, so that their outputs map their corresponding RAMs as shown. During the write operation, bits 3 to 6 of the 7-bit counter are used for addressing. Bit 3 enables data to enter the correct RAM in blocks of 4 bits. Thus all available locations in both RAMs will be filled with data.

On readout, two four-to-one-line selectors (74153s) and a two-to-one selector (74157) extract the desired data in sequence from both RAMs. During the read operation, bits 3 to 6 are used for addressing the RAMs, as before. Bits 0 to 2 address the appropriate data selectors: bit 0 selects either odd- or even-location data (in order) from the 74157, and bits 1 and 2 direct the data from the 74153s to the input of the 74157. Thus 128 1-bit words appear at the output.

Because data from the bus is loaded into the RAMs 8 bits at a time, the clock rate of the RAMs' address counter should be twice that of the bus line's data rate. To say it another way, the 7-bit counter should run 16 times faster than the computer's clock.

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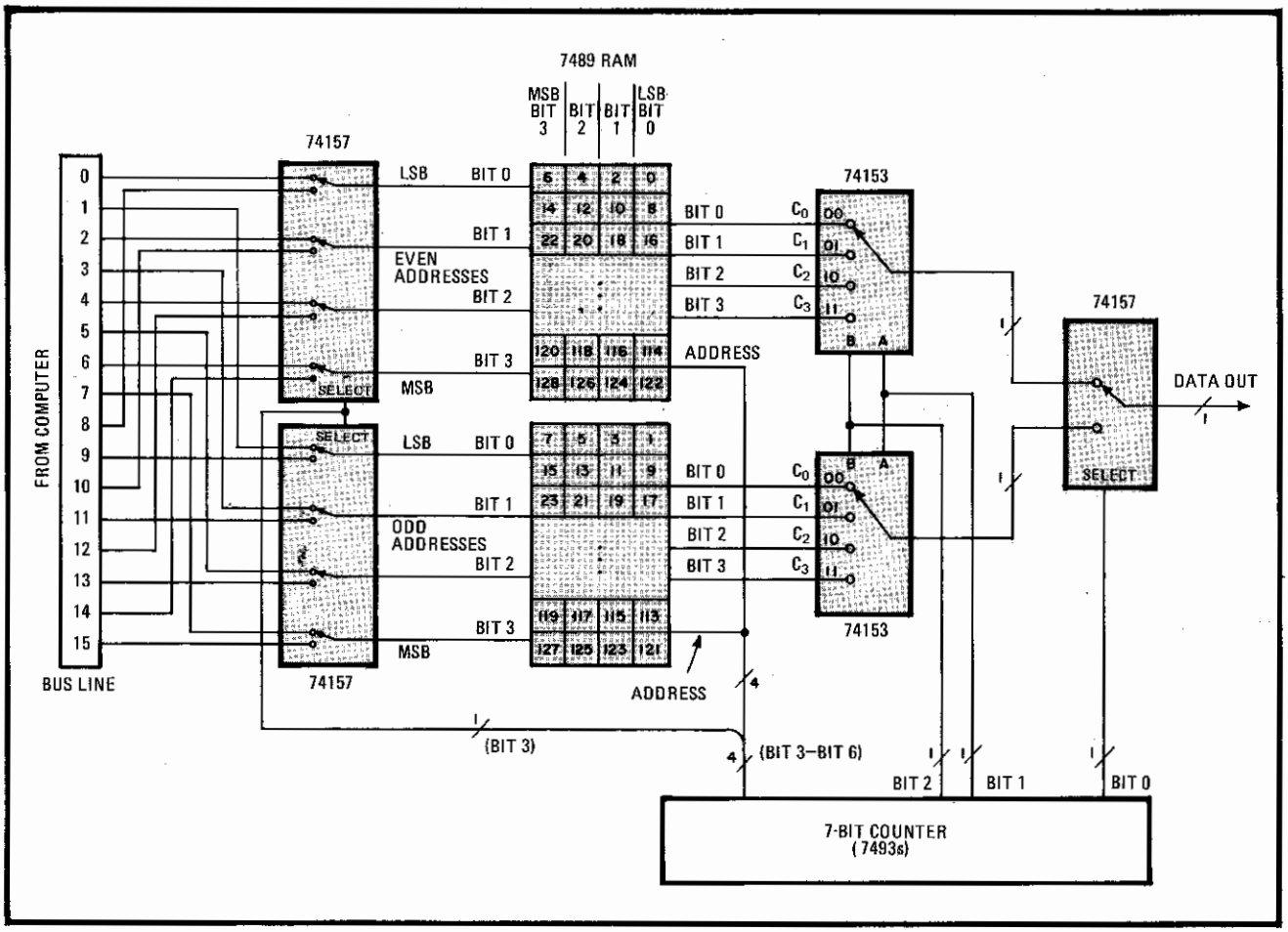

Selective addressing. Maximum number of RAM locations can be filled with data, despite incompatibility of RAM's word and bit organization with data-bus structure. General method for organizing large, nonstandard-sized m-word-by-n-bit data blocks from p-word-by-q-bit data bus uses selectors for mapping data into two RAMs, one of which contains the even-addressed data, the other the odd-addressed data.