TECH TIPS

PROM Expansion Card

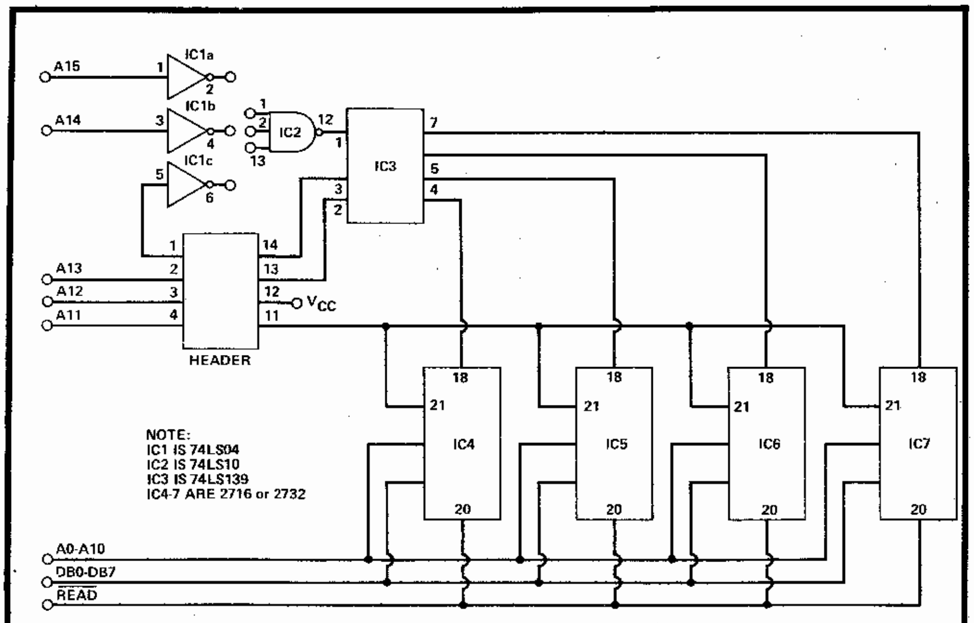
A.Adnitt

This circuit provides a very expandable expansion card for 16 bit address processors and single supply EPROMs. In all expansion cards I have seen they take either four 2K PROMs or two 4K PROMs leaving two empty sockets. Now, by very simple means, an expansion card can be made to give 8K or 16K of memory as shown in the diagram.

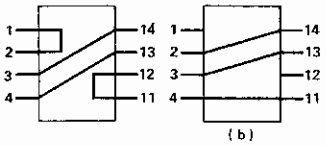
If an 8K set-up is first considered with the header wired as shown in Fig. 1a, then pin 21 (Vpp/A11) of IC4-IC7 is held high, A11 and A12 are used for chip select through the 2-to-4 line decoder (half a 74LS139) and IC1 and IC2 are hard-wired to decode address lines A13, 14 and 15 to select a particular 8K block of memory (see table).

Now, when your operator program outgrows this, a new card is not necessary, just a rewire of the header (Fig. 1b) and the larger EPROMs. In doing this, A11 is taken to IC4-IC7, A12 and A13 are used for chip select through IC3 and now with pins 1 and 2 joined together on IC2, hard wiring with IC1 gives a unique 16K block by decoding address lines A14 and A15. It must be noted, however, that this can only be used for 2716 and 2732 EPROMs as TEXAS 25XX EPROMs have different pin-outs.

By providing 28-pin sockets and additional wiring, the circuit could be reconfigured to take 2764 PROMs — how's that for versatility, as little as 2K to a mammoth 32K of ROM catered for by one card!



NOTE:
IC1 IS 74LS04
IC2 IS 74LS10
IC3 IS 74LS139
IC4-7 ARE 2716 or 2732



8K BLOCK	a	b	c
1st	IN	IN	IN
2nd	IN	IN	OUT
3rd	IN	OUT	IN
4th	IN	OUT	OUT
5th	OUT	IN	IN
6th	OUT	IN	OUT
7th	OUT	OUT	IN
8th	OUT	OUT	OUT

IC1

16K BLOCK	a	b
1st	IN	IN
2nd	IN	OUT
3rd	OUT	IN
4th	OUT	OUT

IC1

Continued on page 84

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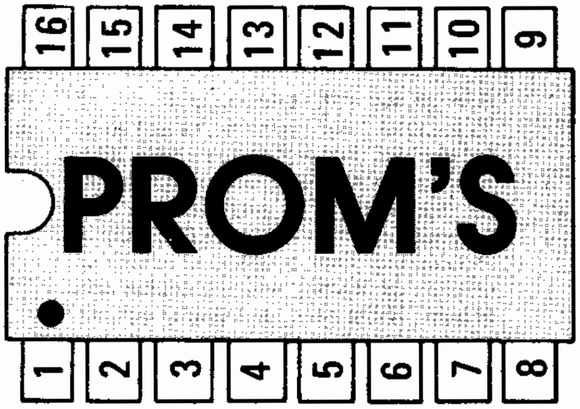
AMD 27S10C
27S10M

	74S387 ✓	54S387	74S287 ✓	54S287
AMD	27S10C ✓	27S10M	27S11C ✓	27S11M
FSC	93416C 93417PC ✓	93417M	93426C 93427 PC ✓	93426M
Harris	HM 17610-5 HPROM 1024A-5 7610 ✓	HM 17610-2 HPROM1024A-2	HM17611-5 HPROM1024-5 7611 ✓	HM17611-2 HPROM 1024-2
INTEL	P3601 ✓		3611 ✓	
Intersil	IM5603AC ✓	IM5603AM	IM5623C ✓	IM5623M
MMI	6201 6300J-1 ✓	5300	H6201	H5201 5301 6301 J-1 ✓
NSC	DM8573	DM7573	DM8574	DM7574
SIG	N82S126 ✓	S82S126	N82S129 ✓ N82S229	S82S129 S82S229

Making PROM'S Work For You



The programmable read-only memory is becoming the workhouse of modern digital electronics and will play an ever-increasing role in your everyday activities. Here is what it's all about.

ROBERT H. PENOYER

THE PROM (PROGRAMMABLE *R*EAD-*O*NLY *M*emory) is increasingly being accepted as a circuit element. The electronic hobbyist or home computer owner should become familiar with this very useful device. Because there have been numerous articles written about both the PROM and the EPROM (*E*rasable PROM), this article will just briefly mention their theory of operation, and concentrate on the ways these devices can be put to use.

What is a PROM?

Figure 1 shows the basic configuration of a 16 × 4-bit PROM; that is, there are 4 address lines, and, therefore, $2^4 = 16$ states can be represented. Each of these 16 states is decoded into a single control line that leads to a set of junctions in the memory array. These junctions are either closed or fused open depending upon how the PROM is programmed. The logic state of the junctions selected by the address decoder passes through the buffer and appears at the output. Figure 1 shows 4 output lines; thus, there are $2^4 \times 4$ or 16×4 junctions. This PROM can also be described as containing 16 words with 4 bits-per-word. There are as many words as there are address states. Therefore, if the PROM had eight address lines and one output line, it would be a $2^8 \times$ 1-bit or a 256 × 1-bit PROM, or containing 256 1-bit words.

Just as there are closed or fused-open junctions in a PROM array, the EPROM uses static charges on MOSFET transistors to achieve the effects of an open or closed junction. The charges on the MOSFET's can last for years or be erased in a few minutes by special ultraviolet lamps.

Using the PROM

The PROM serves two main purposes: First, a single PROM IC can replace an entire multiple-gate logic array. Say, for example, you needed a set of gates that would perform the function described in the truth table of Fig. 2. If standard gates were used, a complex network would result. Instead, let the four left-hand columns of Fig. 2 represent the address lines, and let the column on the right represent the output line of a 16 × 1-bit PROM. Thus you would achieve the desired function using only a single IC. The result is a savings in wiring time, troubleshooting time and board space.

The second main use of a PROM is as a "look-up table." For example, suppose you wanted a counter to count in the sequence shown in the right-hand side of Fig. 3. This could be extremely difficult to accomplish using ordinary logic. Instead, you can apply the output lines of an ordinary binary counter to the address lines of a PROM. Upon reaching any of the 16 possible states, the counter causes the internal logic of the PROM to "look up" the desired output state and pass it through its buffer to the output, according to the truth table. Only two IC's, a 4-bit binary counter and a PROM are needed to arrive at a rather complicated sequential output.

Another example of using a PROM as a look-up table is a Baudot to ASCII code translator. The Baudot code can act as the address for a PROM, and the PROM output can yield equivalent ASCII characters.

Propagation delay and access time

As with any logic device, propagation delays in PROM's are important, particularly so if a PROM's output lines are used to drive counters or clocked logic of any type.

A specifically limited amount of time is required to receive an address, decode it, drive a set of junctions in the PROM array and transmit the result through the buffers to the PROM output. This is called the PROM's access time, and is

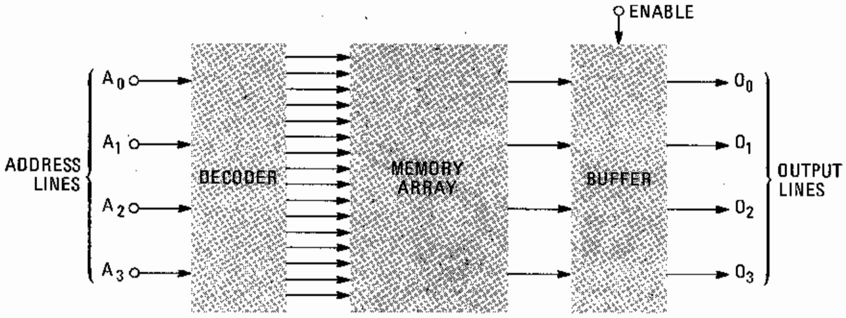


FIG. 1—PROM consists of an address decoder, output buffer and memory array.

A_0	A_1	A_2	A_3	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

FIG. 2—COMPLEX LOGIC FUNCTIONS such as the one shown in the above truth table can be easily handled by a PROM.

A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3
0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	1	1
0	1	0	0	1	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	1	0	1	1
0	1	1	1	1	1	0	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	1	1
1	0	1	1	0	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	0	0	0
1	1	1	0	1	0	0	1
1	1	1	1	1	0	1	0

FIG. 3—COUNTERS with an unusual counting sequence can easily be designed using a PROM.

listed in the manufacturer's data sheet. During the access delay time, the state of the output lines on a PROM is unpredictable. A set of outputs can pass through several states during the transition from one address to the next. Therefore, if the outputs are driving clocked logic, the logic could receive undesired data. Obviously, this should not be allowed to happen. Luckily there are methods to get around this problem.

Buffer and latch isolation

As shown in Fig. 1, the output buffer of the PROM often has an enable control line. Typically, this enable line is used to select the device that is to be connected to a parallel bus system when many such tri-state devices are used. When enabled, the buffer outputs are at normal logic levels. When not enabled, the buffer outputs appear to be open circuits. If all the buffer output lines are pulled to +V through, say, 10K resistors (in the case of TTL logic) then when the output lines are disabled they will be at a known high logic level. Therefore, no output line can go low unless that particular bit was programmed low and the PROM output was enabled. Thus, it is only necessary to disable the output when changing addresses. Using such an arrangement, no glitches appear at the output and low-going pulses appear only when desired. Figure 4 shows a typical circuit using this technique.

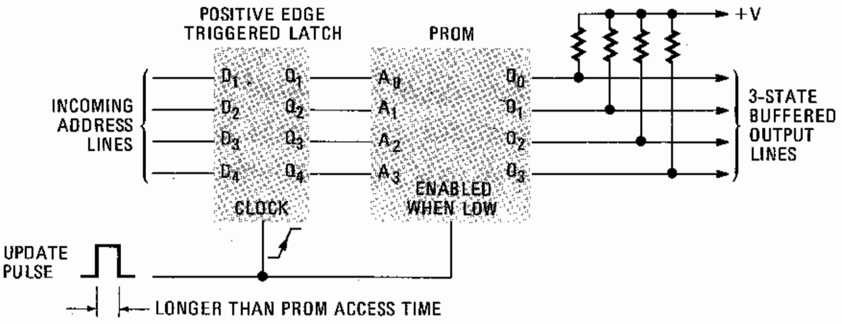


FIG. 4—DISABLING PROM during access time prevents glitches from appearing at the output.

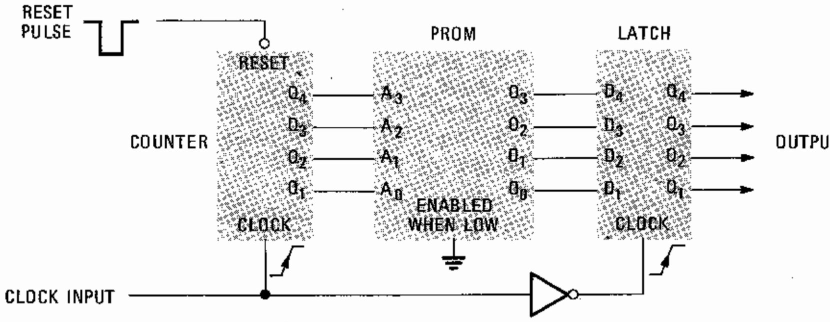


FIG. 5—CLOCK SIGNAL in synchronous circuits can be used to inhibit output during access time.

You can use a similar more desirable technique that requires no pull-up resistors on the buffered output lines. Let's say, for example, you want a circuit that counts as shown in the Fig. 3 truth table. Also assume that you could not arbitrarily allow the outputs to go high, as shown in Fig. 4.

Figure 5 shows an alternative technique: a synchronous binary counter drives the address lines of a PROM that is programmed according to the truth table shown in Fig. 3. Therefore, as the counter passes through each binary state, the desired output appears on the PROM output lines. These lines are always enabled as shown in Fig. 5. Note that both the counter and the latch are triggered by positive-going clock edges, and there is an inverter in the latch clock line. This means that while the counter still triggers on the positive-going edge of the clock, the latch will trigger on the negative-going edge. This provides a delay of one-half clock period between the time the counter is updated and the resulting PROM output appears at the latch output. If the PROM access time is shorter than one-half clock period, its output will be settled by the time the latch uses it. The result is a clean accurate set of waveforms at the latch output.

PROM sources

PROM's and EPROM's are available in many configurations. Just check through manufacturers' catalogs for the type of PROM you need for your application. Sometimes the required number of words and word length are not available and you have used a PROM with more words or bits than you need. In this case, you should consider the economics of wasting PROM capability.

Most large distributors can program a PROM for you if you purchase it from them. Find out all the necessary information before placing the order for your PROM; often the distributors will program the device for a small fee or at no additional cost. **R-E**

how a PROM works

Programmable Read Only Memories are manufactured using various technologies. This article describes each type of PROM and its advantages and disadvantages.

by ROGER L. SMITH

REMEMBER WHEN SOMEONE MENtioned a PROM, we all thought of a high school dance? Well, in today's age of electronics, a PROM is a *P*rogrammable *R*ead *O*nly *M*emory. Incidentally, PROM is a trademark of Harris Semiconductor Div. of Harris Intertype Co.; however, the word has become generic because of its widespread use in describing all field programmable ROM's.

Speaking of ROM's, let's cover some of the basics of memories and the terms used before going any further. The first memories that were used with computers (and a computer is not a computer without a memory) were ferrite-core memories. These core memories—provided they were properly powered down and up—were nonvolatile, meaning the data in them was not lost when power was removed. In a volatile memory, all data is lost in powering down. Most core memories are also classified as DRO, although a few are NRDO. The DRO (*D*estructive *R*ead-*O*ut) uses a read-write cycle to restore data to the cores. An NDRO (*N*on-*D*estructive *R*ead-*O*ut) memory does not require rewriting the data after a read cycle is completed.

With the advent of LSI (*L*arge *S*cale *I*ntegration) techniques and the decreasing cost of semiconductors, the use of semiconductors as memory elements became possible. Various types of semiconductor memories evolved—from simple diodes arranged in a matrix to flip-flops, stored-charge devices and amorphous semiconductors. These new types of memories permitted designers to implement the ROM for cases where the memory was to be used for fixed conditions such as program control.

These ROM's presented logic designers with options not previously available. Now it became possible to replace complex logic circuits with ROM's. You can imagine how difficult it would be to design the logic for a code conversion—a simple job for a ROM. Another unique use for ROM's is in custom waveform generators. A sequential counter feeds the ROM inputs and the outputs go to a digital-to-analog (D-to-A) converter. In another use, the inputs are treated as separate logic inputs and the ROM acts as a Programmable Logic Array (PLA). For more information, refer to the article "What Is A ROM?" in the February, 1974 issue of **Radio-Electronics.**

What PROMs are available?

The simplest PROM's—diode matrices—are available in 14-pin packages (Harris HM1-034-2, a 6 × 8 array) containing diode arrays with fusible links, These diode matrices can be programmed by "burning out" the fusible links and thus can be classified as PROM's. Such memories are used primarily in encoding and decoding functions.

Amorphous semiconductor

An interesting type of memory that is also field-programmable is the amorphous semiconductor memory. This memory consists of amorphous glass semiconductor resistors (called ovonic memory switches by Energy Conversion Devices, Inc.) in series with silicon diodes in a matrix array. The glass semiconductor can exist in either of two phases—amorphous or polycrystalline. The resistors in the amorphous phase show a resistance of about 300K ohms, and in the crystalline phase about 500 ohms. The low-resistance, or set state, is achieved by applying a 15 millisecond pulse to the bit to be set. The high-resistance, or reset state, requires applying 8 to 10 five-microsecond pulses at 80 μs intervals.

These amorphous memories thus have a slow write-cycle time and are called by the manufacturer (Energy Conversion Devices) Ovonic Read-Mostly Memories (RMM). These devices are non-volatile like PROM's but they can also be written into like Random Access Memories (RAM's).

Fusible links

The semiconductor PROM most often used at this time is the bipolar type containing memory elements composed of nichrome fusible-links. Intel is

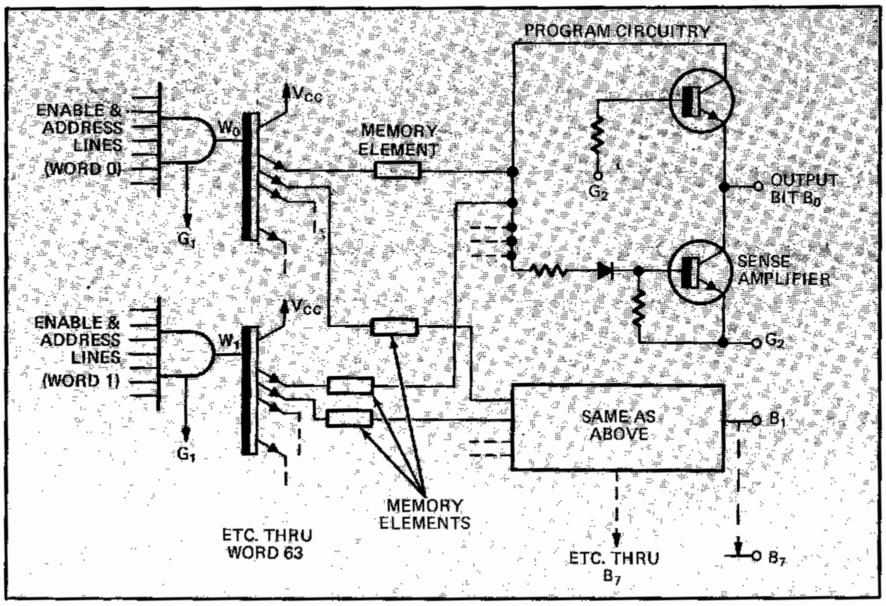


FIG. 1—512-BIT PROM schematic shows the word transistors (64 of them) connected to the sense and program circuits via memory elements.

TABLE 1

Manufacturer	Part No.	Organization	Bits	Supply Voltage		Memory Element	Special Notes
				Normal	Program		
Advanced Micro Devices	AmS08	32x8	256	+5V	10V to 15V	polysilicon	open col. out. { +2 words
	AmS09	32x8	256	+5V		polysilicon	3 state out. { 9th bit
Harris Semiconductor	HPROM-0512	64x8	512	+5V	+5V,+15V	nichrome fuse	Program similar to
	HPROM-1256	256x1	256	+5V	+5V,+15V	nichrome fuse	Signetics.
	HPROM-8256	32x8	256	+5V	+5V,+15V	nichrome fuse	
	HPROM-1024/A	256x4	1024	+5V	+5V,+15V	nichrome fuse	3 state out, A=open coll.
	HPROM-2048/A	512x4	2048	+5V	+5V,+15V	nichrome fuse	3 state out, A=open coll.
Intel Co.	1602A/1702A	256x8	2048	+5V-9V	+12V,−45V	FAMOS device	1702A is erasable
	3604	512x8	4096	+5V	+10V,+15V	polysilicon	all outputs norm. high (1)
	8702A	256x8	2048	+5V-9V	+12V,−45V	FAMOS device	3 state out
	3601	256x4	1024	+5V	+10V,+15V	polysilicon	
Intersil	IM5600C/IM5610	32x8	256	+5V	+5V,+28V	"AIM" device	open coll. 5610=3 state
	IM5603A/IM5623	256x4	1024	+5V	+5V,+28V	"AIM" device	special pulse programmer
	IM5604/IM5624	512x4	2048	+5V	+5V,+28V	"AIM" device	
Motorola Semiconductor	MCM5003AL	64x8	512	+5V	+5V,−6V	nichrome	9th bit. Prog. manually
	MCM5004AL	64x8	512	+5V	+5V,−6V	nichrome	has 2K on output
National Semiconductor	MM5202A	256x8	2048	+5V-9V	+12V,−45V	FAMOS device	Q suffix has quartz lid
	MM5203	256x8	2048	+5V-9V	+12V,−45V	FAMOS device	for erasing.
	MM5204	512x8	4096	+5V-9V	+12V,−45V	FAMOS device	
Signetics	8223	32x8	256	+5V	+5V,+12.5V	nichrome	open coll. Prog. manually
	82S23/82S123	32x8	256	+5V	+5V,+12.5V	nichrome	82S123=3 state
	82S26/82S29	256x4	1024	+5V	+5V,+12.5V	nichrome	26=open coll. 29=3 state
Texas Instr.	SN74186	64x8	512	+5V	+5,−5V	nichrome	9th bit & extra word tested
	SN74188A	32x8	256	+5V	+5V,+10V	nichrome	by mfg. Prog. manually
							open collector output
							All types are 0° to 75°C

presently making bipolar PROM's (up to 4096 bits) using polycrystalline silicon fuses (instead of nichrome). Advanced Micro Devices also makes 256 bit PROM's with silicon fuses. A look at Fig. 1 will help you to understand the operation of this type of fuse-link PROM. This figure is a block diagram of a 64-word, 8-bit PROM (512 bits). The 6-bit ADDRESS input is buffered and inverted to provide true or complement addresses to each of six inputs on the 64 multiple-emitter AND gates. A seventh input provides the chip enable signal. Since only one of the 64 AND gates will be activated for a particular address, that gate will generate a high level on one of the 64 word lines connected to each gate output. These word lines are connected to the bases of 64 multiple-emitter transistors located in the memory section of the circuit.

The selected (1 of 64) multiple-emitter transistor drives the output transistors thru the eight memory elements. With the proper resistive load connected to their collectors, these transistors will saturate and a low voltage, or logic "0," will appear at the output. Thus the normal output of such a PROM, with the memory elements intact, is a "0." This PROM is programmed by opening the appropriate memory elements and causing a logic "1" to appear at the output for a specific address.

Memory elements of this type (as in the Motorola MCM5003) are fused open by connecting a negative voltage (−6V) to the output collector of the desired bit, applying a voltage (+5V) to V_{cc}, grounding pin G2, and connecting G1 to a negative voltage (−6V). Then the desired word is addressed (with −6V as a "0" and −4V to +5V as a "1"). Notice in Fig. 1 that this forward biases the program transistor for that bit so that when the address is

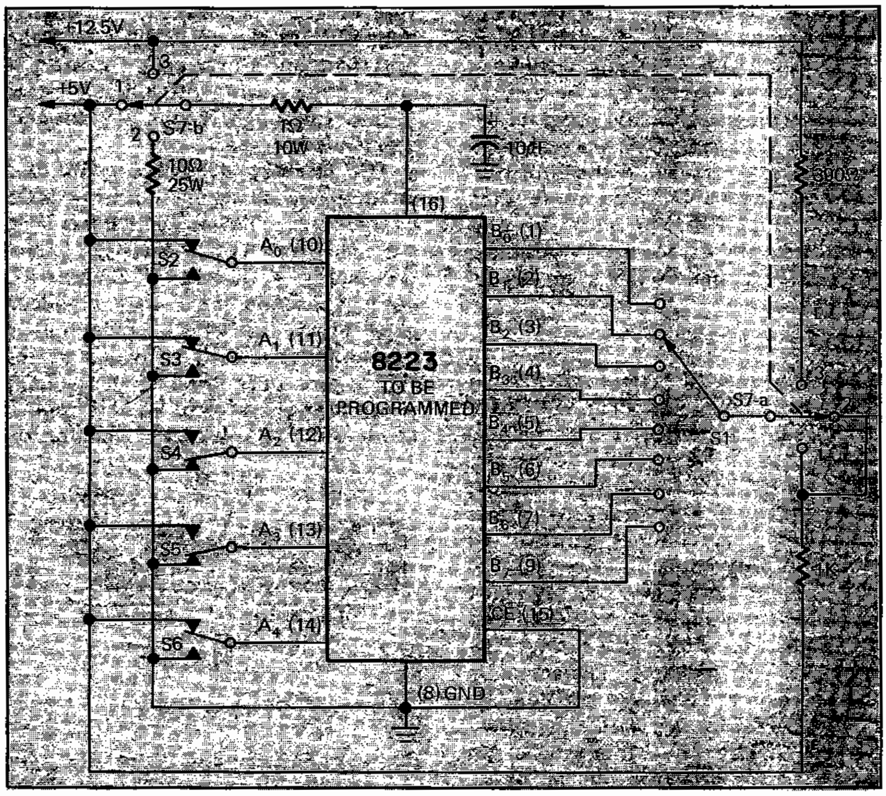


FIG. 2—MANUAL PROGRAMMER schematic. During programming, switch S7 is moved to position 2 long enough to discharge the 10-μF capacitor. Switch S7 should not be in position 3 for longer than one second.

selected, current thru the memory element is increased (to 30 mA). This is sufficient to cause the metal fuse to flow and separate. The current is applied as a ramp and limited to 60-mA maximum to prevent sputtering, metal splatter, or oxide damage.

Programming voltages for other nichrome type PROM's such as Signetics' 8223, vary somewhat. However, the basic idea is to allow a heavy current to pass thru the nichrome "fuse" to a program transistor that is biased into saturation. Figure 2 shows a manual programmer that can be used to program the Signetics 8223. When using this programmer, current should not be applied to a bit for over one second.

Two precautions should be observed when programming this type of PROM. One is to limit the application of programming current to one output at a time. This current passes thru the multiple-emitter "word transistor" whose design doesn't allow it to conduct more current than required to open one element. Another precaution is to maintain the case temperature of the PROM at or below 75°C. This is easy to do if you program manually and remove voltages as soon as the memory element opens. Automatic programming may require a heat sink.

The above description of programming the fuse-link type of PROM illustrated a manual technique. Manual programming is possible with most types of nichrome fuse-link PROM's *provided* that the currents are limited in some manner. Most often, the rise time must be controlled and the duration and amplitude of the programming current must be limited. This is easily done with a pulsing technique. All of this of course, can be accomplished with an automatic programmer that also sequences thru the addresses and bit patterns. Automatic programmers are desirable when more than three or four PROM's are to be programmed, and are required equipment for some of the PROM's to be described next.

AIM

Another type of memory element is used by Intersil in their PROM's. They have patented *A*valanche *I*nduced *M*igration (AIM) programming system. Each memory element in an open-base NPN transistor whose base-emitter junction is shorted out when it is programmed.

A partial schematic of an AIM matrix is shown in Fig. 3. Notice that the matrix is constructed using conventional TTL processes. Collectors on the "X" lines are common and emitters on the "Y" lines are common, allowing for simple fabrication steps. No connection is provided for the bases. To program an element, a high current is forced thru it from emitter to collector. The emitter-base junction is forced beyond normal avalanche and into a second breakdown mode. Aluminum moves into the junction and causes a short. The result is a low-resistance path to the base and a base-collector diode as shown in Fig. 3.

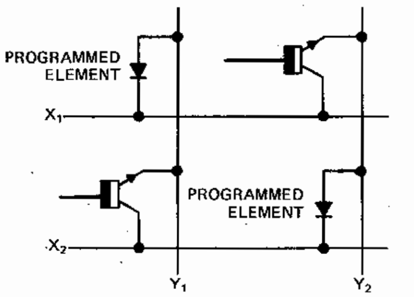


FIG. 3—PARTIAL AIM PROM matrix with two bits programmed as "1".

The programming is done using a 200 mA pulse (at about 32V) of about 2.5 μs duration followed by a 20 mA, 1.5 μs sense pulse. These pulses are repeated a number of times until a change in the bit has been detected. The programmer then moves on to the next bit automatically.

FAMOS

The last type of PROM we will investigate is the stored-charge type made by Intel and National Semiconductor. This type of PROM falls in the same category as the ovonic amorphous semiconductor type mentioned earlier in that it can be *re*-programmed (however, not electrically). The advantage of this type of PROM is obvious. If you make a mistake, or change your bit requirements, you can change your PROM by erasing all bits and programming it over again! Erasure is accomplished with ultraviolet light or X-rays (although X-rays are not recommended).

The memory element consists of a floating-gate avalanche-injection MOS charge-storage device (which has been shortened to FAMOS transistor). Notice in Fig. 4 that the FAMOS transistor is essentially a P-channel silicon gate MOS field-effect transistor in which no contact is provided to the silicon gate. In programming, a voltage pulse in excess of −30 volts is applied to the drain or source PN junction resulting in the injection of high-energy electrons from the PN junction surface avalanche region to the floating silicon gate. This negative charge on the gate results in current flow between source and drain of the P-channel FAMOS transistor.

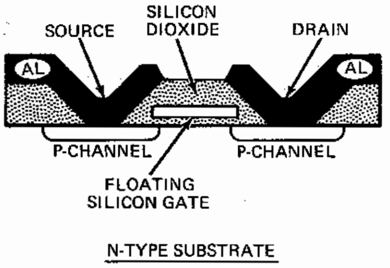


FIG. 4—CROSS-SECTION OF FAMOS structure. Negative charge on floating gate causes conduction between source and drain.

The FAMOS transistors are arranged in a matrix on the silicon chip along with an X and Y decoders, input drivers, output sensors and buffers to form the complete MOS memory device. Programming these PROM's (typically the Intel 1702A, 2048-bit PROM) requires special programmers that pulse the device with a minimum of 32 program pulses for each 8-bit word to be programmed. Note in this PROM that all 8 bits of a word are programmed simultaneously. In addition to the program pulse, voltages V_{GG} and V_{DD} are also pulsed. The Intel Company will furnish you schematics for the MP7-03 PROM Programmer, or of course, you could buy an assembled unit.

The Intel 1702A PROM comes with a transparent quartz lid which permits you to erase the bit pattern. You can erase a device by exposing it to high intensity ultraviolet light at a wavelength of 2537 A. Just put the 1702A about 1 inch away from the lamp tube for 10 to 20 minutes. Recommended lamps are Models UVS-54 or S-52 ultraviolet lamps manufactured by Ultra-Violet Products Inc., San Gabriel, CA. Physically, the erasing action creates an ionizing effect that causes the excess electrons on the floating gate to flow back to the substrate.

You have no doubt noticed that many of the PROM's we have covered use irreversible memory elements. Aside from the fact that such a PROM cannot be reprogrammed, there is also the problem of testing the PROM initially. If you order a ROM, the manufacturer programs it to your specification and tests it to be sure the bit pattern and output circuits are OK. However, if you buy a PROM, there most likely was no way for the manufacturer to test it so you won't know if it is any good until you program it. Most manufacturers build PROM's with experience and quality control. Several PROM manufacturers have decided that this method is not good enoungh (Motorola and Advanced Micro Devices among them). They have solved the testing problem by adding a ninth bit to all 8-bit PROM's. Some have even added several extra words to the memory. In the Motorola MCM5003 there are 32 of these ninth bits that have already been programmed to "1s," and the remaining 32 bits may be used by the customer to check out the capabilities of his programming circuitry.

Table 1 has been prepared to help

(continued on page 119)

HOW A PROM WORKS

(continued from page 74)

you in selecting a PROM. This table includes most of the presently available PROM's along with the number of bits and the bit organization of each. Also included are voltage requirements for both the read and write (programming) modes. Comments in the special notes column may also be helpful in choosing a PROM that exactly fits your requirements.

The main thing for you to remember in selecting a PROM is how you are going to program it. Unless you are prepared to spend some extra time and money for automatic or pulsing type programmers, it is advisable to stick with the fuse-link PROM's that can be programmed manually (Signetics 8223, Motorola MCM5003 etc.). Whichever way you go, remember to proceed slowly. Once you decide on your bit pattern (program), set it aside and check it over from the beginning the next day. It's easy to change an error on paper, but impossible in most PROM's.

Another hint for those of you who want to try out some PROM's: several of the PROM's we have mentioned in this article are available from companies advertising in the back pages of **Radio-Electronics.** For instance, the Signetics 8223 was noted in a couple of ads for under $5, and the National Semiconductor MM203 (similar to Intel's 1702A) can be found for around $20. **R-E**

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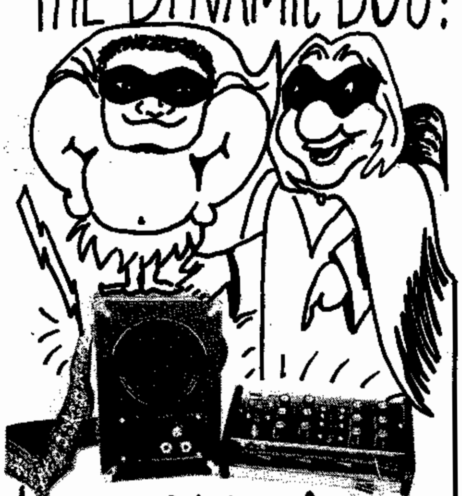

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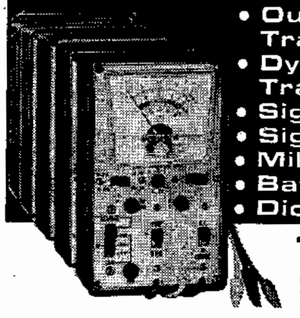

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Engineer's notebook

DIP switches and diodes form programable ROM

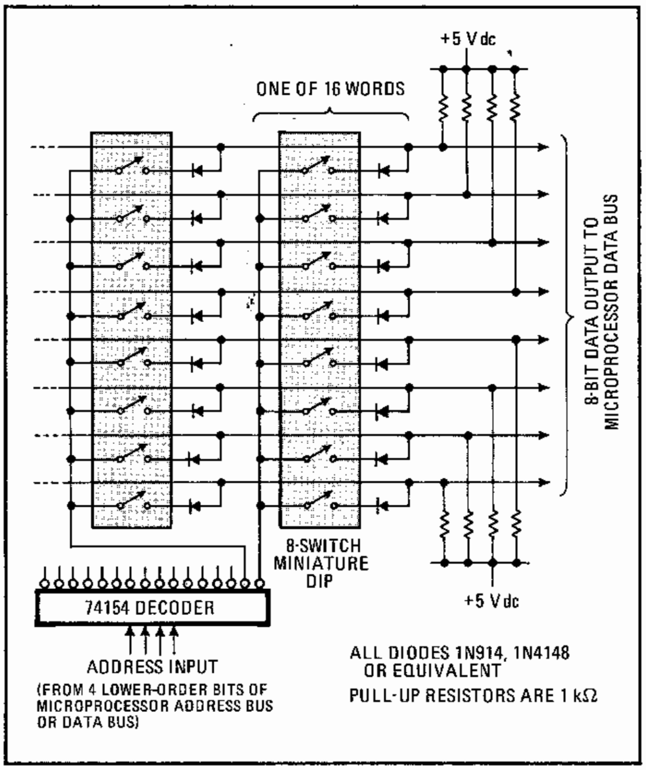
by Louis E. Frenzel
Heath Co., Benton Harbor, Mich.

Microprocessor-based equipment depends more on software than on hardware for its operation, and therefore the design of such equipment consists largely of program development. If the memory in which a program is stored can be changed easily and quickly, program writing and debugging are simplified. The programable read-only memory described here speeds up these program-development processes, and thus facilitates physical breadboarding with the microprocessor in the initial stages of design.

The PROM shown in Fig. 1 is a switchable diode matrix organized into 16 8-bit words. Each bit is implemented with a single-pole, single-throw switch and a diode. To simplify construction and minimize size, the PROM uses the new 8-switch/16-pin dual in-line packages. Each DIP unit thus represents one 8-bit word.

Instruction words and data words are loaded into the memory by setting the switches; a closed switch produces a low (binary 0) output, while an open switch generates a high (binary 1) output.

1. DIP-switch memory. Microprocessor programs can be tested with read-only memory, consisting of eight-switch DIPs used as 8-bit binary words. This memory, which is simple to set or change, can be checked visually. Diodes in the ROM isolate words from one another. The decoder connects the DIPs to the data bus.



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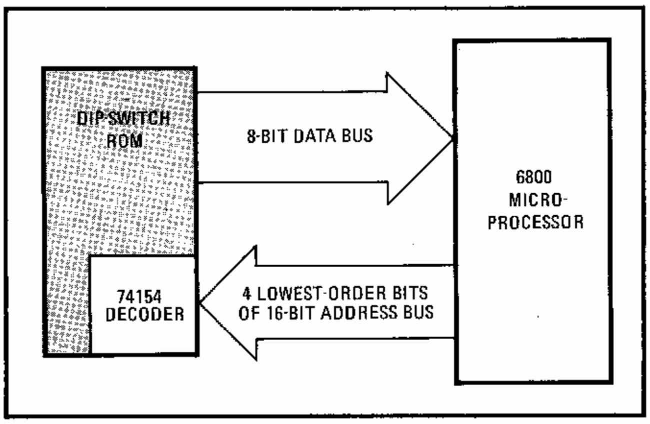


2. Example. This arrangement of a DIP-switch ROM with a 6800 microprocessor is used for the program shown in the accompanying box. (Other microprocessors may have different means for address input.) Programs can be set up, tested, and modified more simply with the switch memory than with integrated-circuit ROMs or RAMs.

Instruction words are loaded into sequential memory locations. Data words can be placed in any convenient memory location that is available. If the DIP switches are arranged in address sequence with the switch levers properly oriented (up = 1, down = 0), the memory contents can be determined at a glance. The ability to see the memory content and to change it in seconds will greatly expedite program development. It becomes possible to modify and debug a program in a fraction of the time that would be required if a conventional ROM or RAM were used.

The use of only 16 words may seem severely limiting in a ROM, but it is usually more than adequate to test and exercise a microprocessor. The memory is sufficient to try all instructions and to test short subroutines. The flexibility of being able to quickly and conveniently change a program and to actually see the program stored in memory makes it easy to design microprocessor systems and to learn programing.

A 74154 TTL 1-of-16 decoder is used to address the memory words. The decoder input lines are connected to the four lower-order bits of the microprocessor address bus or data bus.

The box (top, right) shows a sample program using DIP-switch ROM with a 6800 microprocessor, as in Fig. 2. For this application the 16 switches are numbered consecutively in hexadecimal notation: 00, 01, 02 . . . 09, 0A, 0B, . . . 0F. The program contains five instruction words and two data words. Three of the instructions (LDAA, ADAA, and STAA) occupy two sequential 8-bit locations. Instructions DAA and WAI each occupy a single 8-bit location. The instruction words are loaded into the first eight DIP switches because the microprocessor operates on instructions sequentially. The two data words can go into any of the eight remaining switches; here the data words are put into the last two switches (0E and 0F). The data stored for this example are the numbers 48 and 37, which are set on the switches as 0011 0000 and 0010 0101, respectively.

The program tells the microprocessor to do the following: first, load its accumulator register A with the number stored at location 0F; next, add the number at location 0E to the number in the accumulator, and store the sum in A; finally, convert the binary number in A to its decimal (BCD) equivalent, and store the decimal number in location 1F. After it has completed all these operations, the microprocessor is to await an interrupt signal.

The instruction set provided by the manufacturer of the 6800 shows how to set the ROM switches to deliver these instructions to the microprocessor. The first instruction, designated LDAA, is set into switch 00 as hexadecimal 96, which is binary 1001 0110. The second half of this instruction is stored in switch 01, and gives the location of the data to be loaded; that location is hexadecimal 0F, or 0000 1111. The next instruction, ADDA, is found from the 6800 instruction set to be hexadecimal 9B, or binary 1001 1011. The remaining steps are similarly set into the DIP switches by use of the 6800 instruction set.

The result of adding 37 to 48 could be displayed by an output device that showed the content of location 1F. It would show 85, because decimal notation was specified. □

SAMPLE PROGRAM

ROM address	Instruction or Data	Operation performed	Hex	Binary
00	LDAA	Load accumulator A with the contents of	96	1001 0110
01	F	memory location 0F.	0F	0000 1111
02	ADDA	Add contents of memory location 0E to the	9B	1001 1011
03	E	number in accumulator A and store the sum in A.	0E	0000 1110
04	DAA	Convert the binary number in A into BCD.	19	0001 1001
05	STAA	Store contents of accumulator A in memory location	97	1001 0111
06	1F	1F.	1F	0001 1111
07	WAI	Wait for interrupt.	3E	0011 1110
08				
09				
0A				
0B				
0C				
0D				
0E	48	Data	30	0011 0000
0F	37	Data	25	0010 0101

Experimenter's Corner

By Forrest M. Mims

PROGRAMMABLE READ-ONLY MEMORIES

SEMICONDUCTOR memories are among the most important electronic circuits. They are found in almost all digital devices, ranging from pocket calculators to computers. Besides their obvious application in the storage of information, these memories can be used in the synthesis of unusual waveforms, music, and even human speech.

There are two basic types of semiconductor memories. *Read-only memories* (ROM's) are those from which data is normally only retrieved. *Read/write memories* (R/WM's) or *Random-access memories* (RAM's) are those into which data can be loaded or from which information can be retrieved, each with equal facility. ROM's are factory programmed with fixed data which cannot be changed.

Some ROM's, called PROM's, can be permanently programmed by the user. Others, called EPROM's, can be programmed by the user and then erased by exposure to ultraviolet light. After erasure, EPROM's can be reprogrammed. RAM's can be loaded with information, read, or reloaded electronically, depending on the logic states of the memory cell's READ and WRITE control lines.

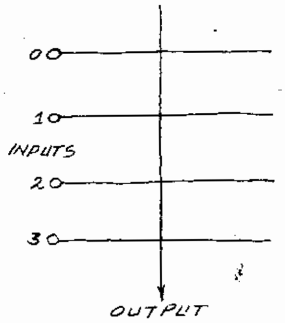


Fig. 1. PROM grid that can be used to simulate a NAND gate.

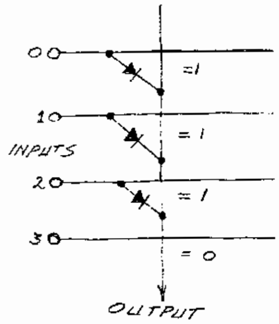


Fig. 2. 4X1 PROM programmed for 2-input NAND gate.

Both types of semiconductor memories store information in the form of binary digits, abbreviated as bits, which have two possible states—logic 0 or logic 1. The stored data can be arranged as hundreds or even thousands of bits or combinations of bits called words. Words comprising four bits (*nibbles*) or eight bits (*bytes*) are the most common, but many other word lengths are also used.

Programmable Diode ROM's. An excellent way for the novice to learn more about ROM's is to assemble a programmable ROM or PROM that uses diode memory elements. A PROM of this type consists of a grid or array of input and output wires called *lines*. A logic 1 is loaded into the ROM by bridging the intersection of an input and output line with a diode. The absence of a diode at an intersection yields a logic 0.

You can use a simple diode PROM to simulate logic gates and combinational logic networks. The first step in designing a PROM for this purpose is to write the truth table for the gate you want to simulate. The truth table for a two-input NAND gate, for example, is

	Inputs		Output
	A	B	
0	0	0	1
1	0	1	1
2	1	0	1
3	1	1	0

This truth table has four possible input combinations and only one output for each set of inputs. Therefore, our PROM will be a 4 by 1 grid of lines as shown in Fig. 1. The truth table is loaded (programmed) into the PROM by placing a diode at the intersection of the output line and the line for each input, which results in a logic-1 output. The programmed array is shown in Figure 2. Figure 3 shows how to demonstrate the operation of the PROM with the help of a

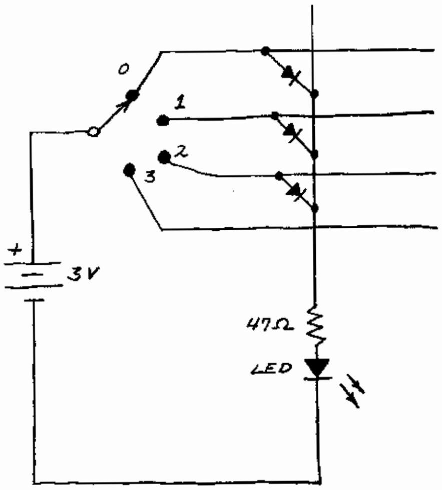
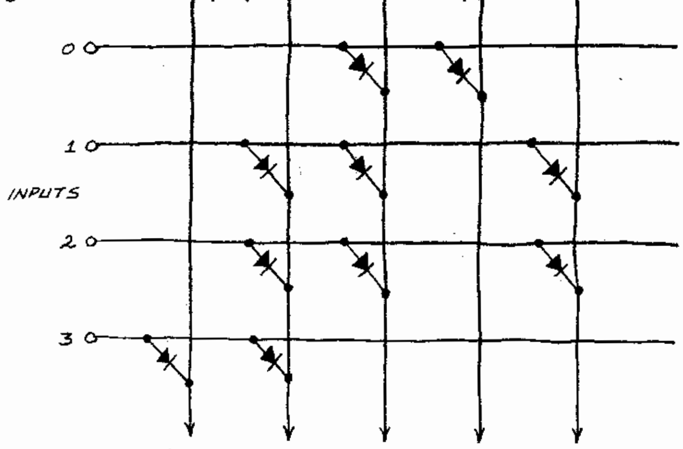


Fig. 3. Circuit to demonstrate the PROM in Fig. 2.



INPUTS	AND	OR	NAND	NOR	XOR
0-- 00	0	0	1	1	0
1-- 01	0	1	1	0	1
2-- 10	0	1	1	0	1
3-- 11	1	1	0	0	0

Fig. 4. Multiple function diode PROM.

battery, a LED, and a four-position switch.

Of course, our simple PROM version of the NAND gate is a trivial example of a read-only memory application. This is particularly true because the diodes aren't even necessary! Logic 1's can be represented simply by connecting the appropriate input lines to the output line. However, diodes are essential when the PROM becomes more sophisticated. For example, Fig. 4 shows a diode PROM that simulates the AND, OR, NAND, NOR, and EXCLUSIVE OR gates. Mass confusion would result without diodes because electrical current would thread its way through the wrong sections of the PROM via *sneak paths*. Diodes eliminate sneak paths because they pass current in only one direction.

Diode PROM Character Generator. Do you want to gain some hands-on experience with PROM's? Then invest some spare time and about three dollars building the diode PROM shown in Fig. 5. This simple PROM is connected as a seven-segment character generator. It allows you to generate up to ten characters including the digits 0 through 9, many letters of the alphabet, and a variety of unusual symbols.

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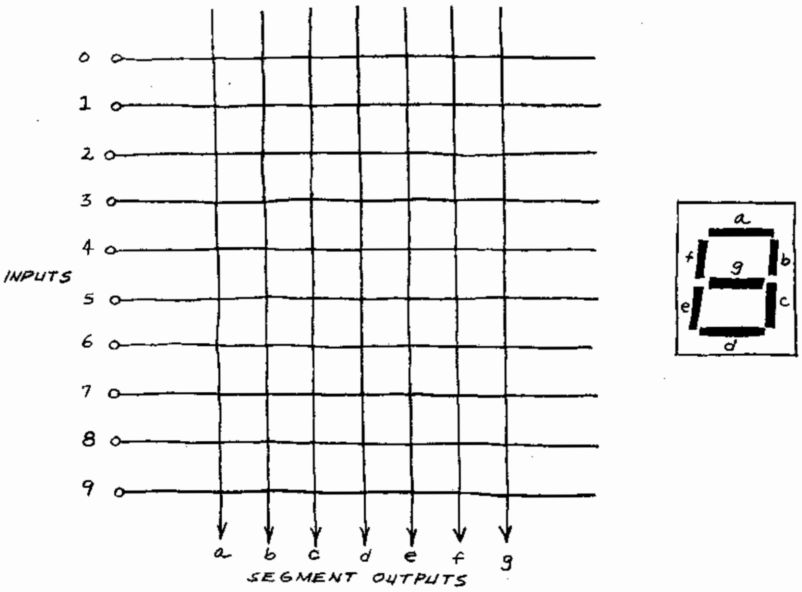

Fig. 5. Seven-segment display character generator diode PROM.

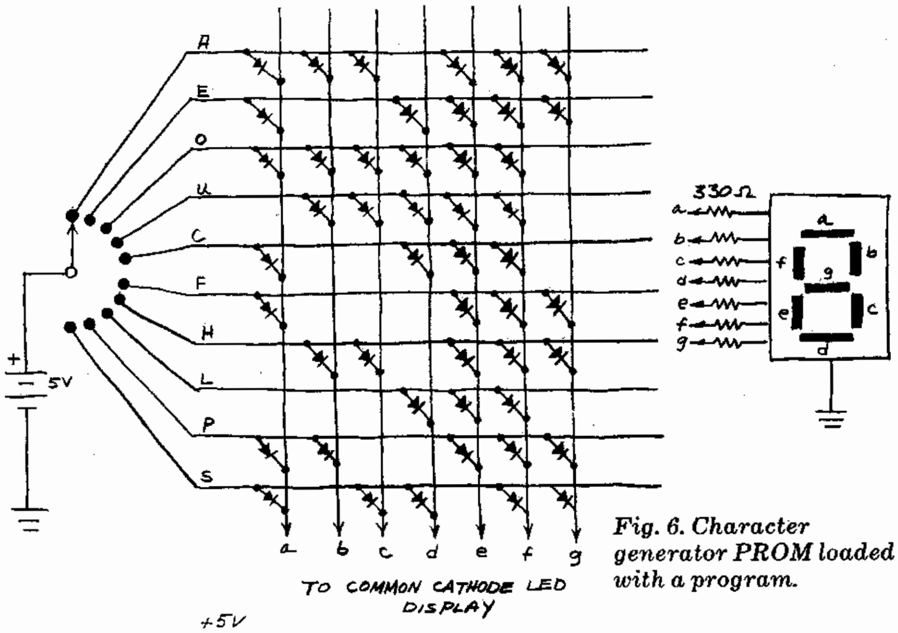

Fig. 6. Character generator PROM loaded with a program.

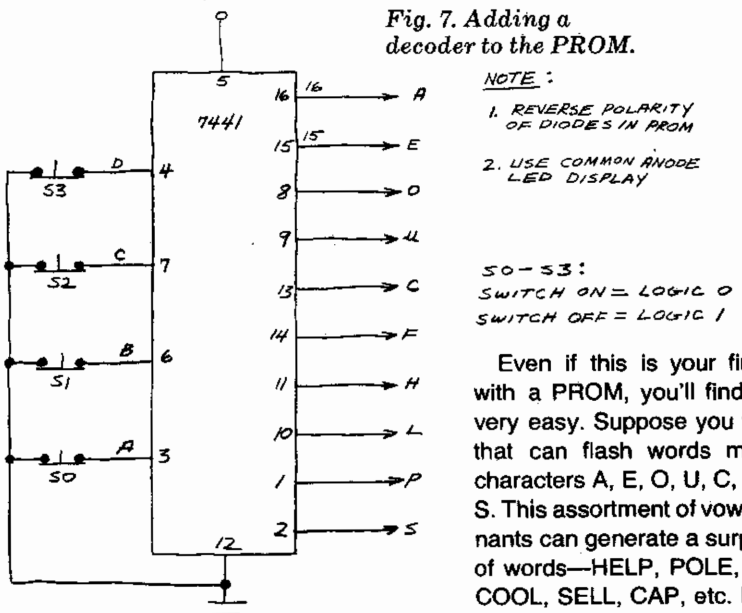

Fig. 7. Adding a decoder to the PROM.

Even if this is your first experience with a PROM, you'll find programming very easy. Suppose you want a display that can flash words made from the characters A, E, O, U, C, F, H, L, P, and S. This assortment of vowels and consonants can generate a surprising number of words—HELP, POLE, PULL, HOLE, COOL, SELL, CAP, etc. First, you write a truth table that shows the segments of the display that must be illuminated to produce each character.

Character	a	b	c	d	e	f	g
A	1	1	1	0	1	1	1
E	1	0	0	1	1	1	1
O	1	1	1	1	1	1	0
U	0	1	1	1	1	1	0
C	1	0	0	1	1	1	0
F	1	0	0	0	1	1	1
H	0	1	1	0	1	1	1
L	0	0	0	1	1	1	0
P	1	1	0	0	1	1	1
S	1	0	1	1	0	1	1

(Header above a–g: **Segments**)

This prom has ten input and seven output lines, so it requires a grid of 10 by 7 wires. The PROM is programmed by inserting a diode at the intersection of each character and segment line where a logic 1 exists in the truth table (Fig. 6). Simple, isn't it? If you're not convinced, try designing the same character generator with logic gates!

We can improve the character generator PROM by replacing the manual selector switch with a BCD-to-decimal decoder. True, this adds an IC, but reduces the number of input lines from ten to four and makes it possible to interface the PROM with other circuits. Figure 7 shows how the decoder is connected to the PROM.

You can assemble a working version of this diode PROM on a perforated board. Insert flea clips at each bit position and run the input and segment lines on opposite sides of the board to prevent shorts. The flea clips will allow you to insert and remove diodes. If you want to go first class, permanently wire a diode in series with an spst toggle switch at each bit position. Turning the switch on will load a logic 1. Placing the switch in the off position will load a logic 0. If you choose to do this, you'll need seventy switches, so be sure to shop around for a good price.

In any event, I hope you'll build a working diode PROM if you're interested in learning about the practical aspects of ROM's and PROM's. You'll learn something about *hardware* (the PROM and decoder), *software* (the truth table you plan to load into the PROM), and *firmware* (the truth table loaded in the PROM in the form of diodes). You'll also learn about *addressing* (the 4-bit character select word applied to the input of the decoder). All of these topics are fundamental to an understanding of advanced digital logic devices like microprocessors, calculators, and hobby computers. ◇

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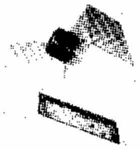

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☐ LIFESCREEN FRONT SURFACE MIRROR, 8" x 10" . . . . @ $20.00
☐ LIFESCREEN FRONT SURFACE MIRROR, 14¾" x 20" . . . . @$30.00
☐ EXTRON LS 50 SCREEN 32" x 40"/50" Diagonal . . . . @$90.00
☐ COMPLETE LIFESCREEN I PACKAGE . . . . @ $269.00
☐ COMPLETE LIFESCREEN II PACKAGE . . . . @ $299.00
All Prices F.O.B. factory – Cal. residents add 6% sales tax. TOTAL: $ ______

EXTRON LIFESCREEN® PROJECTION SYSTEM
8831 Sunset Boulevard,
West Hollywood, California 90069
Name ______
Address ______
City ______ State ______ Zip ______
CARD NAME ______
CARD NUMBER ______ EXPR. DATE ______
INFO PAK – 50c

CIRCLE NO. 27 ON FREE INFORMATION CARD