Inductor simplifies memory-driver circuit

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Designing memory systems with 4,096-bit n-channel random-access memories poses a number of problems with the associated interface circuitry. But a small inductance can at least eliminate the headache of having an extra power supply in the memory driver.

While most of such RAMs on the market today have inputs—all addresses, data-in, chip-select, and read/write—that are compatible with transistor-transistor logic, the clock or chip-enable clock input requires 0 to 12 volts for proper memory operation. Of particular concern is the memory's clock input, where a minimum high level of 11.4 V is required.

A common totem-pole output driver circuit—similar to the SN75365 or MC3960 initially used with p-channel RAMs—tied to a number of n-channel-RAM clock inputs, is shown in (a). Capacitive loading is typically 390 picofarads per clock driver. When $V_2 = V_3 = V_{DD}$, the outputs appear degraded, and $V_{OH} = V_{DD} - 1$ V at $I_{OH} = 50\ \mu A$. Increasing V_3 to $V_{DD} + 3$ V changes the output to a more acceptable level, normally $V_{DD} - 0.3$ V at $I_{OH} = 100\ \mu A$.

However, in n-channel systems, the values of V_{DD} and V_{CC} are usually 12 V and 5 V, respectively. If the method of increasing V_3 is used, V_{DD} must be raised to 15 V for V_3 and then dropped back down to 12 V for V_2 and other parts in the system to generate a separate supply voltage on each array card. The alternative is for a separate supply voltage to be bused in for V_3. These methods, while feasible, are not very practical because of increased power consumption and cost.

A way to provide the correct output levels for both chip and driver with only a +12 V supply is to place an inductor from V_3 to V_2. The inductor overcomes the drawbacks of operating with $V_3 = V_2$ without adding a supply greater than V_{DD} to the system, as shown in (b). The inductor provides an energy source in the form of a voltage "kick" whenever the output totem pole is in a transition state. The increased voltage on V_3 supplies the additional current needed as E_{out} changes from low to high, resulting in a smooth and uninterrupted transition to V_{OH}.

A small value of L will not provide an adequate voltage increase at V_3, while too large a value will not recover fast enough at high repetition rates. Values between 36 and 100 microhenries work well at a pulse width of 500 nanoseconds and repetition rates of 1 microsecond or less. □