DIGITAL INTEGRATED CIRCUITS

PART FOUR

microelectronics

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ONE apparent drawback of using semiconductor integrated circuits is that the user cannot have any control over the actual circuitry of the device he intends to use. Therefore, he must think in terms of building blocks; instead of designing circuits around components, he must now design systems around the circuits. In many cases this makes life a lot simpler, but nevertheless the long term implications are tremendous.

Those users already converted usually look upon integrated circuits as a method of removing the tedium of wiring routine repetitive circuits, thus allowing more sophisticated thought to the overall design of the equipment being built.

As the prices of integrated circuits are rapidly approaching the prices of individual transistors, the experimenter can get more "electronic function" for his money, and can therefore involve himself in systems much more complex than those he has previously been used to.

As it was felt early on that integrated circuits would have to be manufactured on a really large scale to obtain cost benefits, the original manufacturers decided to make circuits which could be standardised most easily, and would be in most demand. Undoubtedly the most commonly used electronic circuits are switching circuits, flip-flops, and logic gates, therefore most low cost circuits fall into this category.

The fact that there are only a few possible combinations of components to make these circuits has resulted in a natural standardisation between manufacturers, and although there are many manufacturers, the types of logic circuits they make usually fall into any of four or five main groups. A point worth mentioning here is that although the same types of circuit may be offered by different manufacturers, it does not necessarily imply that the terminal connections are the same.

Linear (or non-digital) circuits are not nearly so easily standardised as any constructor will know. For example there are innumerable ways in which one can wire up an audio amplifier stage to give either similar, or subtly modified performances. For this reason the numbers of amplifiers available are not nearly so great; the prices are usually higher than for digital circuits.

FOUR COMMON FAMILIES

The four most common families of circuit to be encountered at present are RTL (resistor transistor logic), DTL (diode transistor logic), TTL (transistor transistor logic), and ECCSL (emitter coupled current steered logic). In nearly all these families the unit block is either a NAND or a NOR gate with anything from one to six inputs. Most circuits are available as multiple gates, the controlling factor being the number of inputs and gates per package. For example, one package might contain four independent gates each with two inputs, or two gates each with four inputs, and so on. The other standard circuits common to all families are bistable, and monostable multivibrators of various types.

It is the basic gate which determines the family, and examples of each of the four main types are shown in Figs. 15 to 18. Generally speaking the user need not worry too much about the actual circuitry of the package, but he should know the overall characteristics of each type in relationship to each other, as this could affect the choice of family for a given application.

RESISTOR TRANSISTOR LOGIC

RTL was one of the very first families of circuits to be made, largely due to its comparative simplicity and ease of manufacture. Because of this it is now one of the cheapest types of circuit available on the market.

Operation of the gate is very easy to understand (see Fig. 15a). If any input is in a "high" state, i.e. has a logical "1" or a positive potential applied to it, the output will fall to level "0". Only when all inputs are at level "0" will the output rise to level "1". The operating function of the gate is therefore NOT OR or NOR.

This description of the function of the gate is usually written on data sheets in the form of a "truth table", which shows the condition of the output for all possible combinations of logic levels at the input.

This is sometimes expressed on data sheets in Boolean algebraic form. For example, $D = \overline{(A + B + C)}$, which simply means D is not equal to A or B or C. Both these expressions are common to any three-input NOR gate irrespective of the circuitry, and therefore it is possible to write a symbol which can be used in logic diagrams of systems to show that the gate required is of the NOR type (see Fig. 15b).

Although it is doubtful if the amateur would be worried by limitations in speed, it is worth noting that with RTL a compromise has to be drawn between the propagation delay of a gate, and its power dissipation. It is always desirable to keep power dissipation low as in large computer systems, which may involve thousands of such gates, the overall power consumption can be

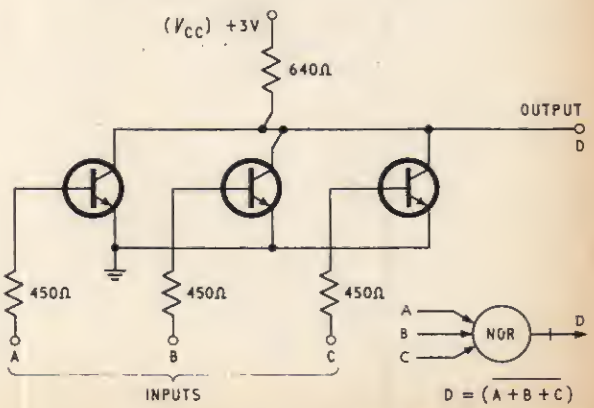


Fig. 15a. A typical RTL NOR gate

Fig. 15b. Logic symbol for NOR gate

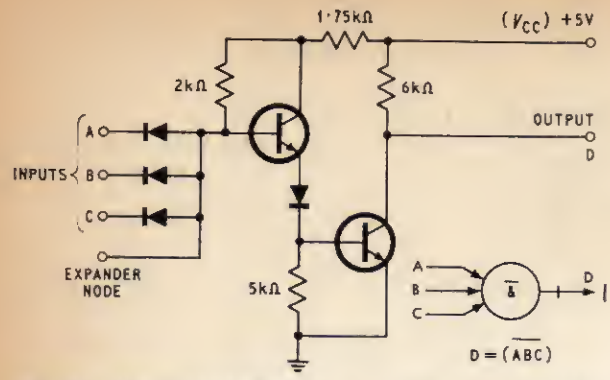


Fig. 16a. Basic DTL NAND gate *Fig. 16b. Logic symbol for NAND gate*

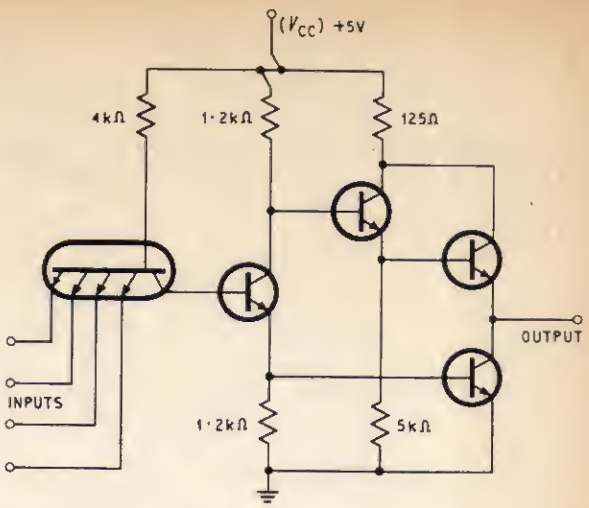


Fig. 17. Basic TTL NAND gate

enormous. Unfortunately, to reduce the power dissipation of RTL, it is necessary to increase all the resistance values proportionally. This immediately reduces the switching speed of the gate as the capacitance of the output has a larger resistive load through which to discharge.

This problem can be overcome by bypassing the input resistors with capacitors which act as a low impedance path to the pulse without upsetting the transistor bias conditions. It is undesirable to include capacitors in integrated circuits, and to achieve this faster switching speed involves greater costs.

A further point worth mentioning is that the driving current for any gates connected to the output of a particular stage has to be supplied via the collector load resistor of the driving stage. There is thus a maximum number of gates which can be driven successfully by a single stage, and this is again proportional to the value of the resistive load, and indirectly proportional to the switching speed.

Typical parameters of RTL gates are as follows:

Power requirements (V_{cc})	+3 to +5V
Power dissipation (per gate)	12mW
Propagation delay (per stage)	15ns
Fan-out (per gate)	5
Fan-in	2 to 4
Flip-flop frequencies	20MHz

An important feature of all types of gate is "noise margin". This is the difference in voltage between the state of an input, and the voltage necessary to make the gate change its logical state. There are many arguments as to what "noise margin" actually is, but it can be considered as a "safety margin" between the triggering levels of a gate. In general, the larger this margin the better.

With all types of gate this safety margin is reduced as the fan-out load is increased and consequently if systems involving large numbers of fan-outs are required, the noise margin of the gate must be as large as possible to prevent accidental triggering from spurious signals. RTL unfortunately does not have a good noise margin compared with other systems; therefore, fan-outs should be kept down to five or less. The typical value of noise margin for RTL is 300mV.

DIODE TRANSISTOR LOGIC

A more sophisticated gate is the diode transistor logic (DTL) gate shown in Fig. 16. Again this is a very popular circuit, and consequently is relatively low priced, but it has certain advantages over RTL.

The most immediate difference is that the input resistors of RTL are dropped in favour of multiple diodes. This is a much more satisfactory circuit to make in integrated circuit form for the reasons stated previously. A secondary advantage of this form of input is the ease with which fan-in can be expanded merely by paralleling further diodes to the direct entry point, or common node.

The effect of the first transistor, and the coupling diode, is to improve the noise margin of the gate, and the second transistor gives signal inversion (NOT function) as well as acting as a driver for subsequent stages. The overall function of such a gate is NAND.

An important feature of this NAND gate is the way in which it is possible to parallel the outputs of several gates to carry out the OR function between gates with no extra components. This operation is called "wired OR", and can save a considerable number of components in some types of system.

The power dissipation per gate is relatively low, and fan-outs are high, thus making it an ideal all round gate for universal applications.

Typical parameters are:

Power requirements (V_{cc})	5V
Dissipation (per gate)	16mW
Propagation delay (per stage)	25ns
Fan-out (per gate)	8
Fan-in (using expander diodes)	Up to 20
Flip-flop frequencies	8 or 20MHz
Noise margin (typically)	1V

TRANSISTOR TRANSISTOR LOGIC

A neck and neck runner with DTL in the popularity race is transistor transistor logic (TTL). This is sometimes called T^2L.

Referring to Fig. 17 it can be seen that the diode inputs are replaced with a multiple emitter transistor. Each emitter acts as a diode but, as they are coupled to form the active part of a transistor, gain is injected which helps towards enhancing the noise margin. This stage is followed by a phase splitter, which drives two output transistors operating in push pull.

As with DTL the overall function of the gate is NOT AND (NAND), but the advantage it holds over DTL is its

very low output impedance both in the "1" and "0" condition. This means that the gate can be used to drive relatively high capacitance loads without seriously affecting the switching speed, or alternatively the fan-out can be considerably greater.

Unfortunately this advantage has to be paid for at the expense of power dissipation which is relatively high, and rises as the pulse repetition frequency increases. This increase in dissipation is caused by the fact that on one portion of the switching cycle both output transistors are conducting simultaneously for a short period, thus giving a short circuit path to earth. As the mark/space ratio between consecutive pulses decreases, the effect of the short circuit condition becomes more marked.

A secondary effect caused by the same action is that of current "spikes" being fed back down the power lines, which in the worst case could trigger other gates if the spikes exceeded the noise margin. This problem is only likely to occur in complex systems, and can be avoided by carefully decoupling power lines between stages.

Typical parameters of TTL gates are:

Power requirements (V_{cc})	+5V
Dissipation (per gate)	22mW
Propagation delay	25ns
Fan-out (per gate)	15
Fan-in	4
Flip-flop frequency	20MHz
Noise margin	1V

It is not possible to expand the fan-in by coupling extra diodes, neither is it possible to carry out wired OR due to the very low output impedance in both states.

CURRENT MODE LOGIC

So far we have dealt with one group of logic circuits which are all "saturating" circuits. This means that the two states are defined by a transistor being either switched hard on or off. When this happens voltage swings tend to be in the same order as supply voltages (3 to 4 volts). This causes a substantial reduction in switching speeds as any stray capacitance in the circuit has to charge to this voltage before switching can occur.

For most amateur applications the switching speeds mentioned so far for RTL, DTL, and TTL would be more than adequate. The requirement for increased switching speed brought about the development of non-saturating logic, which has very low voltage swings giving overall propagation delays for gates as small as 1·5ns. Fig. 18a shows such a circuit. This circuit configuration is called emitter-coupled current-steered logic (ECCSL) or sometimes current mode logic (CML).

The circuit (Fig. 18a) is similar to a differential amplifier, the transition between the "1" and the "0" state being defined by the reference voltage V_b. When the gate input transistor bases are below this reference the current from the common emitter resistor flows through the reference transistor. When any of the inputs rise above the reference voltage the current will be steered through the resistive collector load of the input transistors. This causes the output $\overline{D}$ to go negative, and D to go positive.

The overall function of such a gate is OR or NOT OR (NOR) depending on which output point is used. As the logic levels are relative to the reference voltage it is very important that this reference voltage is stable. In practice this voltage is obtained from a simple regulator circuit which resembles a Zener diode stabiliser built into the chip.

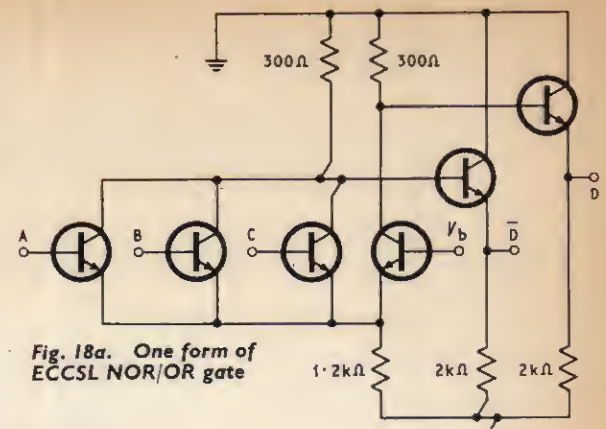
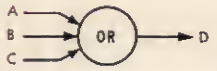


Fig. 18a. One form of ECCSL NOR/OR gate



D = A + B + C *Fig. 18b. Logic symbol for OR gate*

Two conventional diodes are used to generate this reference voltage from the forward voltage drop across them which is approximately 1·1V. This forward voltage drop is temperature dependent, which is why the stabilising circuit is built into the chip. Any changes in temperature will affect the circuit as a whole, and to a certain extent the effect will be neutralised. Nevertheless this circuit cannot withstand wide variations of temperature.

Noise margin is very low, and power dissipation is high as current is always flowing through one collector load or the other.

The circuit has been mentioned here for general interest, but it is not to be recommended for general amateur use unless ultra high speed is absolutely essential.

BISTABLE ELEMENT

A very important circuit to the logic user is the flip-flop, or binary element. Every range of gates whether it be RTL, DTL, or TTL has associated with it one or two types of flip-flop. At first sight these are most formidable looking circuits compared with the straightforward Eccles Jordan types of circuit with which we are more familiar.

The simplest form of bistable element is the RS (reset/set) type. This can be made by cross-coupling two 2-input NOR gates as shown in Fig. 19. If a pulse is applied to one of the inputs, the element will take on a condition where one output will be high, and the other low. This condition will be held indefinitely until a pulse is applied to the other input, when the circuit condition will be reversed. These conditions can be shown in the truth table below:

Table 1. TRUTH TABLE FOR TWO NOR GATES

Input R	Input S	Output Q	Output $\overline{Q}$
0	0	Dependent on switch-on condition	
1	0	1	0
0	1	0	1
1	1	Indeterminate	

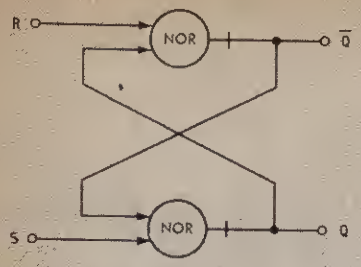


Fig. 19a. Logic diagram of an RS flip-flop using two cross-coupled NAND gates

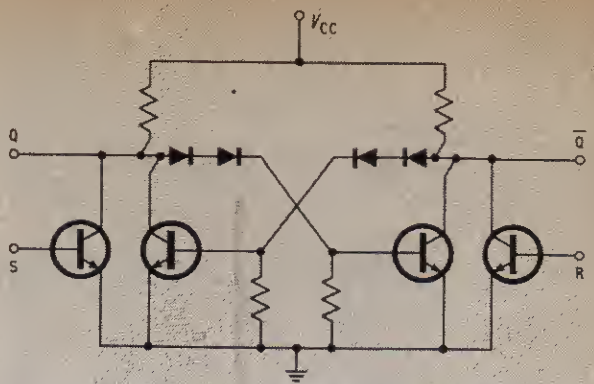


Fig. 19b. Typical circuit of an RS flip-flop

When both inputs are simultaneously at condition "1" there is no set rule for the output, as this will be dependent on the internal parameters of the components giving rise to an ambiguous condition. This is an undesirable state of affairs; therefore, the circuit has to be modified to prevent ambiguity and to ensure that when "1" appears simultaneously on both inputs the bistable will change state irrespective of its previous condition. This type is called a "J K flip-flop".

It is usual in a system to command the flip-flop to change state with a "clock" or command pulse. To do this the J K inputs are each gated through an AND gate with the clock pulse.

Fig. 20 shows the block logic diagram of such a circuit. There are J, K, R, and S inputs, and a clock input. With such a unit it is possible to make binary divider chains, shift registers, ripple counters and ring counters by arranging the input and output connections accordingly.

By cascading four binaries with suitable feedback it is possible to make a scale of ten counter. Some manufacturers actually offer complete counting chains and shift registers in a single chip of silicon, which would be housed in the same size package as a single binary. While these steps to large scale integration are at present comparatively expensive, it is easily foreseeable that in the next year or so a complete scale of ten counter will cost very little more than a single binary element using discrete components.

There are many special types of logic circuits available within each family: inverters, buffers, power gates, monostables, and gate expanders. In the main these are self-explanatory, but it is worth mentioning that some of the power gates and buffers are quite capable of driving low power indicator lamps or relays. These should, however, be used with care and limiting currents should not be exceeded. One must remember that while it is a comparatively cheap matter to replace a single transistor in a conventional circuit when it has been overloaded, the whole of the integrated circuit is scrap even if the only fault is a damaged output transistor. On the whole, however, integrated circuits are very tolerant, and manufacturers go to great lengths to make them immune to such effects as short circuits between terminals.

Next month: Linear amplifying circuits

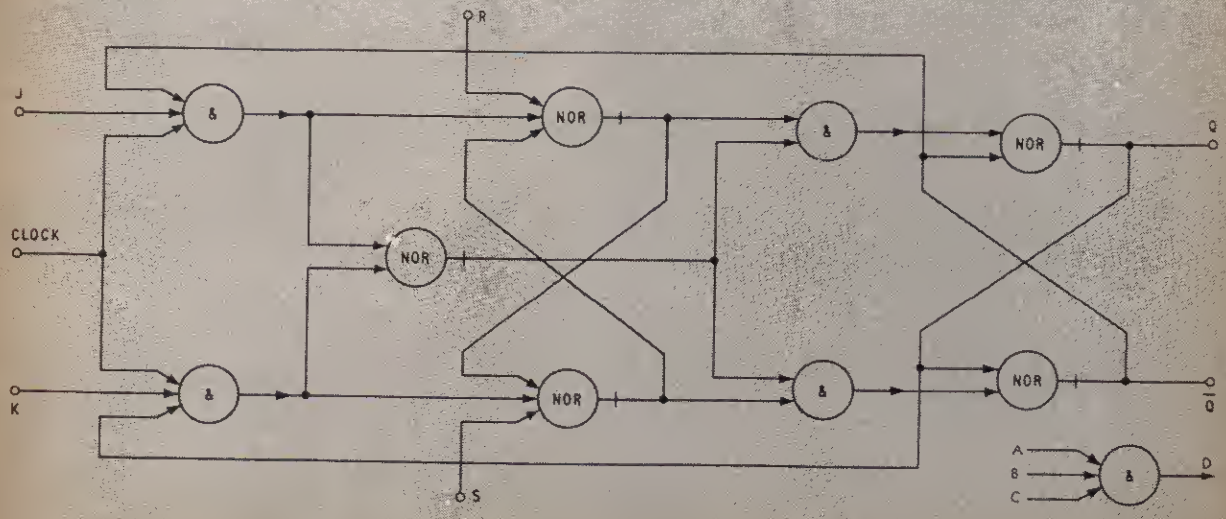


Fig. 20a. Logic diagram of the JK binary

Fig. 20b. Logic symbol of an AND gate