New Electronics

N° and issue date : 31111 - 12/11/2003
Circulation : 24000
Frequency : Fortnightly
NewElectronics_31111_56_306.pdf
Web Site: http://www.findlay.co.uk
Page : 56
Size : 100 %

"It's even more important for them to understand at the outset what their options really are in tracking down and solving problems."

ANALOG DEVICES

Sponsored Tutorial

For more, go to www.analog.com/processors/processors/blackfin/index.html.

The art of

Processor debug features contribute to design success. By **David Katz** and **Rick Gentile**.

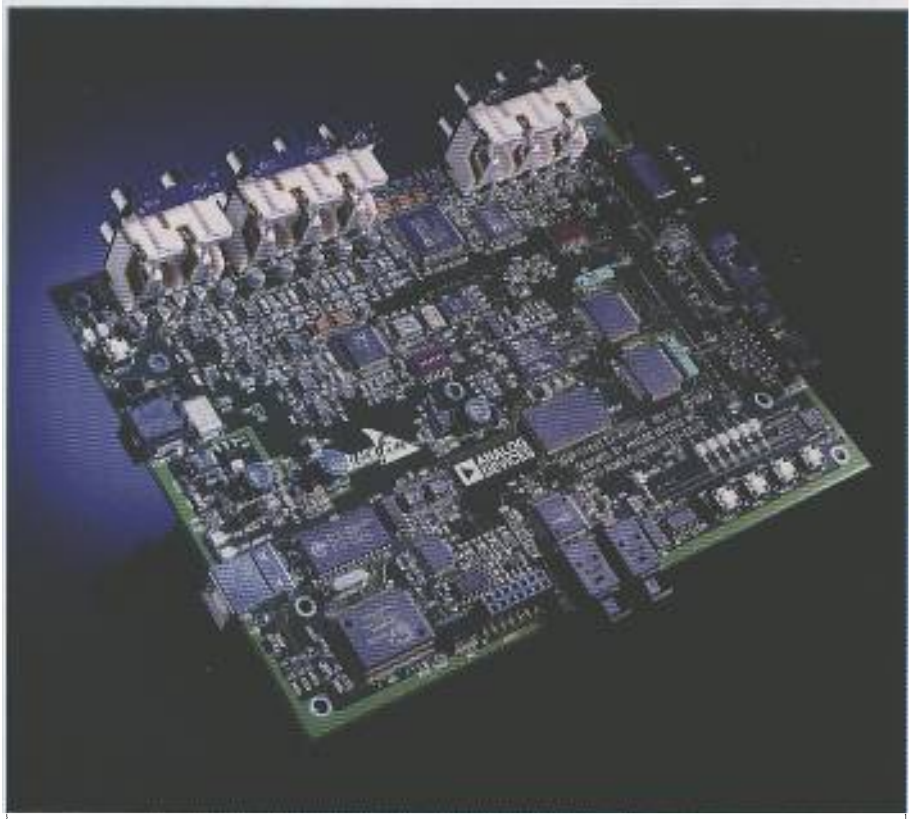
As embedded processing applications grow more complex and time to market demands increase, the 'art' of debugging grows ever more critical. As important as it is for developers to have debugging tools at their disposal, it's even more important for them to understand at the outset what their options really are in tracking down and solving problems in their application.

Software tools

Software tools perform two important roles in system development. First, they allow development to begin before custom hardware is available. Algorithms can be simulated from a functional standpoint, whilst performance can be estimated at an early stage in the development process using cycle accurate core simulation.

Several key features in the Blackfin VisualDSP++ tools suite allow a software developer to predict the performance that will be achieved on the eventual target. Because the Blackfin architecture fundamentally supports efficient compiled code, most development can be performed in C or C++. This allows existing code to be integrated quickly into the project and facilitates many design decisions without delving into architectural details.

Once the initial project is built, several simulation options allow a tradeoff between cycle accuracy and simulation speed. VisualDSP++ provides code profiling capability as part of both



Algorithms and most peripherals can be exercised using an EZ-KIT Lite evaluation platform.

Copyright (New Electronics N° 31111) No reproduction without authorisation

New Electronics

N° and issue date : 31111 - 12/11/2003
Circulation : 24000
Frequency : Fortnightly
NewElectronics_31111_56_306.pdf
Web Site: http://www.findlay.co.uk
Page : 57
Size : 100 %

debugging

its simulator and its emulator. This allows a programmer to visualise how time is being spent within different parts of an application, which provides focus in the optimisation effort.

Even though the Blackfin compiler performance is outstanding for signal processing and mcu applications (low cycle count, low byte count), some sections of code can be further optimised using assembly based libraries. While this should be uncommon in a large development project, the VisualDSP++ simulator provides a Pipeline Viewer to identify stalls graphically – furthering the optimisation effort.

The Blackfin instruction pipeline is interlocked, so stalls do not have to be tracked manually and managed by the programmer. Even so, the ability to see a stall in a critical section of code usually allows the programmer to make a small adjustment and thereby obtain a dramatic improvement in cycle count.

Another handy feature of the simulator is the Cache Viewer. With the ever present trade offs that system designers must make between on and off chip memory sizes, the Cache Viewer can be invaluable in predicting how the cache will perform based on the instruction flow, as well as showing how data is actually accessed.

Hardware platform

Once the overall system has been simulated, algorithms and most peripherals can be exercised using a low cost EZ-KIT Lite evaluation platform. This gives developers a way to evaluate a Blackfin processor for audio, video and other processing intensive algorithms.

A USB debugger interface provides access to the VisualDSP++ pc hosted tools suite and, for higher performance, a boundary scan in circuit emulator (ICE) can be connected.

An EZ-Extender daughter card for the ADSP-BF533 EZ-KIT allows high speed converter evaluation boards (a/d converter, mixed signal and d/a converter), cmos image sensor evaluation boards and some tft lcds to be attached. It also provides a breadboard area for circuit staging and most pins of the Blackfin Processor are available for probing.

Chip level tools

The Blackfin architecture provides built in hardware debugging features. These include the Performance Monitor, Cycle Counter, Watchpoint Unit and Trace Unit.

• Performance monitor

Each Blackfin processor has two registers that can be programmed to count occurences of specific 'performance centric' events. There are 35 unique events that can be tracked, summarised in Table 1.

Developers can use performance monitoring events to find focus areas for the optimisation process. Rather than predicting these events through simulation, Performance Monitor provides insight into what is happening at the silicon level.

Take, for example, data and instruction cache performance. Performance Monitor provides information based on cache misses for both data and instructions. Knowing the cache miss rate, a programmer can move data and instructions around interactively in memory using VisualDSP++ Expert Linker until maximum performance is achieved.

Another example of how Performance Monitor can be helpful involves how the core and the direct memory access (dma) engine interact when accessing internal memory banks.

Blackfin processors have an integrated dma controller that allows efficient data movement without core interaction. The core sets up the transfers and is notified when a data buffer is ready for processing. The processor core and dma controller can access different sub banks of memory in the same cycle, but when they attempt to access the same sub bank in the same cycle, one of the accesses must stall.

In system flows with heavy core memory accesses in parallel with multiple dma channel accesses, it is important to know when the dma and/or core are stalling due to attempts to access the same memory sub bank. Performance Monitor counts these events so the developer can optimise data allocation in memory.

• Cycle counters

Blackfin also features a 64bit cycle counter that tracks all execution cycles, including pipeline activity such as stalls. It is a useful tool for determining execution time of a given algorithm. Cycle count can be converted to time by dividing the number of cycles by the processor's core clock speed. The core simulator for Blackfin processors is cycle accurate and a cycle count obtained on the simulator is designed to match the count measured on actual hardware when running from internal Level 1 memory.

• Watchpoints

The Watchpoint unit provides more debug flexibility. It monitors both instruction bus and data bus addresses, generating an exception after a particular address or address range occurs for a specified number of times. This is a handy way to trap errors or optimise code, triggering an event based on actual bus activity.

Another practical feature is 'code patching' – the process of running new code in lieu of existing code. The Watchpoint Unit can be configured to trigger an exception when the old code's start address has been reached, and then the exception service routine jumps to the memory location where the new code resides.

• Trace buffer

The Trace unit stores a history of recent processor activity by logging the last 16 changes in program flow. An exception can be generated when the Trace Buffer is full, thus allowing the user to create a complete log of program sequencer activity from the point the unit was enabled. The unit is intelligent enough to selectively ignore flow changes that match the last one or two buffer entries, so that a tight loop won't cause a Trace Buffer overflow.

Clearly, for embedded processors like those in the Blackfin family, there is a wealth of debugging features available. By using these software and hardware tools, as well as using on chip debug functionality intelligently, designers can shorten their product development cycles and gain a better understanding of the inner workings of their systems. NE

Table 1: Event tracking with Performance Monitor

Event	Description
Loop count	Provides insight into loop efficiency
Branch counter	Tracks number of branches made
Stalls	Counts stalls of all types
Data cache misses	Provides data cache hit/miss rate
Instruction cache misses	Provides instruction cache hit/miss rate
Core/dma collisions to memory banks	Provides insight into core and dma conflicts

Author profiles:

David Katz and Rick Gentile are senior Blackfin applications engineers with Analog Devices.

Copyright (New Electronics N° 31111) No reproduction without authorisation