

## How to recover a pulse signal with a large capacitance load

Chenan Tong, Texas Instruments

In some applications, it is necessary to transmit square waves across a long cable. Long cables, however, typically have high capacitance, which can significantly affect the signal's wave shape. As such, the signal's frequency and duty cycle need to be maintained if the signal is to remain free from distortion. This Design Idea discusses this phenomenon and offers a simple solution.

Figure 1 illustrates a common solution used to reconstruct a square wave at the end of a long cable (47-pF cable capacitance).  $V_{IN0}$  is the signal to be transmitted. The signal at  $V_{IN1}$  represents the signal at the end of the cable. You can see that this signal is distorted by the charge and discharge of the parasitic capacitance of the cable. Furthermore, the gate (IC<sub>2</sub>) sees the rising and falling edges differently, so the reconstructed output signal will not be an accurate representation of the original digital signal.

The results in **Figure 2** show that you cannot recover input pulse with a simple logic gate. You need to find a different method to detect the rising and falling edges of the digital circuits. A differentiator can be used to detect the square-wave edges because the output of the RC circuit rises after the rising edge and falls after the falling edge of the square wave. Remember that the differentiator output is proportionate to the rate of change of the output signal, so it moves positively for increasing signals and negatively for decreasing signals.

The design in Figure 3 uses a differentiator. Figure 3 also shows the



simple gate solution  $(IC_2)$  for comparison. In this example circuit, you can see how the simple gate solution does not

effectively solve the problem. Note that the signal at  $V_{\rm INI}$  is from the charging and discharging of  $C_2$  times  $R_6$ . In this



Figure 2 Simulation results for the common pulse reconstruction show that you cannot recover the input pulse with a simple logic gate.



example,  $C_2$  is 470 pF, or 10 times larger than the example in **Figure 1**. When the input pulse is high (after the rising edge), the capacitor voltage increases. The differentiator output is negative for increasing capacitor voltage. When the input pulse is low (after the falling edge), the capacitor voltage decreases. The differentiator output is positive for increasing capacitor voltage.

Thus, by differentiating the RC sig-

nal you can reconstruct a signal that more closely resembles the original square wave. A comparator follows the differentiator output to create a sharp square-wave output.

**Figure 4** shows the simulation results for the circuit in **Figure 3**. The input signal is a 20-kHz square wave with a duty cycle of 20%. The output of IC<sub>2</sub> clearly does not reproduce the original signal. In fact, IC, does not even detect



Figure 4 In these simulation results for differentiator-plus-comparator reconstruction, the differentiator output looks like a smoothed inversion of the original digital signal.

most of the pulses. The differentiator's output looks like a smoothed inversion of the original digital signal. The comparator converts the differentiator output to a sharp square wave that accurately matches the frequency and duty cycle of the original signal. Specifically, the overall error in the duty cycle for this example is approximately 10%.

With this circuit, you can easily implement pulse recognition after a long cable and heavy capacitance load. This method produces pulse transmission with low distortion so that the frequency and duty cycle of the original signal are preserved.EDN

## ACKNOWLEDGMENT

Special thanks to Arthur Kay and Matthew Hann of Texas Instruments for contributing their technical expertise in this subject area.

## REFERENCES

 "Tutorial 7 of 8: The Op-amp Differentiator Amplifier," Electronics-Tutorials.ws, http://bit.ly/PT8kLM.
OPA365 data sheet, Texas Instruments, http://bit.ly/UNNAWp.