

# Pulse-width modulator has digital control

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In this Design Idea, the total time period of an output pulse's width is 16 times the pulse width of the input clock. The input clock connects to a binary counter (Figure 1). The output of the binary counter then goes to a decoder. The decoder scans the signal such that the first output of the decoder goes to an inverter gate and then to the counter. The output of the counter then goes to one as soon as the signal to the counter goes from zero to one and then from one to zero.

The multiplexer decodes the output pulse width's time to be in the on state. The first output of the demultiplexer sets the output of the counter, and the next outputs clear the output of the counter. The multiplexer, a 14067, selects the clearing signal. Upon the 0th input of the multiplexer, the PWM (pulse-width-modulator) out-

put becomes zero because the setting time and clearing time become nearly

zero. The last input of the multiplexer does not connect, so the final input selection becomes independent of the PWM output. The design uses all the intermediate input selections of the multiplexer. **EDN**

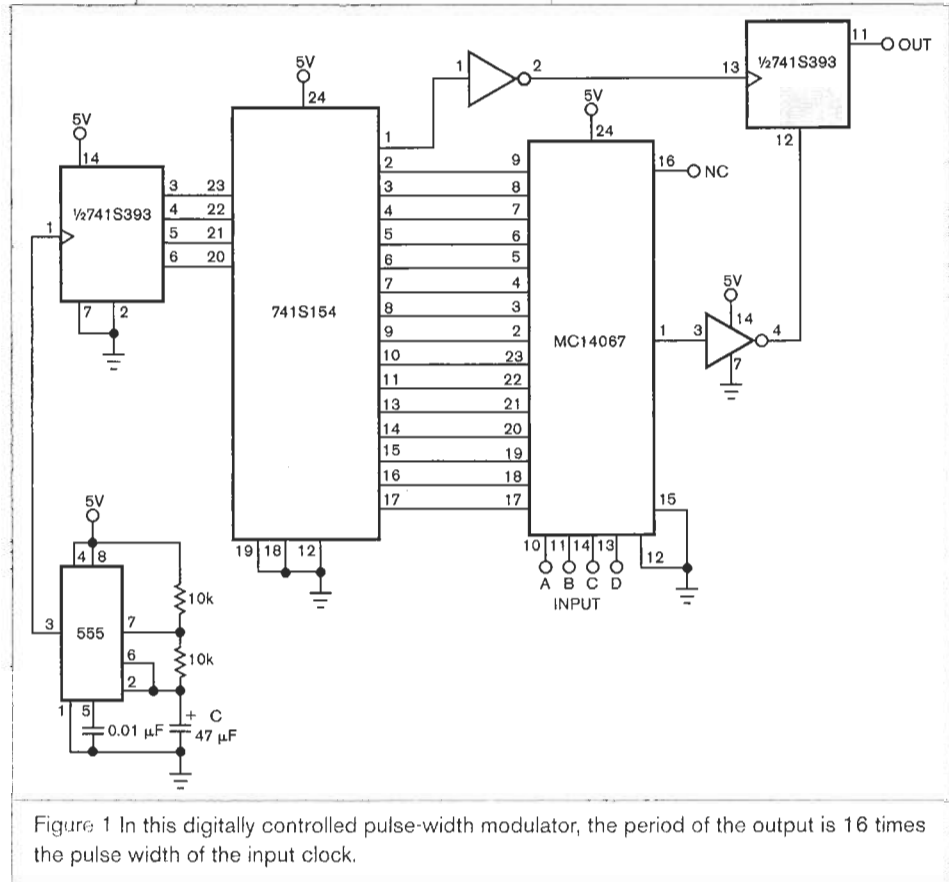


Figure 1 In this digitally controlled pulse-width modulator, the period of the output is 16 times the pulse width of the input clock.