Application Briefs

Sample/Arbitrary Hold

by Bob Craven, Staff Engineer, ADI

SAMPLE-HOLD USING A/D CONVERSION PERMITS ANALOG DATA TO BE STORED DIGITALLY FOR ARBITRARILY-LONG INTERVALS WITHOUT DROOP. DIGITAL READOUT IS AVAILABLE, TOO.

As we have indicated on page 7 of this issue, digital storage can provide the benefits of arbitrarily-long *hold* duration with no droop. Other advantages include: no sample-hold offset, no feedthrough, no dielectric absorption effects, and no sample-to-hold transients or settling time, since the system is automatically in *hold* after a conversion, unless a *sample* command is applied. In addition, both analog and digital outputs are available. Disadvantages are increased cost and complexity, typically longer acquisition time, and possible need for pre-sampling, in the manner of the two-stage Sample-Hold example, Fig. 8, page 8.

Figure 1 shows how this function can be achieved with a D/A Converter, an up-down counter, a comparator, a clock, and a few gates. The initial acquisition time may be quite long,

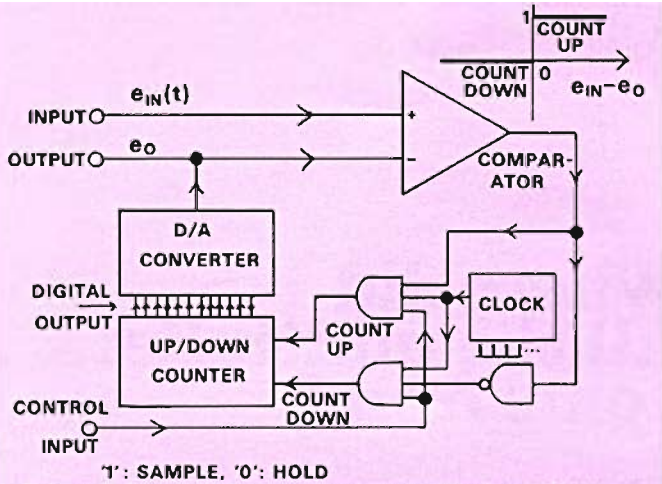


Figure 1. Tracking Sample-Hold Using Up-Down Counter

since the choice of clock frequency depends on the LSB settling time of the D/A converter, and the number of counts required depends on its resolution. For a full-scale step, acquisition time is approximately $(2^n - 1)\tau_s$. Smaller, slower changes, however, will be followed quite rapidly. The system can be converted into a *peak* follower by disabling the *down* count, and into a valley follower by disabling the *up* count. Reset, for peaks, is to 000 . . . 0, and for valleys to 111 . . . 1. The range of input signal levels and polarity determine the choice of D/A-converter output specifications. If a BCD counter and BCD DAC are used, with a numeric display, one has an "all-time-peak"-reading DVM.

Figure 2 shows the generic approach, using an A/D converter and a D/A converter. Where averaging is desired, the A/D converter may be an integrating type. The overall acquisition time is approximately equal to the sum of the A/D converter's conversion time and the DAC's settling time. If the D/A output of a successive-approximations type is available, suitably scaled and buffered, a separate D/A converter is unnecessary, and acquisition time is equal to conversion time.

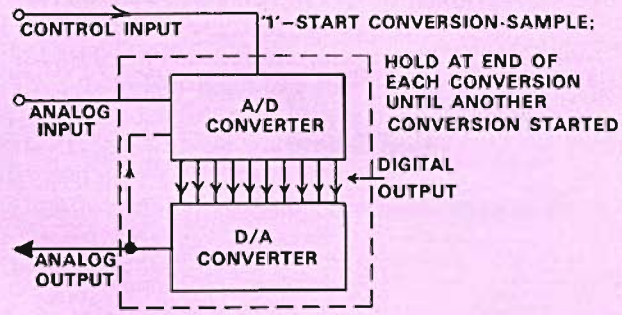


Figure 2. Sample-Hold Using A/D and D/A Converters

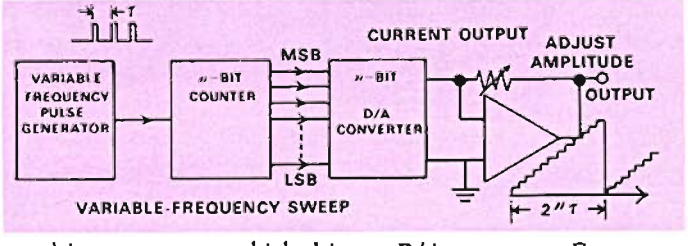
Digital Sweep Generation

by Bob Craven

CLOCK, COUNTER, AND DAC PROVIDE PRECISE SWEEP WITH INDEPENDENTLY-CONTROLLABLE AMPLITUDE & PERIOD, FAST RETRACE.

For a long time, the classical way to generate a sweep has been to make an integrator that is reset either automatically or periodically. With automatic reset, the amplitude is determined by the reset value, the frequency by the input level. With programmable reset, the amplitude is determined by the input level, the frequency by the reset rate. In either case, the essential elements are an op amp, a good capacitor, precision voltage source and resistors, a clamp switch. If frequency is to be adjustable, a choice of capacitors is needed for the several ranges, and a variable precision resistor (possibly ganged) for continuous adjustment. Amplitude and frequency are, in general, interdependent.

With low cost DAC's and digital logic now available, there is a Better Way: Use an adjustable-frequency clock pulse generator



to drive a counter, which drives a D/A converter. Frequency then depends only on clock rate, and amplitude can be scaled from the output of the converter. Since the counter automatically recycles, the sawtooth is automatically reset after each 2^nth count, within 1 counting period.

Resolution is determined by the number of bits, linearity by that of the converter, and clock stability. For slow sweeps, filtering may permit use of a lower-resolution system. "De-glitched" converter output is desirable.*

* For information on the "de-glitched" DAC-10D Converter for display applications, use reply card. Circle D14