

# All-digital phase shifter handles 5-to-1 bandwidth

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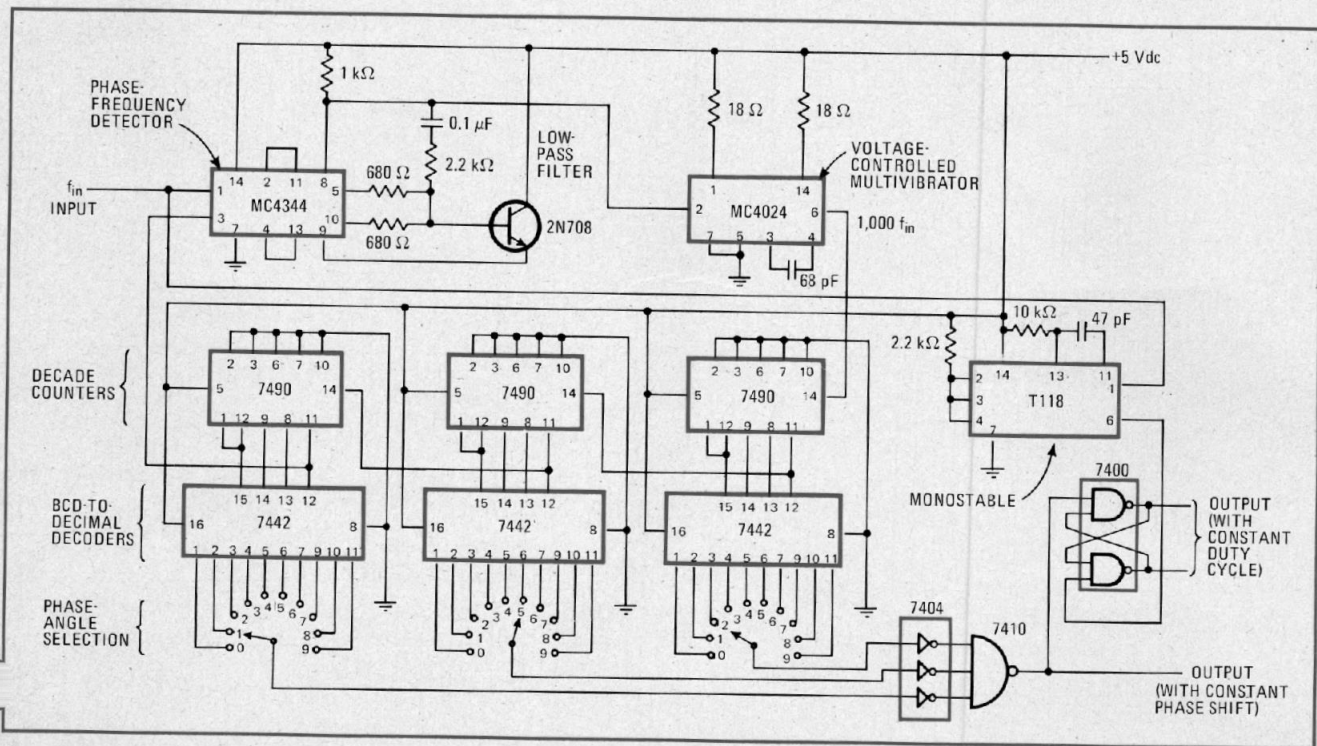
A digitally programable phase-shift network can be made to maintain the phase shift at its output constant, even though the frequency at its input varies by as much as a factor of five. The circuit consists mainly of digital ICs, including its input-detector stage.

**Locking phase digitally.** Circuit produces the phase shift (between  $0^\circ$  and  $360^\circ$ ) selected by the three switches. This digitally programed phase angle does not change, although the input-signal frequency may vary from 2 to 10 kilohertz. The circuit's operating frequency can be changed by adjusting the low-pass filter and the timing of the voltage-controlled multivibrator. There is also a constant-duty-cycle output.

The desired phase shift is switch-selectable through a three-stage counter/decoder network. Any phase shift between  $0^\circ$  and  $360^\circ$  can be chosen. Here, the angle selected is divided into 1,000 bits, but a finer resolution can be obtained by increasing the number of decade counters.

For the component values indicated, the circuit's phase angle stays locked for input frequencies from 2 to 10 kilohertz. This operating frequency range can be shifted by changing the values of the low-pass filter components and the value of the timing capacitor for the voltage-controlled multivibrator.

The circuit also produces an output whose duty cycle remains constant. □





# Digital phase shifter covers 0° to 360° range

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Offsetting the phase of a signal by digital means over the range of 0° to 89° in any quadrant, this low-power circuit is particularly useful in data-recovery systems that employ synchronous detectors. Unlike most RC phase shifters, the value set is independent of the input frequency.

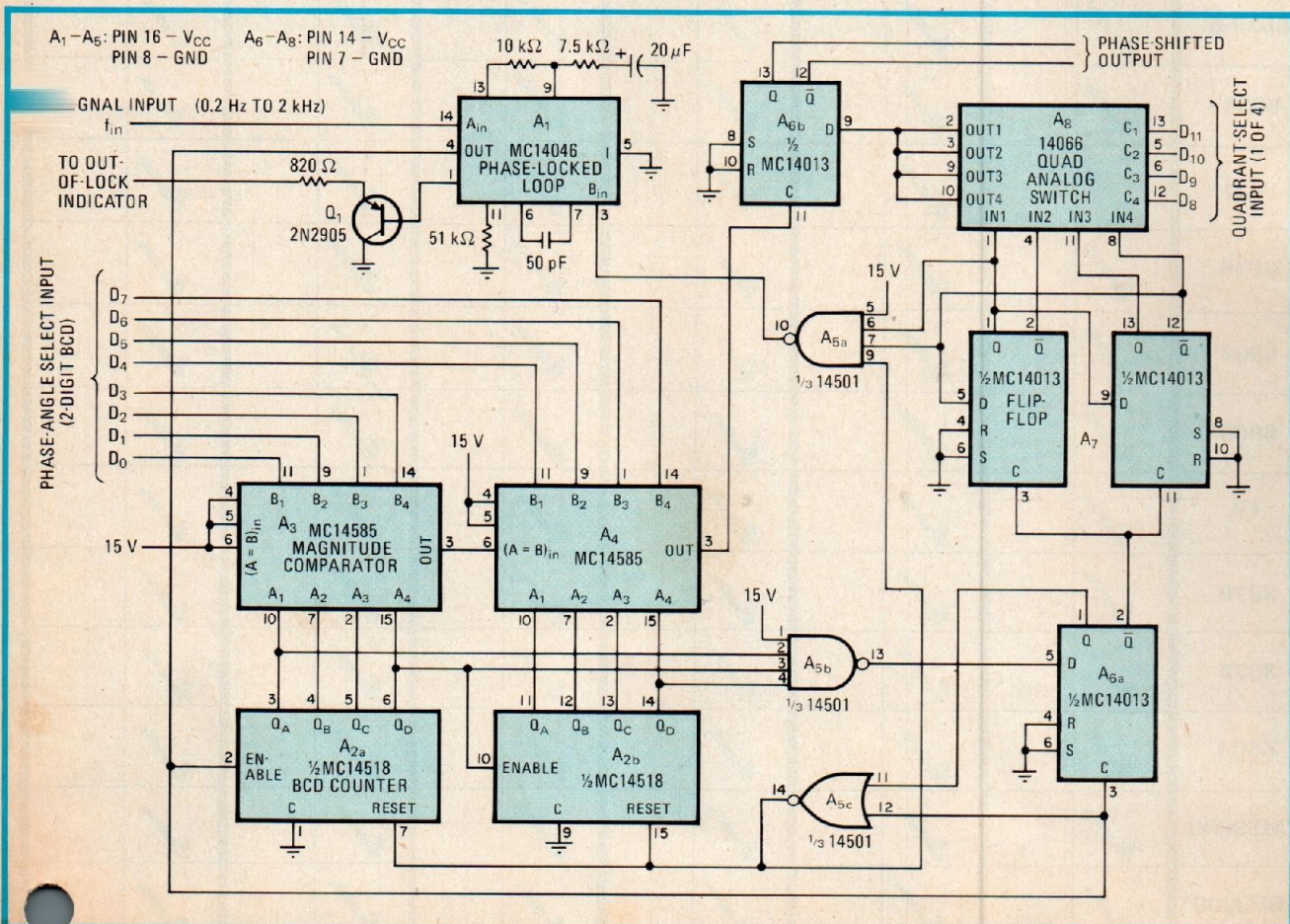
The input reference signal is first introduced to the 14046 phase-locked loop. Its output, which is set to generate a frequency 360 times that of  $f_{in}$ , is then applied to the 14518 binary-coded decimal counter, where it is divided by 10. A second, cascaded counter,  $A_{2a}$ , divides  $A_{2a}$ 's output by 9, the 89th count of a 90-step cycle being detected by  $A_{5b}$ .  $A_2$  is then reset to zero on the 90th count by  $A_{6a}$  and  $A_{5c}$ .

The signal at the output of  $A_{6a}$  is thus at a frequency equal to  $4f_{in}$ . Flip-flop  $A_7$  performs a divide-by-four operation on this signal, at the same time generating four quadrature outputs. Meanwhile,  $A_{5a}$ , which gener-

ates one pulse per cycle of  $f_{in}$ , locks the PLL in phase with the zero count of  $A_2$ . Note that the operation of this divider chain is unaffected by the setting of the digital input lines.

The desired phase is selected by applying the appropriate digital signals  $D_0$ - $D_7$  in binary-coded decimal form. Thus, the output from  $A_3$  and  $A_4$  moves high when  $A_2$  counts to that number and clocks flip-flop  $A_{6b}$ . This action occurs four times per each cycle of  $f_{in}$ . The appropriate quadrant, available at  $A_7$ , is selected by digital inputs  $D_8$ - $D_{11}$ , the active quadrant corresponding to which one of the lines is high. Flip-flop  $A_{6b}$  thus produces a symmetrical square wave at  $f_{in}$  having a phase shift equal to the number of degrees specified plus 0°, 90°, 180°, or 270°. There is an additional phase shift of 0.5° at all settings because of the way the PLL is operated to achieve lock. The error can be eliminated by adding an inverter between the output of  $A_{5a}$  and the B input of  $A_1$ .

With the component values shown and a 15-volt supply, the circuit will operate over the range of 0.2 hertz to 2 kilohertz. Thumbwheel switches with 1-megohm pull-down resistors are used to set the phase-angle input lines. A four-position switch can be used to select the quadrant. With slight modification, the circuit will find application as a digitally controlled ignition timing system for internal-combustion engines. □



**Discrete degrees.** Circuit sets 0° to 360° phase shift of reference signal by digital means. Digital inputs  $D_0$ - $D_7$  determine displacement over 0° to 89° range,  $D_8$ - $D_{11}$  set quadrant. Output is thus 0° to 89° signal shifted by an additional 0°, 90°, 180°, or 270°.