

A code lock circuit should be able to do more than just release
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 an electromechanical door latch. It must also be able to reliably prevent entry by any potential intruder who doesn't know the code - which is exactly what this circuit does. The lock releases the latch when the right pair of buttons is pressed at the same time. If any other button is pressed (here represented by button S3 in the circuit diagram), the user must wait 90 seconds before making another attempt. This makes any effort to discover the right code by trying all possible combinations a very time-consuming enterprise. For instance, you could use a 12 -button keypad with all buttons except the two buttons for the desired code connected in parallel (in other words, connected as shown for 53 ). The fact that the right buttons must be pressed at the same time instead of in one after the other can also be regarded as a severe obstacle to unauthorised entry, since most code locks operate with sequential code entry.

The circuit is based on a type 4028B CMOS decoder IC, which is designed to convert a 4-bit binary code into a decimal value. However, this function is not used in this case. The only thing that matters here is that a ' 1 ' is present at the $0_{0}$ output (pin 3) when a ' 0 ' level is present on all four inputs (A-D). When this happens, power MOSFET TR1 conducts and the electromechanical latch is energised to open the door.

The C input is tied to ground (' 0 ' level), and in the quiescent state the $D$ input is held in the ' 0 ' state by resistor R3. In order to open the door, the user must put inputs $A$ and $B$ in the ' 0 ' state as well by pressing buttons S1 and S2 simultaneously.
If an incorrect button (S3) is pressed, input $D$ is put in the ' 1 ' state, which prevents opening of the latch (a single ' 1 ' is all that is necessary for this). After this happens, capacitor C1 discharges slowly via R3 and prevents the circuit from responding to any further key presses for the next 90 seconds.
If you wish, you can increase the degree of protection against potential code breakers even further by changing the value of C1. For instance, if the value of C1 is raised to $1000 \mu \mathrm{~F}$ a potential intruder would

be well advised to bring along a tent and sleeping bag ;). Although using a higher capacitance value may increase security, it also has drawbacks - especially if the legitimate user accidentally presses the wrong button.

As already mentioned, you can use a 12-button keypad for code entry. Select two buttons of your choice for the code and wire them as shown for S 1 and S 2 in the schematic diagram. Now the latch will not open unless these two buttons are pressed at the same time. Connect the rest of the buttons in parallel and wire them as shown for 53 in the diagram.

Note that many keypads have one contact of each of the buttons connected in to a common terminal. This sort of connection does not present a problem for the 'wrong' (S3) buttons, since they must anyhow be connected together. However, if S1 and S2 are also connected to this common terminal, the connection to the rest of the buttons (represented by S3) must be broken, as otherwise the supply voltage will be short-circuited. In most cases, the connection can be broken by simply scraping away the appropriate tracks on the printed circuit board.

The power MOSFET can easily handle a power level up to 10 watts. For levels higher than this (up to 43 W ), it must be mounted (with insulation) on a heat sink.

The choice of mains-powered or battery-powered operation depends on the specific situation. The circuit draws almost no current in the quiescent state, so battery-powered operation is certainly possible. However, the battery must be large enough to supply the high short-term current that flows when the code lock actuates the latch solenoid. Does this mean that mains-powered operation is better in case of frequent use? Perhaps, but you should also consider what happens when there is power failure.

