32 interference rejector

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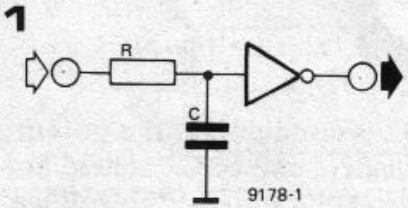
Many TTL circuits have relatively low noise immunity and consequently suffer from spurious pulses upsetting the logic process.
This interference can be greatly reduced by using a circuit that recognises logic pulses by their pre-determined length and level.
Some type of RC network (figure 1) could be used for this purpose. It would, however, affect the TTL levels, narrowing the margin for the R and C values.

1



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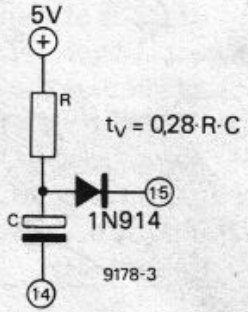
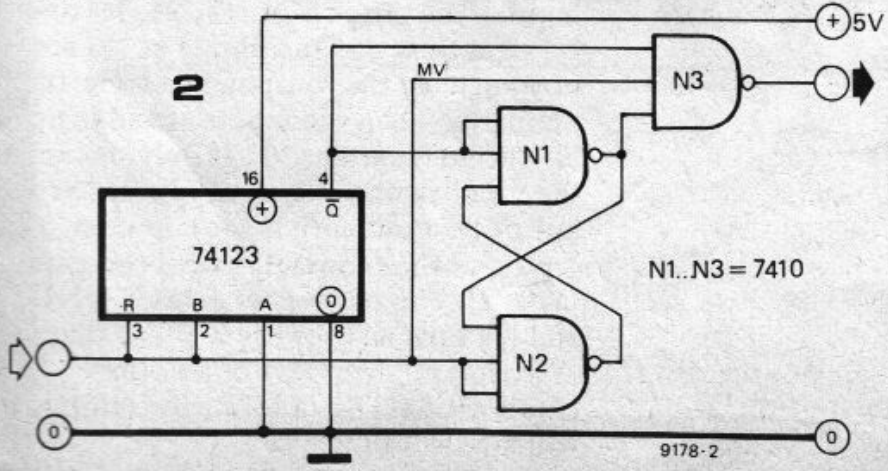


A better performance is given by the circuit of figure 2. It compares the duration of the incoming signal with the length of the 'set' state of a monostable multivibrator. The incoming pulse will have effect only when its length outlasts this state. Shorter pulses will not only be rejected but also, at their trailing edges, 'reset' the MMV to prepare it for the next pulse recognition.

Components shown in figure 3 determine the delay characteristic of the circuit (connected to pins 14 and 15).
Figure 4 shows the logic pulse diagram.
The MMV is 'reset' by a logic '0' whereas a logic '1' of pre-determined length is admitted.

2



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