TTL DESIGN: TRICKS & TIPS

Designing with TTL? Check out the tip sheet in this article before you go one step further. If you aren't aware of all of the notes in this article, learn them before you continue.

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DURING THE LAST FIVE YEARS, THE INtegrated-circuit industry has made tremendous technological advances and has created new and exciting IC families. We now have CMOS, PROM's, ROM's, and a host of other families; but the designer's "workhorse" is still the old reliable TTL (*T*ransistor-*T*ransistor *L*ogic).

Texas Instruments introduced the first TTL package to the electronics industry in 1964. From that early beginning, the TTL logic family has become so economical, versatile, and easy to use that today almost all digital circuits contain at least one of the packages.

Even though TTL chips are relatively easy to use, designers, (particularly the first-time user), often overlook simple but critical design procedures. This article identifies those procedures and offers tips and short-cuts for implementing them.

All TTL inputs and outputs exist either in a HIGH or as a LOW condition. These two conditions are often referred to as states. A HIGH, or positive state is any input or output that is between +2.4 volts and +5.0 volts. A HIGH state must also allow for leakage currents. An input or output is called LOW any time its voltage is between +.8 volt and ground. A LOW input also needs a low-impedance path to ground that can handle 1.6 mA. A good rule of thumb to follow when dealing with inputs is: *Input swings must not exceed the positive supply voltage (+5.0V) or go below ground (0 volts).*

When selecting a power supply, remember that each gate in an IC package draws current. A practical method of determining how much current each gate draws is to divide the total supply current (I^{cc}) by the number of gates contained in that package. The most reliable method, however, is to check the data sheet for each component.

Every gate has a fan-in (input requirements or capabilities) of one and an output (fan-out) that can drive up to ten different loads. If more than ten loads are connected to any one output line, that gate's noise margin is severely impaired. Once the noise margin is impaired, the voltage and current swings become too small to operate all the loads properly. A gate's output voltage (HIGH state) is typically 3.3 volts but it can be boosted to a full +5.0 volts by adding a 2.2K pull-up resistor as shown in Fig. 1. An output transistor and a 1K resistor added to a gate's output (Fig. 2), will provide more current.

If a gate is used as a line driver, remember to use it for that purpose only. Also, never connect the inputs of other gates directly to the output of a gate that is being used as a line driver. If a receiving gate is hooked directly to the output of a line driver, line reflections can cause false inputs. The line-driving gate itself may become excessively

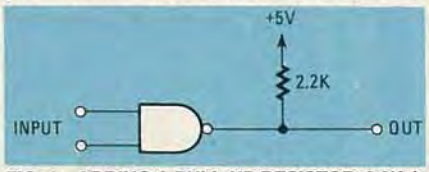


FIG. 1—ADDING A PULL-UP RESISTOR, 2.2K, is al it takes to boost a gate's HIGH output to a full 5.0 volts.

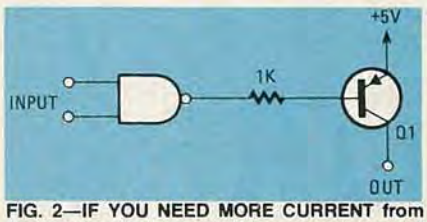


FIG. 2—IF YOU NEED MORE CURRENT from the gate's output add an output transistor and a 1K resistor.

loaded and cause long delay times. Therefore, the line driver's output must first be properly terminated through a resistor network or by some other means. Always decouple line driver and receiver gates by placing a 0.1-μF capacitor across the IC package ground and supply voltage.

Most TTL gates are high-speed devices that can switch at speeds of 20 MHz or more. That rapid switching causes high-frequency current spikes to appear on the power lines. Even though those current spikes are noise, some gates (flip-flops and counters) may see them as trigger pulses. Noise caused by current spikes is only one of the many problems that TTL gates are susceptible to. In a real circuit, noise can come from crosstalk, line reflections, the power supply, or from the environment itself.

Those noises and other associated problems don't have to be "hair-raisers" or "eye-rollers" if the simple and practical design procedures outlined below are followed:

1. USE A REGULATED +5 VOLT SUPPLY! The key word here is *regulated*. TTL circuits are usually designed to operate from a single +5-volt sup-

ply. Manufacturers usually guarantee the proper operation of their IC's as long as the supply voltage is between +4.75 and +5.25-volts (± 5%). Therefore, a regulated +5-volt supply must be one of your most important design considerations.

2. USE HEAVY WIRE FOR ALL POWER CONNECTIONS. For your circuit to operate properly, it must first receive all the power that it requires. Number 20 AWG wire works in most TTL power-line applications. These power lines should be laid out so the transmission path impedance is as low as possible.

3. USE GROUND AND POWER PLANES—IF POSSIBLE. As we said before, TTL circuits are high-speed switching devices. To minimize current spikes caused by that fast switching, keep power and ground planes (PC board areas) as large as possible. A large ground plane acts as a low inductance return for the supply voltage. A ground plane is used if it is not essential to avoid ground loops.

4. USE BYPASS CAPACITORS. The internal design of most regular TTL circuits uses the totem-pole output arrangement shown in Fig. 3. As the TTL gate switches from one state to the other, there is a short time period when both internal output transistors, Q1 and Q2, will be ON. When that occurs, there is a direct low-impedance path between the supply voltage and ground. The result can be 10-to

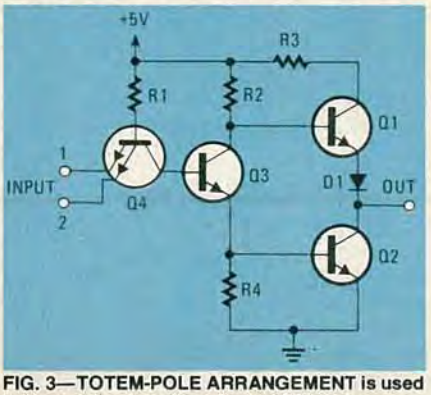
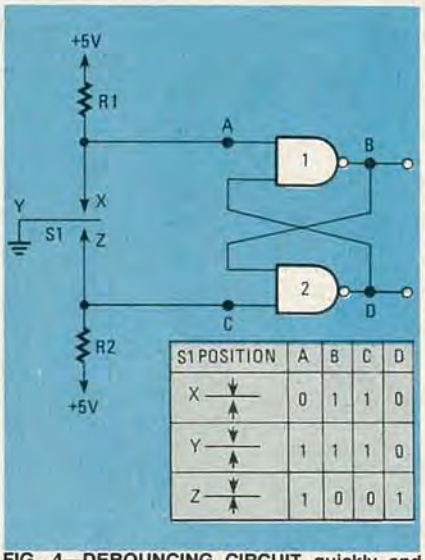


FIG. 3—TOTEM-POLE ARRANGEMENT is used in the internal design of most TTL IC's.



S1 POSITION	A	B	C	D
X	0	1	1	0
Y	1	1	1	0
Z	1	0	0	1

FIG. 4—DEBOUNCING CIRCUIT quickly and easily eliminates the problems of contact bounce.

100-mA current spikes. To solve this problem, place a .01-μF capacitor between the IC's supply input and ground. Keep capacitor leads short and locate it as close as possible to the IC package. If two to five packages are close together, a single capacitor connected across the +5V and ground lines is needed to do the job.

5. AVOID CROSSTALK! If wires that carry similar current or voltage signals are grouped too closely together, you'll get crosstalk. The magnetic or static field created by one wire interacts with the fields created by adjacent wires. To avoid crosstalk don't use wires that are longer than 10 inches. If you must use wires that are 10 to 20 inches long, route them close to a ground plane and **do not bundle them tightly together with similar wires.**

Twisted-pair wire and coaxial cable also effectively reduce crosstalk. Coax cable, however, is usually used only in very noisy environments.

6. DECOUPLE SUPPLY VOLTAGES. A power supply is not an ideal voltage source; therefore, it must be decoupled. An electrolytic capacitor that is rated for at least 10 volts and has a value of 4 to 100 μF will do this job nicely. The capacitor must be placed across ground and the point where the supply voltage first comes into the board.

7. DEBOUNCE GATES THAT ARE CONNECTED TO MECHANICAL SWITCHES. The contacts of a mechanical switch actually strike each other several times before they finally close. Each time those contacts "bounce", a pulse is created. Flip-flops, counters, and other trigger-dependent gates interpret those pulses as signals. Two NAND gates placed between the switch and the receiving gate (Fig. 4) act as a "contact debouncer"

When setting up a debounce circuit, always follow these four rules:

- **A.** Use a SPDT 'break-before-make' switch.
- **B.** Cross-couple the two NAND gates by using the output of gate one as input of gate two and vice-versa.
- **C.** Connect the switch input of gate one and gate two to +5 volts through a 1K resistor.
- **D.** Ground the switch to signal ground.

As a final precaution, never leave an unused input unconnected. An unconnected input will rise to a HIGH and become susceptible to noise.

Therefore, tie all unused inputs either to logically similar inputs or to +5V via a 1K resistor. Unused output pins can be left unconnected.

On most schematics, the connections for +5 volts and ground are not shown. Every TTL IC, however, needs those connections to work properly. If the guidelines set forth in this article and in the IC data sheets are followed, then the procedure of going from design to breadboard will be a snap. **R-E**

REFERENCES:

1. Ott, Henry W., *Noise Reduction Techniques*, John Wiley & Sons, New York, 1976.
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3. Texas Instruments, Inc., *Designing with TTL Integrated Circuits*, McGraw-Hill, New York, 1971.