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## Serial digital multiplier handles two five-bit numbers

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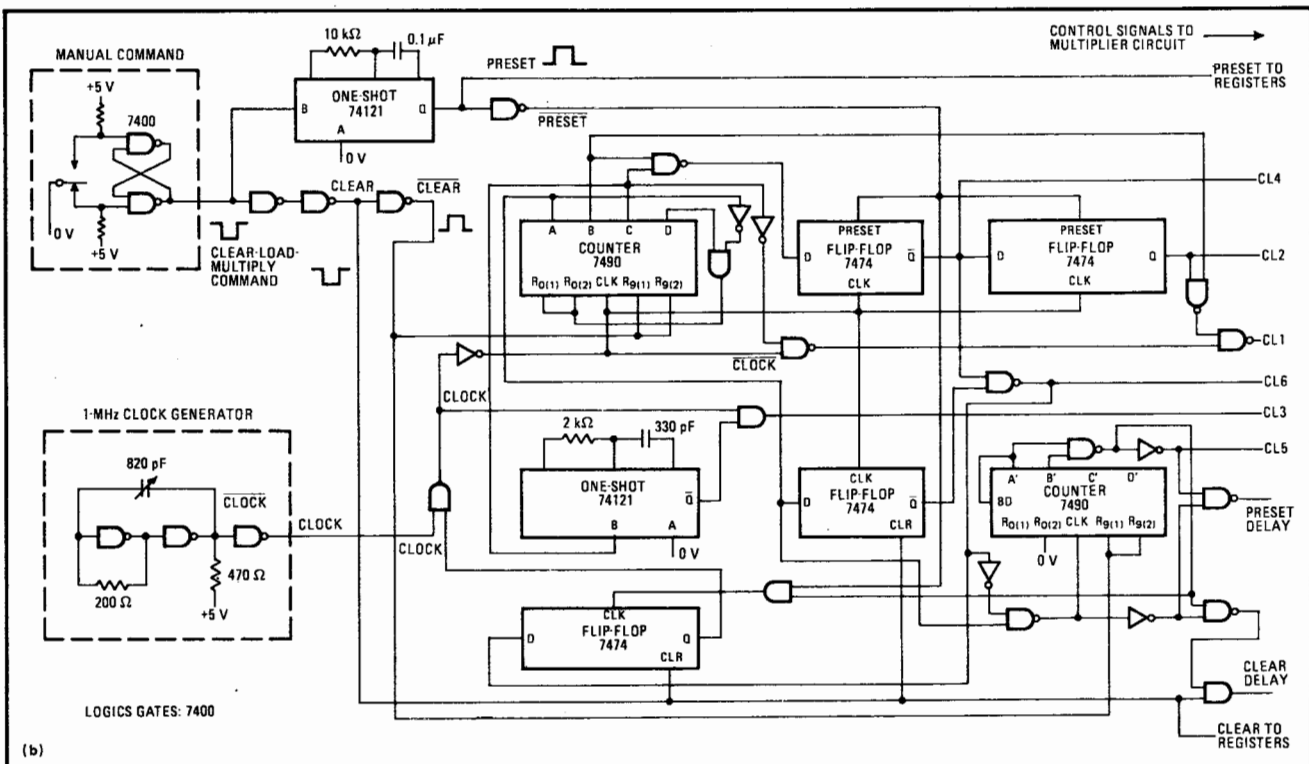
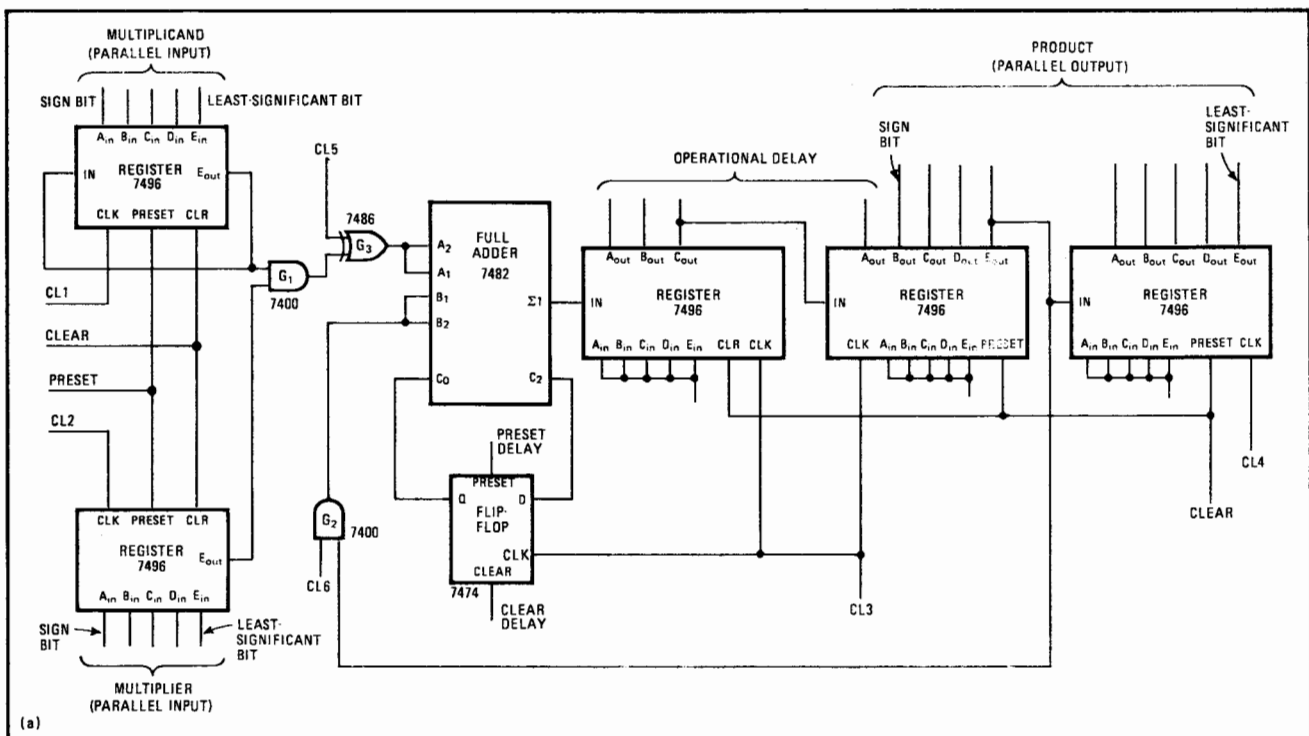
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Because of the fast operating speeds of today's digital circuits, the serial type of digital multiplier can be regarded as a practical alternative to the parallel or serial/parallel type in many applications. The serial ap-

proach can mean a large savings in the number of ICs required to do the job.

The circuit shown is an expandable serial digital multiplier that can accept two 5-bit numbers in two's-complement form. It is useful in such applications as digital filters, signal correlators, and other digital systems that employ two's-complement notation. The multiplier circuitry is shown in (a), while the circuitry used to get the necessary control signals is shown in (b).

The multiplication process is started by a CLEAR-LOAD-MULTIPLY command, which is generated by a manual latch, and stops automatically upon completion. When this start command initiates the control sig-



**Serial multiplication.** The number of ICs needed to build this digital multiplier is minimized because the circuit performs the multiplication serially. The two 5-bit two's-complement input numbers, however, as well as the output number, are in parallel form. The multiplier circuitry is given in (a), and the control-signal circuitry in (b). The system is easily expanded to accommodate larger numbers.

nals, the two numbers to be multiplied—the multiplicand and the multiplier—are loaded into their respective registers.

Each bit of the multiplicand is gated by each bit of the multiplier through gate  $G_1$ . To obtain the final product, the partial sums are added to the partial products. Gate  $G_2$  passes the partial sums, and gate  $G_3$  pro-

vides an inversion when the flip-flop delay is preset. This inversion causes the multiplicand to be subtracted when it is gated by the sign bit of the multiplier. An additional shift register provides an OPERATIONAL DELAY for spreading the sign bit. The final product is available in parallel form from the two output registers.

The basic clock frequency for the multiplier circuit is