SOLID-STATE DEVICES

A new monthly column on semiconductor technology and developments

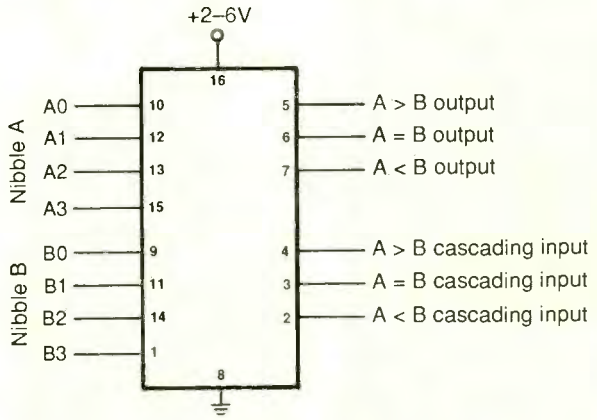
By Harry Helms

Electronics engineering journals and trade magazines today are busily beating the drum for applications-specific ICs (ASICs), the catch-all term for a host of technologies that produce custom and semicustom ICs. Indeed, many predict that by early in the next decade ASICs will capture over half of the worldwide IC market.

I happen to think they're right. ASICs *will* be a big and important part of electronics in the 1990s. But they won't be the whole show by any means. For many purposes, existing IC designs will be adequate and there will be no need to use an ASIC approach. Since ASIC devices in small quantities are an expensive proposition in small quantities, it seems likely that cost-conscious engineering managers will urge their design staffs to try to find solutions using "off the shelf" devices before going the ASIC route.

Therefore, keeping up with developments in standard ICs will continue to be highly important. A recent one I found interesting is the explosive growth in *high-speed CMOS* devices. I'm so impressed by the capabilities of this logic family and the range of devices offered in it that I'm going to go out on a limb and predict that HCMOS (as it's known) will be *the* dominant logic IC family of the next decade, supplanting standard CMOS and TTL (including advanced low-power Schottky ALS versions).

What's so special about HCMOS? Think of it as a marriage between TTL and CMOS that produced children with many of the good qualities of the parents and few of their shortcomings. For years, the tradeoffs in digital logic were clear. TTL was fast and its devices were "tougher" than CMOS but consumed globs of current, was bothered by "noise," and its power supply had to be +5 volts. In contrast, CMOS used little current and could operate over a wide supply voltage range. Unfortunately, CMOS was very slow compared to TTL. A serious problem was CMOS's susceptibility to damage from static discharge (some frustrated users felt you could "zap" a CMOS device simply by looking at it wrong!). Enhanced versions of CMOS and TTL were developed to address some of these problems, but they were more expensive and had some new limitations of their own.



74HC85 4-Bit Magnitude Comparator

Dc supply (V_{CC}): +2 to +6 volts
Dc input voltage: Not to exceed V_{CC}
Maximum quiescent mode power consumption: 8 μA
Minimum high-level input voltage: 1.5 volts for a 2-volt V_{CC}, 3.15 volts for a 4.5-volt V_{CC}
Propagation delay: 230 ns at 2-volt V_{CC}, 46 ns at 4.5-volt V_{CC}
Prime vendors: GE/RCA Solid State, Motorola
Secondary vendors: Hitachi, National Semiconductor, Signetics, Texas Instruments

Fig. 1. Pin diagram and salient specifications and information for the 74HC85 magnitude comparator.

Ahhh, but HCMOS! Now we're getting somewhere! Let's compare HCMOS to ALS, the most advanced version of TTL. HCMOS can operate from a supply voltage from +2 to +6 volts instead of the fixed +5 volts needed by ALS. ALS ICs typically have a quiescent supply current demand of 0.2 mA per gate, which HCMOS easily beats with a 0.0005-mA figure. In speed, there's no real difference between HCMOS and ALS. For example, a D flip-flop typically has a maximum speed of 35 MHz in ALS and 40 MHz in HCMOS, while a typical counter IC can operate at up to 45 MHz in ALS and 40 MHz in HCMOS.

Propagation delay times are virtually identical for ALS and HCMOS. HCMOS noise immunity is greatly superior to ALS. And HCMOS has a big advantage in fan-out capability. For example, a typical ALS IC can drive inputs of 20 other devices, while HCMOS outputs can drive over 50 inputs.

HCMOS also has remarkable compatibility with other logic families. HCMOS outputs can directly drive HCMOS, standard CMOS, or up to ten TTL inputs if all ICs use the same supply voltage. Moreover, HCMOS can accept inputs from HCMOS, standard CMOS and NMOS devices. There are even some HCMOS devices that can directly accept TTL inputs.

You can identify HCMOS devices by the "HC" or "HCT" in their part numbers. "HC" is a "normal" HCMOS device, while "HCT" indicates a device with TTL-compatible inputs and out-

puts. The normal format for part numbers begins with "74" (sometimes, "54"), then the "HC" or "HCT," followed by two to four numbers. One such part is the 74HC00, which identifies a quad 2-input NAND gate device. If that number looks familiar, it should; 7400 is the part number of the same device in standard TTL. Virtually all TTL devices have HCMOS equivalents identified by "HC" and "HCT." These are identical in their pin numbers and functioning. In addition, a number of standard CMOS devices are available in HCMOS versions. This means you can incorporate analog switches, multiplexers/demultiplexers, timers, and even phase-locked loops (the 74HC4046A) into all-HCMOS designs. If you're already familiar with TTL and CMOS, you won't have to learn a new variety of part numbers, devices and functions.

HCMOS isn't perfect, however. It still consumes more power and is more susceptible to noise than standard CMOS. It can't operate over as wide a voltage range as standard CMOS, and "HCT" devices must be operated from a constant +5 volts like TTL (HCT devices also consume more power than HC types). Furthermore, HCMOS is currently more expensive than most other logic families. And HCMOS still is vulnerable to damage from static discharge, requiring the same handling and use precautions that ordinary CMOS does. But these shortcomings are more than offset by HCMOS's many strengths. On balance, it's clearly the best existing logic family for most purposes.

4-Bit Magnitude Comparator

One useful new HCMOS device is the 74HC85 magnitude comparator. Figure 1 shows a pin diagram for this device, which takes two 4-bit (or "nibble") inputs and compares them. The two nibbles are labeled A and B, and three outputs (at pins 5, 6 and 7) indicate three possible relationships between them: A > B, A = B and A < B.

The output corresponding to the relationship between the two nibbles has a high logic level, while the other two outputs are low. There are three cascading inputs (pins 2, 3 and 4) that are used when two or more devices are cascaded to compare "words" larger than four bits. If you're using just one 74HC85, set the A = B cascading input (pin 3) to high and the other two inputs (pins 2 and 4) to circuit ground.

Figure 2 shows how to cascade the 74HC85 to compare two bytes. The first device is used to compare the least-significant nibbles of the two bytes and the second 74HC85 compares the most-significant nibbles. Outputs of the first device feed the cascading inputs of the second, while the cascading inputs of the first device are held to the same logic levels used with the single device. Additional devices can be cascaded in the same manner shown in Fig. 2 to compare words of 16, 32 or more bits. Though it would be easy to use an ASIC device to compare two bytes, this is one example where using standard components can be just as effective and much less expensive!

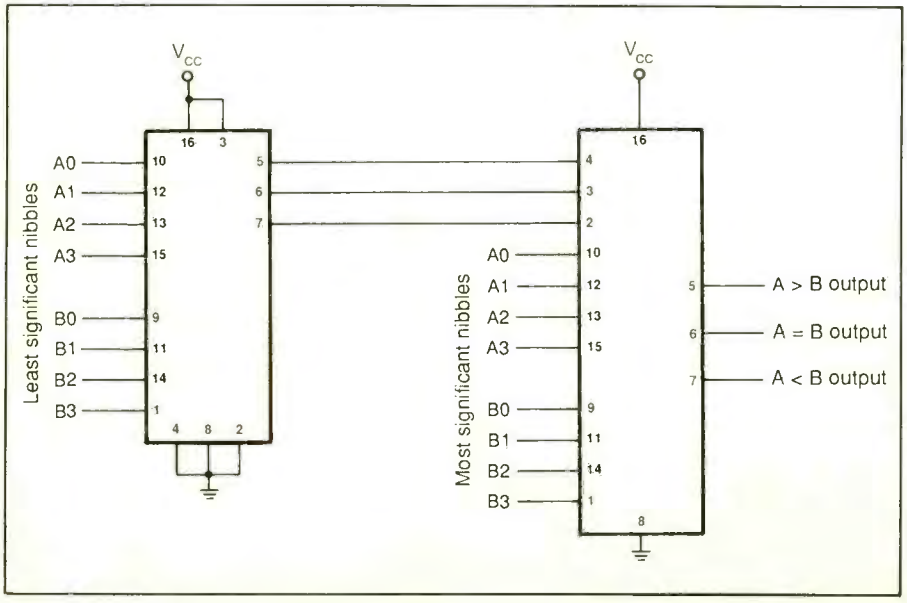


Fig. 2. Details of how to cascade 74HC85s to compare two bytes. Additional 74HC85s can be cascaded in the same manner to compare words of 16, 32 or more bits.

An 8-Bit Equality Comparator

There are often cases when all we need to know is whether or not two bytes are equal. Figure 3 shows the pin diagram for the 74HC688 8-bit equality comparator device. The inputs consist of two bytes, labeled A and B, and a single A = B output at pin 19. This output is low whenever the two bytes are equal; otherwise, it is high. There is also a cascade input at pin 1, which should be kept at a low logic level when only one device is used. (If it is at a high level, pin 19 will be high regardless of the inputs.)

The cascade input is used if more than one 74HC688 is used to compare data "words" that are longer than one byte. This is done by connecting the A = B output of the first device to the cascade input of the second. The pattern is repeated for all other devices in the cascade chain. The cascade input of the first device must be connected to ground. The first device accepts the least-significant byte of each word, the last device in the chain accepts the most-significant bytes.

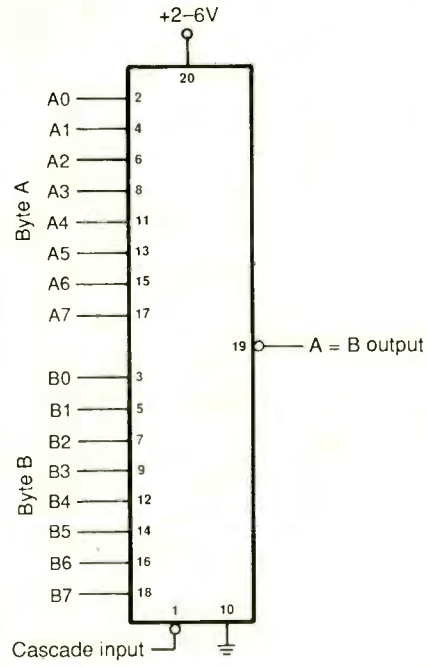
A 9-Bit Odd/Even Parity Checker & Generator

Parity checking it a technique to detect errors when data is transmitted serially from one point to another. Each data

word has one bit known as the *parity bit*, and *odd* or *even parity* can be used. If odd parity is used, the number of 1 (high logic level) bits in the data word will always be an odd number. In even parity, the number of 1 bits will always be even.

The parity bit is usually the first bit in each data word; in the data word 101100011, the first "1" is the parity bit; 0 is used for even parity, while 1 is used for odd parity. Some parity-checking systems "borrow" a bit from a data word byte, leaving only seven bits for data, while other methods add an extra bit to a byte to form 9-bit words.

Figure 4 shows a pin diagram for an HCMOS device to detect the parity of a 9-bit data word input. The 74HC280 has two outputs, the even parity (pin 5) and an odd parity (pin 6). Input bit A (pin 8) is the parity bit. Depending on the parity of the input, one output will be high while the other will be low. If the number of 1 bits in the input is even (0, 2, 4, 6, 8), pin 5 will be high and pin 6 will be low. If the number of 1 bits is odd (1, 3, 5, 7, 9), then pin 5 will be low and pin 6 will be high. This allows you to not only determine the parity of an input signal, but also to "generate" a parity signal for use when comparing inputs that are larger than nine bits. To cascade 74HC280 devices, connect the odd-parity output of the first device to the A bit input of the next device in the chain. Leave the even-parity output open. Additional devices can be cascaded in this manner to handle 33- or 65-bit inputs.



74HC280 9-Bit Odd/Even Parity Checker & Generator

Dc supply (V_{CC}): +2 to +6 volts
Dc input voltage: Not to exceed V_{CC}
Maximum quiescent mode power consumption: 8 μA
Minimum high-level input voltage: 1.5 volts for a 2-volt V_{CC}, 3.15 volts for a 4.5-volt V_{CC}
Propagation delay: 205 ns at 2-volt V_{CC}, 41 ns at 4.5-volt V_{CC}
Prime vendors: GE/RCA Solid State, Motorola, Signetics
Secondary vendors: Hitachi, Mitsubishi, National Semiconductor

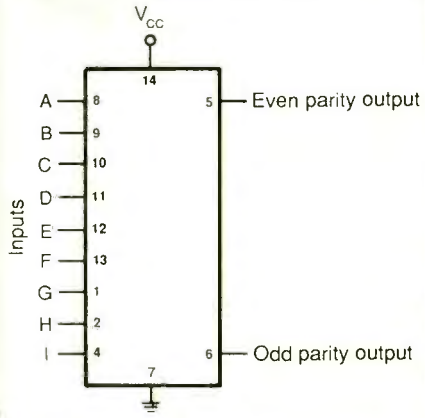
Fig. 3. Pin diagram and salient specifications and information for the 74HC688 8-bit equality generator.

Good Reading

Manufacturer literature is one of the best ways to keep up with semiconductor applications and electronics technology. You can obtain literature from their distributors and sales representatives, or you can obtain it directly from the manufacturer if you request it on business or professional letterhead.

Integrated devices haven't totally conquered the world. For many high-power applications, it's tough to beat a MOSFET. A valuable collection of MOSFET circuits is *TMOS Power FET Design Ideas*, available from Motorola Semiconductor Products. This book includes schematics and circuit information for voltage regulators, motor speed controls, lamp switches and dimmers, audio amplifiers, modulators, power supplies, and radio transmitters. This manual runs 70 pages and proves that discrete devices are alive and well. (Motorola, P.O. Box 20912, Phoenix, AZ 85036.)

I started this month's column by mentioning how ASICs seem destined to dominate electronics. A good guide to what an engineer must keep in mind when designing an ASIC is *Practical Considerations for the Design of Semicustom ASICs* (ICAN-8740), available from GE/RCA Solid State. Some of the advice is surprising, such as suggestions to avoid using on-chip clock signal oscillators and tri-state (high, low and high-



74HC688 8-Bit Equality Comparator
Dc supply (V_{CC}): +2 to +6 volts
Dc input voltage: Not to exceed V_{CC}
Maximum quiescent mode power consumption: 8 μA
Minimum high-level input voltage: 1.5 volts for a 2-volt V_{CC}, 3.15 volts for a 4.5-volt V_{CC}
Propagation delay: 210 ns at 2-volt V_{CC}, 42 ns at 4.5-volt V_{CC}
Prime vendors: GE/RCA Solid State, Motorola, Signetics, Toshiba
Secondary vendor: Hitachi

Fig. 4. Pin diagram and specifications and information for the 74HC280 9-bit odd/even parity checker and generator.

impedance) outputs. (GE/RCA Solid State, P.O. Box 3200, Somerville, NJ 08876.)

A Personal Note...

This is my first of what I hope will be a long line of columns. I'm particularly glad to once again write for Art Salsberg, for whom I wrote over a decade ago at *Popular Electronics*, and to appear in the same magazine as Forrest Mims, who has been a good friend since my days in Radio Shacks's technical publications group. My charter is to bring you the most recent developments in semiconductor technology and news on the latest devices available. I'd appreciate your feedback and comments about what you'd like to see in this column! ME