Configurable logic gates' Schmitt inputs make versatile monostables

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You can assemble a pulse-generation circuit from a simple Schmitt-input AND gate plus a resistor-capacitor timing network. However, if you need a logic function that's not a standard catalog item, you need a Schmitt-input gate or inverter and an additional logic gate. Drawing from an earlier Design Idea (**Reference 1**) and a recent design requirement for adding pulse-generation functions to a crowded pc board, I searched Fairchild Semiconductor's Web site (www.fairchildsemi.com) for small-footprint Schmitt-input logic gates and found only "old faithfuls"—familiar Schmitt-input AND gates and Schmitt buffers.

Disappointed, I investigated other logic offerings from Fairchild and stumbled across a section of the Web site that describes "configurable logic gates." Lo and behold, I suddenly realized I was looking at the solution to my problem. The NC7SZ57 and NC7SZ58 (**Reference 2**) comprise tiny, six-pin surface-mount packages that you can configure as inverters or as AND, OR, or XOR gates, all of which allow the inversion of one input. These devices feature inverted outputs, overvoltage-input tolerance, and high current drive.

Every input has hysteresis, making these devices ideal for timed pulse generation. A design that combines digital logic with analog interfaces often requires timed pulses and delays, along with pulse shorteners and stretchers. For applications in which exact pulse times are not critical, the added feature of Schmitt inputs allows the delay of one input using an RC (resistance-capacitance) timing network. When the slowly changing RC circuit's output crosses the analog-level upper- or lower-trip-point thresholds, the Schmitt feature converts the slowly rising and falling voltages to fast digital edges.

Texas Instruments (www.ti.com)

offers functional equivalents—the SN74LVC1G57 and SN74LVC1G58 (**Reference 3**). Both companies' devices offer upper- and lower-trip-point-voltage thresholds averaging 37 and 63%, respectively, of V_{CC}, or approximately one RC time constant on the rising or the falling edges. According to the published data sheets from the manufacturers' Web sites, Texas Instruments' versions impose somewhat tighter tolerances on the analog threshold levels and thus deliver tighter timing tolerances than do the Fairchild parts.

For digital-analysis purposes, any voltage below the upper trip point for a rising edge effectively represents a logic zero, and any voltage above the lower trip point for a falling edge represents a logic one. These conditions are true only after the input crosses a respective trip point, such as a rising edge that approaches but never crosses the upper trip point. This voltage remains a logic zero, even if the voltage then drops back to ground potential on its falling edge.

Figure 1a shows some typical circuit implementations. Note that these circuits lack some of the niceties of genuine monostables. For example, a circuit doesn't retrigger until after its RC network has stabilized or about five time constants have elapsed. The RC time constant must be five times shorter than the time between triggering events. Devices from the SN74LVC1G57 family produce the waveforms in **Figure 1b**, and circuits using the SN74LVC1G58-family devices produce the inverse of these waveforms. The circuits' operation is straightforward. The RC circuits delay one input, so that the inputs momentarily rest at opposite states. When one RC time constant elapses, the delayed voltage crosses the Schmitt upper- or lower-trip-point thresholds, and the delayed input catches up to the straight-through input.

Of unusual interest and unlike the usual variety of monostable that triggers only from a voltage transition in one direction, the XOR implementation functions as a monostable triggered by both the rising and the falling edges, enabling it to function as a frequency doubler for generating strobe pulses on rising and falling clock edges. You can make any inverting-gate configuration into an oscillator by feeding back its inverted output to an RC-delayed Schmitt input and enabling the gate's remaining input. However, once the XOR oscillator's remaining gate switches off the oscillation, the gate's output state hangs at either a one or a zero to produce a truly random state derived from the oscillation's nonsynchronous relationship to the timing of the disabling input. EDN

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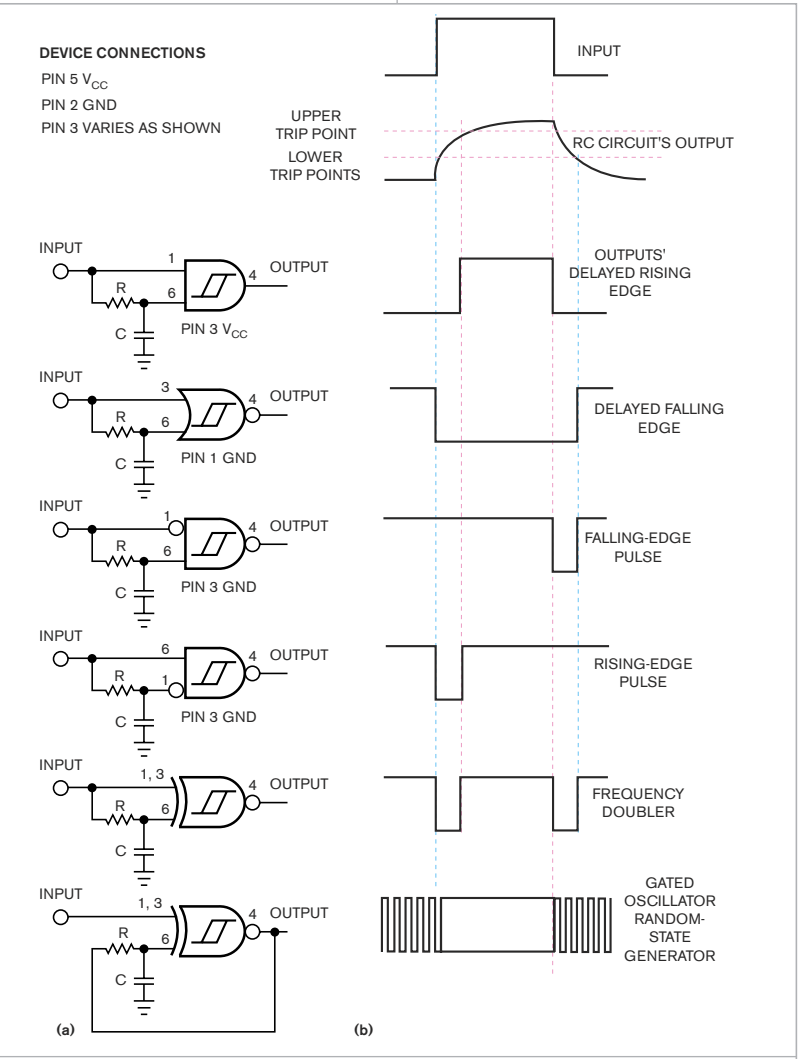

Figure 1 One gate plus an RC network (a) can deliver a range of useful timed outputs (b).