

Change-of-state detector

A conventional change-of-state detector uses the OR'ed outputs of two monostables triggering from opposite polarity edges. This circuit uses only one exclusive-OR gate i.e., and performs frequency doubling or change-of-state detection. The first three gates are connected as buffers and the final gate exclusive-ORs the output of the buffers and the input. An output pulse of width equal to the total propagation delay of the buffers is obtained, in practice about 100ns, from the CD4070B. This pulse may be extended if necessary by the addition of a <math>< 5\text{nF}</math> capacitor from point B to ground.

If the line shown tied to V_{DD} is connected to V_{SS} instead, the output polarity is inverted.

S. Roberts,
Sheffield.

Audio overload monitor

This circuit uses two of the four comparators in an LM339 package to provide detection of excessive positive or negative signal peaks. Pulse-stretching is used to ensure that a clear indication of short-duration peaks is given. Bidirectional peak measurement is important as positive and negative peaks may vary by up to 8dB.

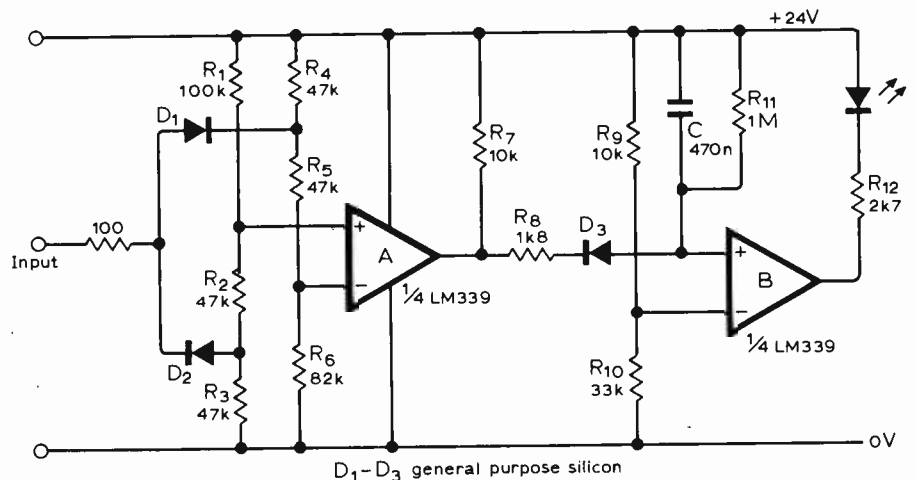
Comparator A detects peaks of either polarity, and the two potential dividers hold the inverting input 400mV below the non-inverting input. If the audio input exceeds the trip point on a positive peak, D_1 conducts which pulls up the inverting input and causes the comparator to change state. Likewise, a suitably large negative peak will make D_2 conduct and pull down the non-inverting input, again causing the comparator output to go low.

When output A goes low, storage capacitor C charges rapidly through D_3 and R_8 . When the peak is past, C remains charged and keeps the output of comparator B low so the l.e.d. remains on. The output goes high again after C has discharged through R_{11} , and the l.e.d. is extinguished.

With the values shown, the circuit trips at a peak level equivalent to a 5V r.m.s. sine wave. This is 3dB below the maximum voltage swing to be expected from an amplifying stage operating from a 24V rail. Note that the circuit should not be driven from a high impedance point because the diodes may cause distortion.

A stereo version may be conveniently made using a single LM339 package.

D. Self,
London E.17.



SR flip-flop

Using a c.m.o.s. dual D-type flip-flop and one exclusive-OR gate an SR flip-flop may be made which is triggered by a positive edge on either input, irrespective of the level of the other input.

A positive edge on the set input will force the two flip-flops into opposite states and hence one input to the exclusive-OR will be a 1 and the Q output will be a 1. A positive edge on the reset input will force both flip-flops to the same state, the two exclusive-OR inputs will be equal and the Q output will be a 0.

K. Dillon,
Epsom,
Surrey.

