The ins and outs of logic gates

Digital inverters, buffers and logic gates can come in either IC form or made up from discrete circuitry. Which type should be used in a particular application? Ray Marston answers this and many other 'logic' questions in this article.

Ray Marston

PULSE INVERTERS, buffers and gates are the most basic elements used in digital electronics. When designing complex digital circuits, it is often necessary to work out the most economic or cost-effective method of implementing these elements. Sometimes it's best to use discrete components (diodes-resistors-transistors) to make an element, and at others it's best to use a dedicated CMOS chip. How do you make the choice? I'll explain that in the next few pages.

The best known logic gates are the OR, NOR, AND, NAND, EX-OR and EX-NOR (EXclusive) types. Less well known is 'majority' logic which, as the name implies, gives an output only when the majority of an odd number of inputs are high. Majority logic is useful in 'voting' and psuedo-intelligent applications, such as decision-making in robotic and security systems.

Buffers and inverters

The most basic type of digital circuit is the simple pulse inverter. Figure 1a shows the standard circuit symbol of the inverter, and Figure 1b shows the 'truth', or operational table; Figure 1c shows a discrete resistor-transistor version of the inverter.

In digital circuits, input and output signals are either at zero, or logic 0 values, or at the full supply-rail voltage of logic 1 value. Thus, in Figure 1c, when the input is low (at logic 0) the transistor is cut off and the output is pulled high (to logic 1) via R2, and when the input is high the transistor is driven to saturation and the output is pulled to zero volts. The importance of the Figure 1b truth table is that it illustrates this information in short-hand form.

The standard inverter is the most versatile of all logic elements. It can be used to convert an OR gate to a NOR type, or vice versa, or to convert an AND gate to a NAND type or vice versa. A pair of inverters can be used to make a bistable, monost-

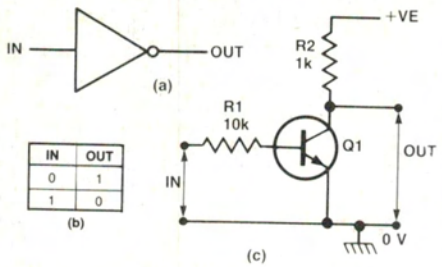


Figure 1. (a) Standard symbol and (b) truth table of a digital inverter with (c) a resistor-transistor version of the unit.

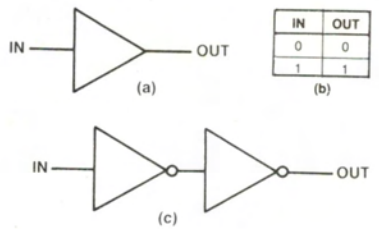
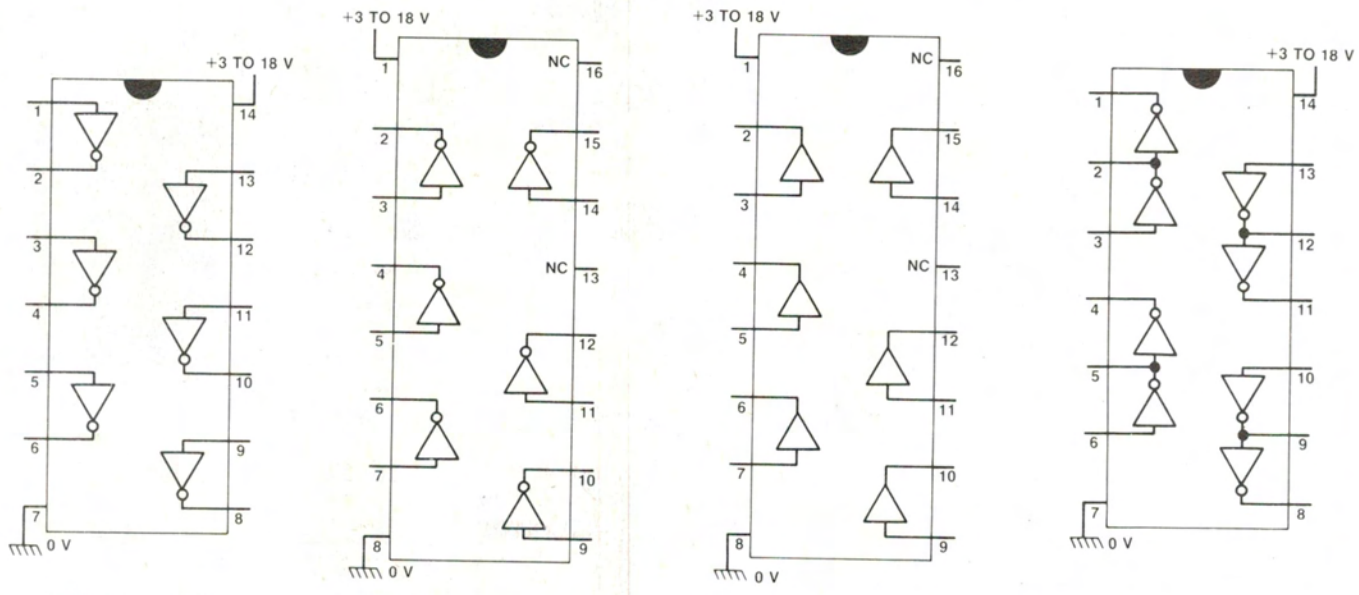


Figure 2. (a) Symbol and (b) truth table of a non-inverting buffer stage which can be made by (c) cascading two inverter stages.



4069UB hex inverter.

4049UB hex inverting buffer.

4050B hex non-inverting buffer.

4041UB quad invert/non-invert buffer.

Figure 3. Five popular CMOS inverter and buffer ICs.

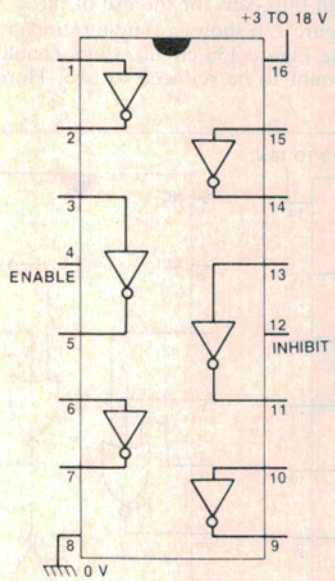
able or astable multivibrator, etc. Usually, a practical inverter has an input impedance that is high relative to its output impedance, and can be used as an impedance 'buffer'.

Not all buffers are of the inverting type. Figure 2a shows the standard circuit symbol of a non-inverting buffer stage which can be made by cascading two inverting elements as shown in Figure 2c.

Inverters and buffers are available in dedicated CMOS IC form, and Figure 3 gives details of five popular examples. The 4041, 4049 and 4069 types use the unbuffered (UB) low-gain form of CMOS construction, and the 4050 and 4502 use the high-gain buffered form of construction.

The 4069UB is a simple general-purpose hex inverter, housed in a 14-pin package, with 'standard' output drive capability. The 4049UB hex inverting buffer and the 4050B hex non-inverting buffer, on the other hand, have high output drive capability and are specifically intended to drive TTL loads; they can accept input signals far greater than the supply voltage so can be used to give signal-level translation between CMOS and TTL circuits.

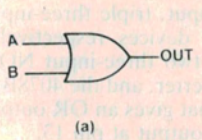
The 4041UB also has high output-drive capability and can be used to drive TTL, but can not accept input signals greater than its supply voltage. The device is a quad invert/non-invert buffer. If, for example, an input is applied at pin 3, an inverted output is available at pin 2 and a non-inverted output at pin 1.



4502B tri-state hex inverting buffer. Normally pins 4 and 12 are grounded. If pin 4 is high the outputs go into the high-impedance tri-state mode. If pin 12 is high all outputs go low (if not in the tri-state mode).

The 4502B is a hex inverting buffer capable of driving TTL loads, and has a tri-state output which can be selected via pin 4; when pin 4 is low the IC gives normal inverting operation, but when pin 4 is high all outputs go into the high-impedance tri-state mode. The IC also has an INHIBIT control terminal (pin 12), which is normally held low but which drives all outputs to ground (in the 'normal' mode) when pin 12 is taken high.

The basic guidance rules for using inverters and buffers in practical circuits are simple. If you need a large number of stages, use as many dedicated ICs as necessary. If you get to the point where you are short of just one or two stages, see if you can make them from spare stages of existing logic ICs (I'll show how later) or, failing that, consider using simple resistor-transistor stages of the type shown in Figure 1c.



A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

(b)

Figure 4. (a) Symbol and (b) truth table of a two-input OR gate.

OR and NOR gates

Figure 4a shows the standard symbol of a two-input OR gate, and Figure 4b shows its truth table. As indicated by its name, the output of the OR gate goes high if any of its inputs (A OR B, etc) go high. The simplest way to make an OR gate is to use a number of diodes and a single load resistor, as shown in the three-input OR gate of Figure 5. The diode OR gate is reasonably fast, very cost effective, and can readily be expanded to accept any number of inputs by adding one more diode to the circuit for each new input.

Figure 6a shows the standard symbol of a two-input NOR gate (which functions like an OR gate with an inverted output) and Figure 6b shows its truth table. Figure 7 shows how a diode OR gate can be converted to a NOR type by feeding its output through a transistor or IC inverter stage.

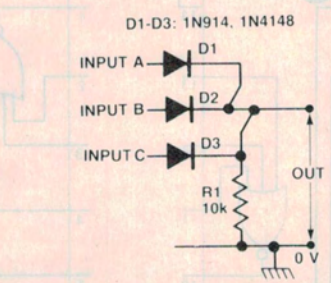
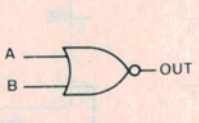


Figure 5. Three-input diode OR gate.



A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

(b)

Figure 6. (a) Symbol and (b) truth table of a two-input NOR gate.

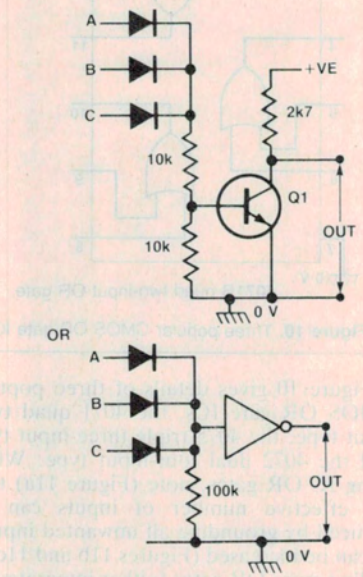


Figure 7. The diode OR gate can be converted to a NOR type by feeding its output through a transistor or IC inverter.

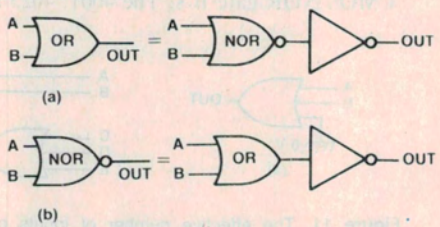


Figure 8. An OR gate can be made from a NOR gate, or vice versa, by taking the output via an inverter.

Figure 8 drives this lesson home by pointing out that an OR gate can be made from a NOR gate plus an inverter, and a NOR gate can be made from an OR gate plus inverter.

Figure 9 shows that a NOR gate can be made to act as a standard inverter, and an OR gate can be made to act as a non-inverting buffer, by either grounding all but one of the inputs or by connecting all inputs in parallel.

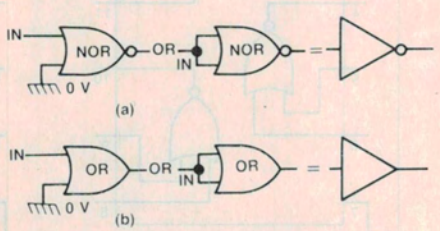


Figure 9. A NOR gate can be converted to an inverter and an OR gate can be converted to a non-inverting buffer. ▶

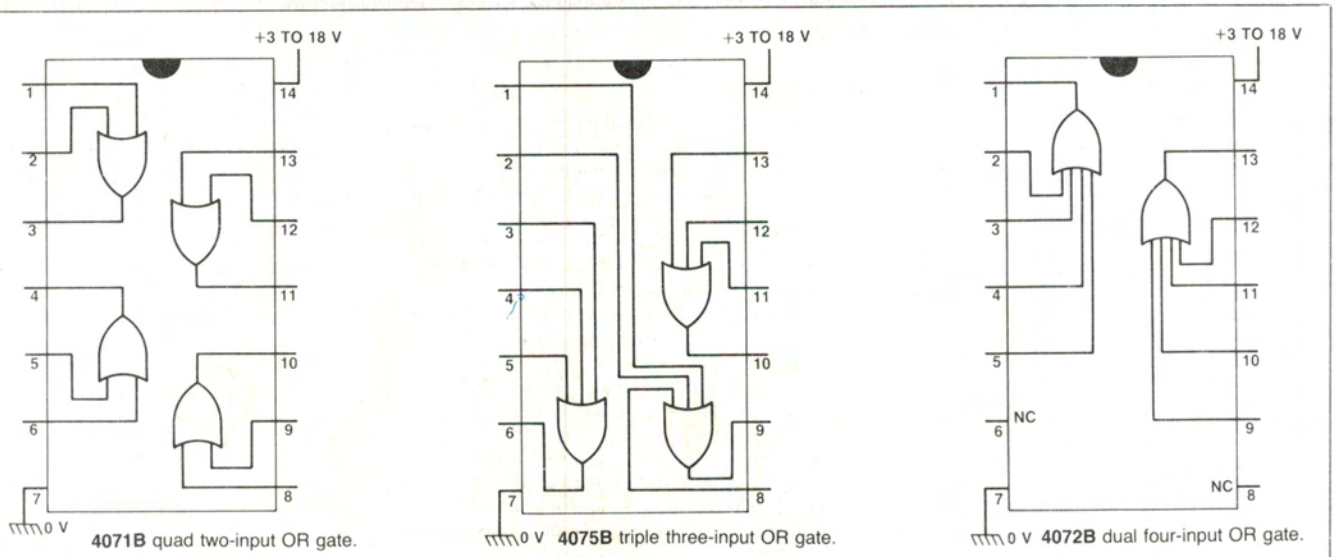


Figure 10. Three popular CMOS OR-gate ICs.

Figure 10 gives details of three popular CMOS OR gate ICs, the 4071 quad two-input type, the 4075 triple three-input type and the 4072 dual four-input type. When using IC OR gates, note (Figure 11a) that the effective number of inputs can be reduced by grounding all unwanted inputs, or can be increased (Figures 11b and 11c by adding more OR gates (either integrated or discrete) to one of the inputs.

Figure 12 gives details of five popular CMOS NOR gate ICs. The 4001, 4025 and 4002 are quad two-input, triple three-input and dual four-input devices respectively. The 4000B contains two three-input NOR gates and a single inverter, and the 4078B is an eight-input gate that gives an OR output at pin 1 and a NOR output at pin 13.

Note that, since a NOR gate is equal to an OR gate with an inverted output, the effective number of inputs of a NOR gate can be increased or reduced by using the techniques that have already been shown in Figure 11.

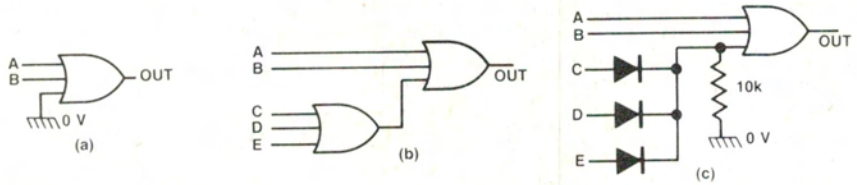


Figure 11. The effective number of inputs of a CMOS OR gate can be reduced (a) by grounding all unwanted inputs, or increased (b or c) by adding more OR gates to one of the OR inputs.

Figure 13 illustrates a simple example of logic design using OR and NOR gates and inverters, the aim being to design a simple low-power tone generator (using a PB-2720 piezoelectric transducer) that can be activated via any one of four inputs. Look first at Figure 13a. At first sight, the design seems to call for the use of a four-input OR gate, with its output feeding to a gated tone generator. A suitable tone generator can be made by connecting a two-input NOR gate and an inverter in the standard astable configuration shown, but this astable is gated on by low input signals, so (in Figure 13a) the required circuit action can be obtained by interposing an inverting stage between the output of the four-input OR gate and the input of the astable. The Figure 13a design thus calls for the use of three ICs.

Figure 13b shows a simple rationalisation of the Figure 13a circuit which enables the IC count to be reduced to two. Here, the

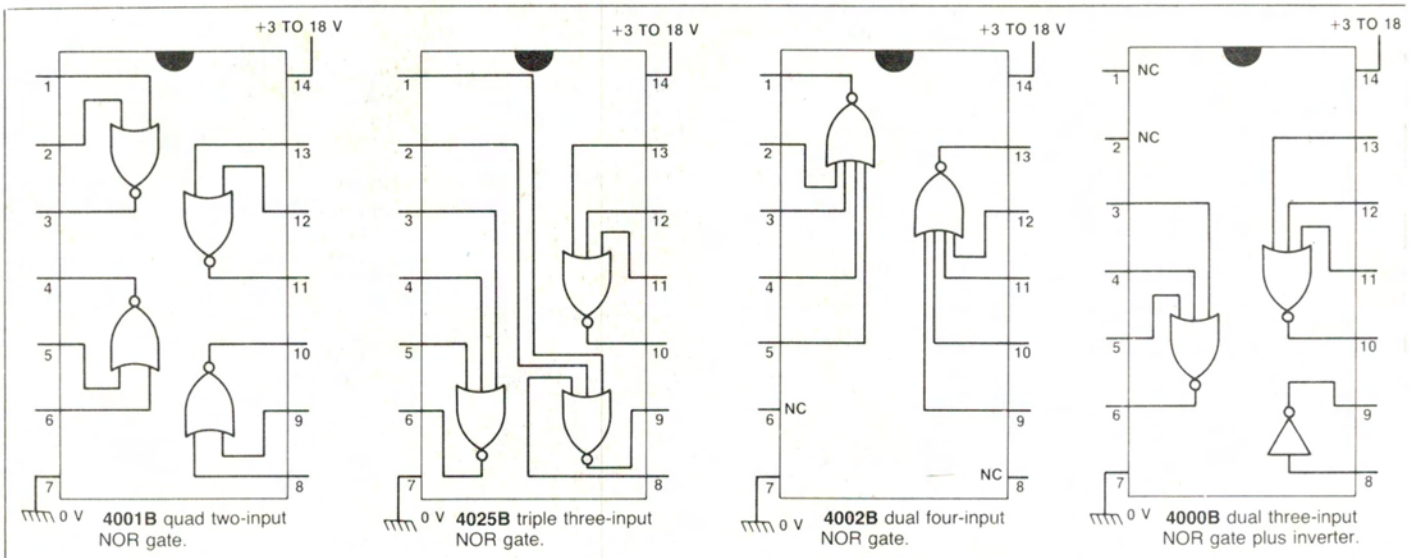


Figure 12. Popular CMOS NOR-gate ICs.

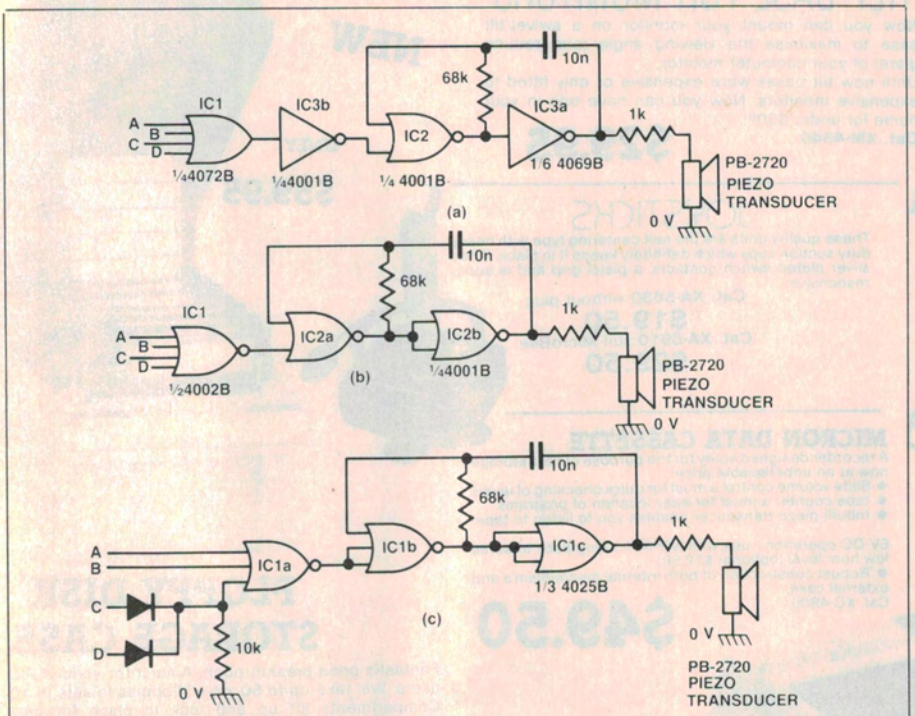
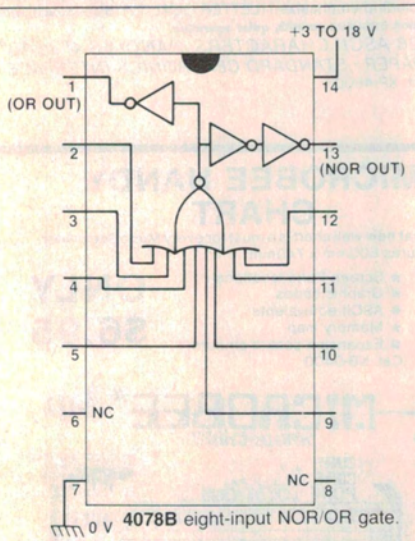


Figure 13. Low-power tone generator activated by any of four 'high' inputs. The 'over-designed' version shown in (a) uses three CMOS ICs but the rationalised design shown in (b) uses only two CMOS chips. In (c) the design is further rationalised so that it uses only a single IC.

four-input OR gate plus inverter of Figure 13a is replaced by a four-input NOR gate, and the inverter section of the astable is made from a two-input NOR gate with its inputs shorted together.

Finally, Figure 13c shows how the design can be further rationalised so that it uses only a single IC (a triple three-input NOR gate) and a couple of diodes. Here, the astable is made by converting a three-input NOR gate to a two-input type by shorting two of its inputs together, and by shorting all three inputs of another gate together to make an inverter. The input gate of the circuit is converted to a four-input type by connecting a two-input diode OR gate to one of its inputs.



4078B eight-input NOR/OR gate.

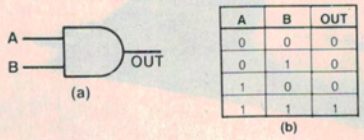


Figure 14. (a) Symbol and (b) truth table of a two-input AND gate.

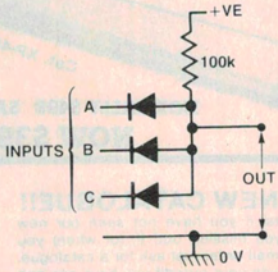


Figure 15. Three-input diode AND gate.

AND and NAND gates

Figure 14 shows the standard symbol and truth table of a two-input AND gate which, as indicated by its name, gives a high output only when all of its inputs (A AND B, etc) go high. The simplest way to make an AND gate is to use a number of diodes and a single load resistor, as shown in the three-input AND gate of Figure 15; more inputs can be obtained by adding one extra diode for each new input.

Figure 16a shows the standard symbol of a two-input NAND gate (which functions like an AND gate with an inverted output) and Figure 16b shows its truth table.

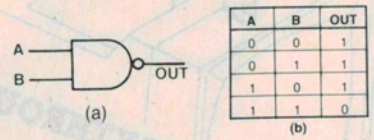


Figure 16. (a) Symbol and (b) truth table of a two-input NAND gate.

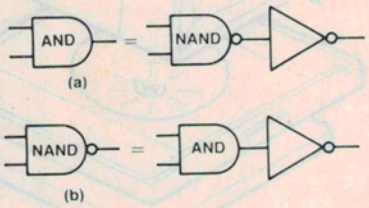


Figure 17. An AND gate can be made from a NAND gate, or vice versa, by taking the output via an inverter.

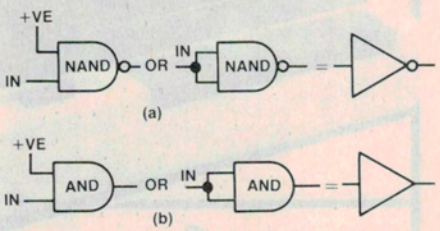


Figure 18. A NAND gate can be made to act as an inverter and an AND gate can be made to act as a non-inverting buffer.

Figure 17 shows how a NAND gate can be made from an AND gate and an inverter, and an AND gate can be made from a NAND gate and an inverter. Figure 18 shows that a NAND gate can be made to act as an inverter and an AND gate can be made to act as a non-inverting buffer either by wiring all but one of the inputs to the positive (logic 1) rail or by wiring all inputs in parallel.

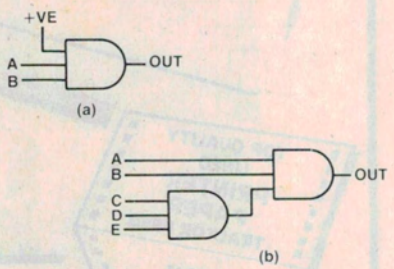


Figure 19. The effective number of inputs of an AND or NAND gate can easily be (a) reduced or (b) increased.

Figure 19 shows that the effective number of inputs of an AND or NAND gate can be (a) reduced by wiring all unwanted inputs to the positive supply rail, or (b) increased by wiring extra AND gates to one of the inputs. ▶

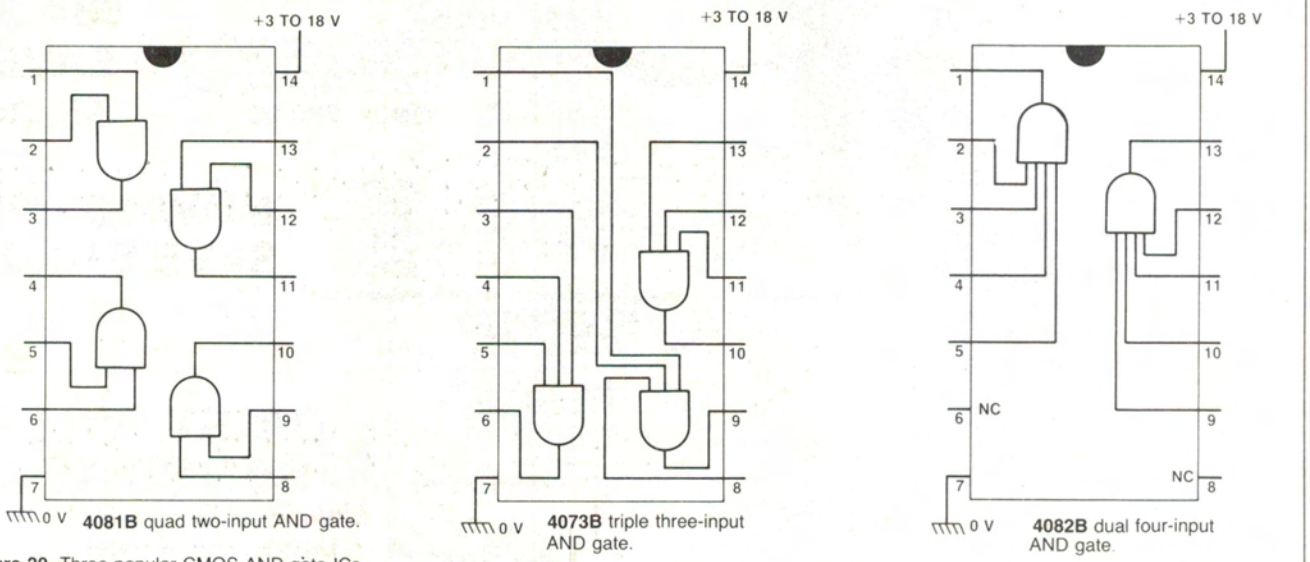


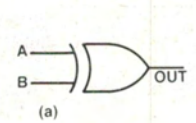
Figure 20. Three popular CMOS AND-gate ICs.

Figure 20 gives details of three popular CMOS AND gates, the 4081B quad two-input type, the 4073B triple three-input type, and the 4082B dual four-input type.

Figure 21 gives details of five popular CMOS NAND gates. The 4011, 4023 and 4012 are quad two-input, triple three-input and dual four-input types respectively. The 4068B is an eight-input device with both AND and NAND outputs. The 40107B is a dual 2-input NAND gate, housed in an 8-pin package, with outputs via open-drain n-channel transistors that can (typically) sink 136 mA.

EX-OR and EX-NOR gates

Figure 22a shows the standard symbol of a two-input EX-OR (EXclusive-OR) gate, and Figure 22b shows its truth table. The output of the EX-OR gate goes high only when the two inputs differ. A useful feature of the EX-OR gate is that it can be used as either an inverting or a non-inverting amplifier by wiring or switching one of its inputs either to the positive (logic 1) supply rail (inverting mode) or to ground (non-inverting mode), as shown in Figure 23.



A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

(b)

Figure 22. (a) Symbol and (b) truth table of a two-input EX-OR gate.

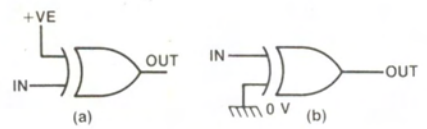


Figure 23. Two-input EX-OR gate connected as (a) inverting and (b) non-inverting amplifier.

Figure 24 shows the symbol and truth table of a two-input EX-NOR gate. This logic element is equivalent to an EX-OR

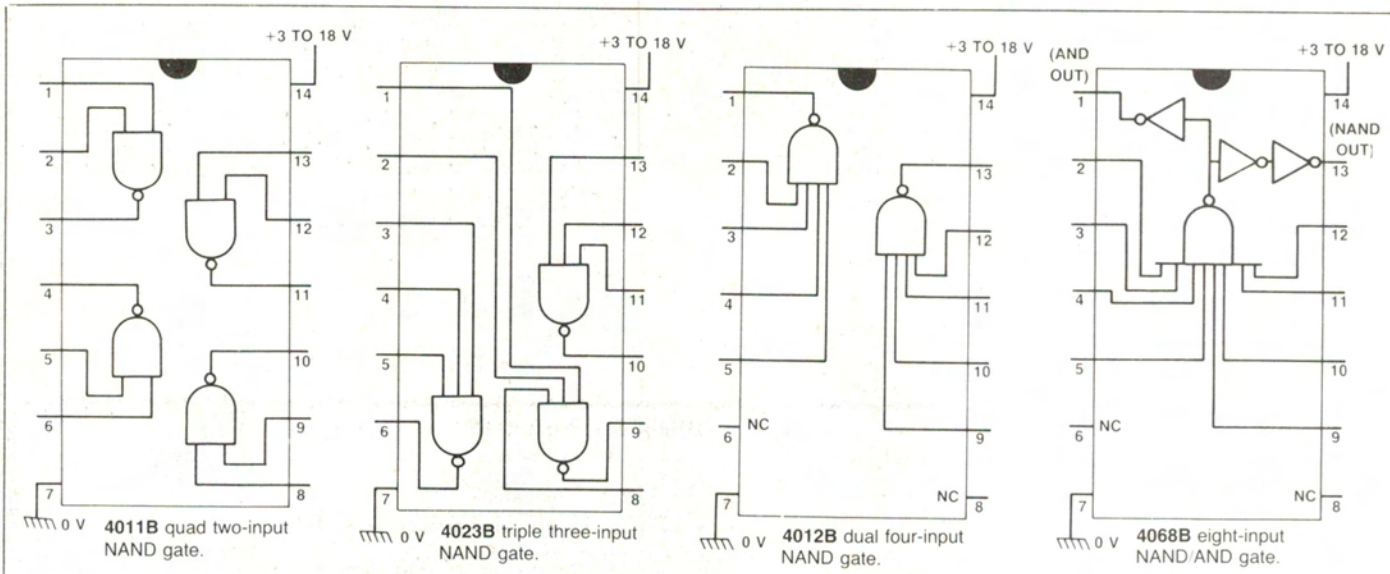


Figure 21. Five popular CMOS NAND-gate ICs.

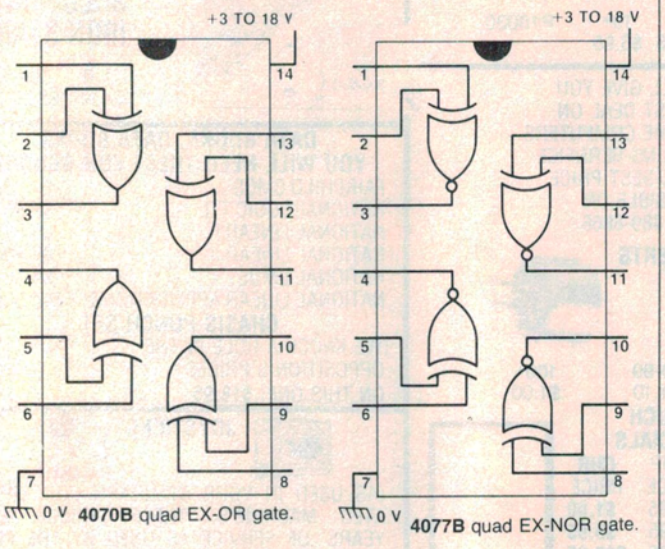


Figure 25. Two popular CMOS 'EX' ICs.

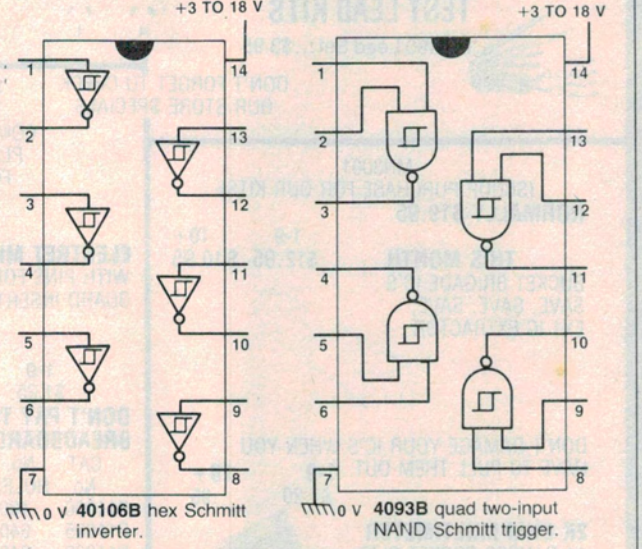
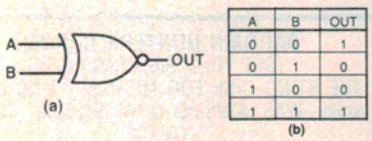


Figure 26. Two popular CMOS Schmitt ICs.

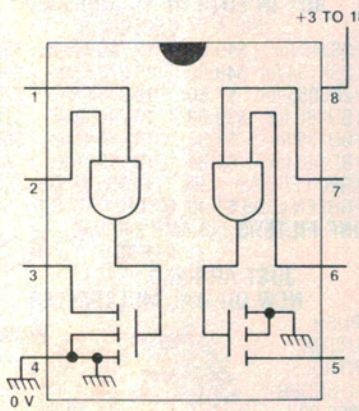
gate with an inverted output. It gives a high output only when both inputs are identical, and is very useful in logic-comparator applications.



A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	1

Figure 24. (a) Symbol and (b) truth table of a two-input EX-NOR gate.

Figure 25 shows details of the two best known CMOS 'EX' devices, the 4070 quad EX-OR gate and the 4077 quad EX-NOR gate.



40107B dual two-input NAND buffer/driver.

Special inverters and gates

CMOS inverters and gates are generally intended to be driven by logic signals that are in either the fully-high (logic 1) or fully-low (logic 0) states. If inputs are allowed to linger between these two states for more than a few microseconds, there is a danger that the inverter/gate will become unstable and act as a high-frequency oscillator, thereby generating false output signals. Consequently, if 'slow' signals are present at one or more of the inputs of a CMOS logic system, these signals must be 'conditioned' (given fast rise and fall times) before being applied to the actual logic circuitry.

The most useful conditioning element is the Schmitt trigger, and Figure 26 gives details of two popular CMOS Schmitt ICs, the 40106B hex Schmitt inverter and the 4093B quad two-input NAND Schmitt trigger.

Most CMOS logic ICs are dedicated devices; e.g: the 4082B is a dual four-input AND gate, and can be used as nothing *but* an AND gate. One very useful exception to this is the 4048B multifunction 'programmable' eight-input gate, which has the functional diagram and outline shown in Figure 27. This IC has two groups of four input pins, plus an EXPANSION input pin, and is provided with four control (K) pins which enable the user to select the mode of logic operation.

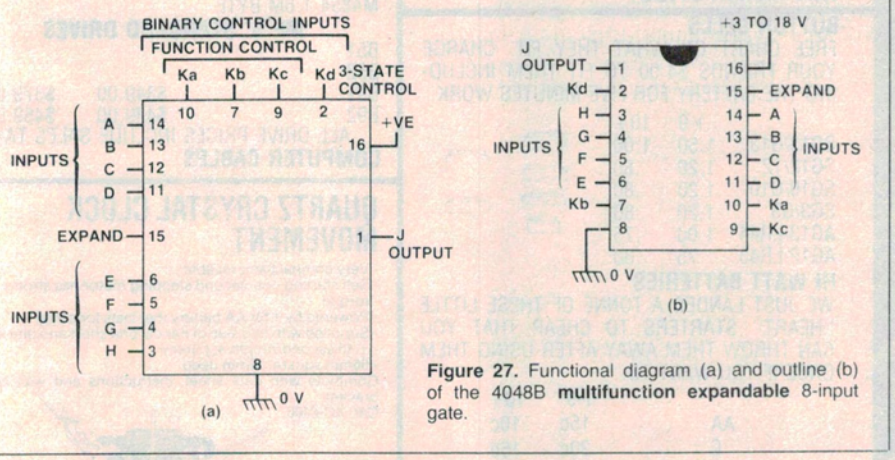
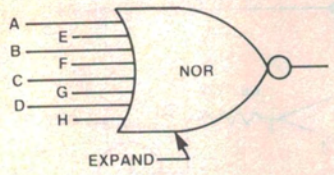


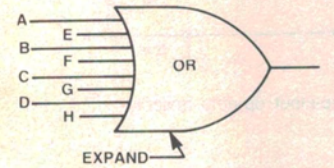
Figure 27. Functional diagram (a) and outline (b) of the 4048B **multifunction expandable** 8-input gate.

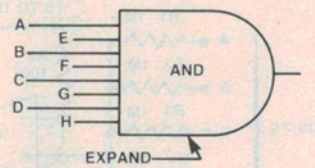
Control input Kd (pin 2) enables the user to select either normal (pin 2 high) or high-impedance tri-state (pin 2 low) output operation. The remaining three binary control inputs — Ka, Kb and Kc — enable one of eight different logic functions to be selected, as shown by the table of Figure 28a, which also shows how to connect unwanted inputs in each mode of operation. ▶

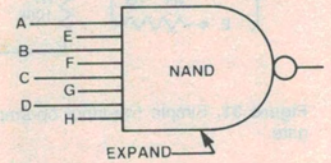


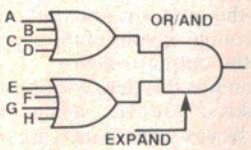
OUTPUT FUNCTION	Ka	Kb	Kc	UNUSED INPUTS
NOR	0	0	0	0
OR	0	0	1	0
OR/AND	0	1	0	0
OR/NAND	0	1	1	0
AND	1	0	0	1
NAND	1	0	1	1
AND/NOR	1	1	0	1
AND/OR	1	1	1	1

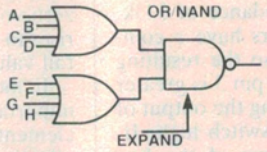
Kd = 1 for normal action
= 0 for high-Z outputs
Expand input = 0

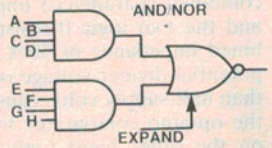












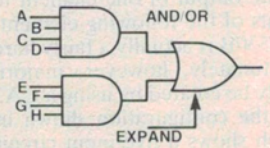


Figure 28. Function table and the eight basic logic configurations of the 4048B **multifunction expandable** eight-input gate.

Thus, to make the 4048B act as a normal six-input OR gate, connect the two unwanted inputs to ground (logic 0), and control pins Ka and Kb to ground and pins Kc and Kd to the positive supply rail. The EXPAND input (pin 15) is normally tied to ground.

Eight different logic functions are available from the 4048B, as shown in Figure 28b. Note that operation in the AND, OR, NAND and NOR modes is quite conventional, but that operation in the remaining four modes (OR/AND, OR/NAND, AND/OR and AND/NOR) is less self-evident.

In the latter cases the inputs are broken into two groups of four, with each group providing the first part of the logic function, but with the pair of groups providing the second part of the logic function. Thus, in the OR/AND mode, the circuit gives a high output only if at least one input is present in the A to D group at the same time as at least one input is present in the E to H group.

The EXPAND input terminal of the 4048B enables ICs to be cascaded so that, for example, two ICs can be made to act as a 16-input gate by feeding the output of one IC into the EXPAND terminal of the other.

Note when using expanded logic that the input logic feeding the EXPAND terminal is not necessarily the same as the overall logic that is required: Thus, an OR EXPAND input is needed for expanded NOR or OR operation, a NAND EXPAND for AND and NAND operation, a NOR EXPAND for OR/AND or OR/NAND operation, and an AND EXPAND for AND/OR or AND/NOR operation.

Majority logic

To conclude, let's take a brief look at a little-known logic system known as *majority logic*, in which the logic unit has an odd number of inputs (3, 5, 7, etc) and gives an output only when the *majority* of inputs (2, 3, 4, etc) are high, irrespective of WHICH inputs are active. This type of logic is useful in some special applications, such as in voting machines and semi-intelligent alarms and robotic devices in which, for example, an alarm bell may sound only if at least two or three detectors indicate a 'fault' condition, or a robot may move only if there is more stimulus to move than there is to stand still.

The best known CMOS majority logic IC is the 4530B dual five-bit unit (Fig 29), each half of which contains a five-input majority logic element with its output feeding to one input of an EX-NOR gate that has its other input (W) externally available, enabling it to be wired as either an inverting or non-inverting stage. Thus, when 'W' is tied to logic 1, the EX-NOR stage gives non-inverting action and the output of the element goes high only when the majority of inputs are high: when 'W' is tied to logic 0, the EX-NOR stage gives an inverting action and the output of the element goes high when the majority of inputs are low.

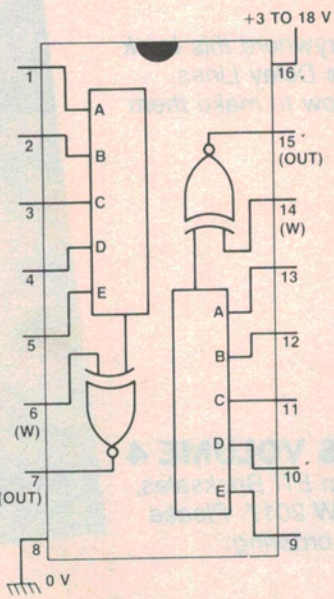


Figure 29. Details of the 4530B dual five-bit majority-logic gate.

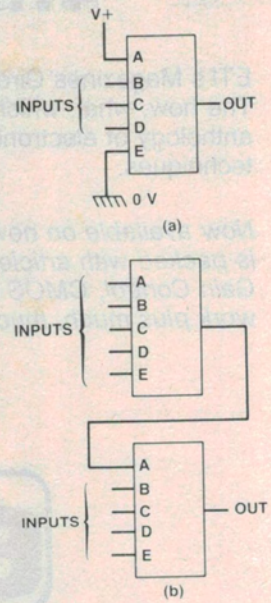


Figure 30. The number of effective inputs of a majority-logic circuit can easily be (a) decreased or (b) increased.

The effective number of inputs of a 4530B can be reduced by wiring half of the unwanted inputs to logic 1 and the other half to logic 0 (Figure 30a). The effective number of inputs can be increased by cascading elements, as shown in Figure 30b. ▶

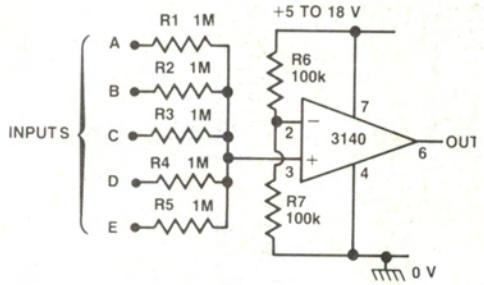


Figure 31. Simple five-input op-amp majority-logic gate.

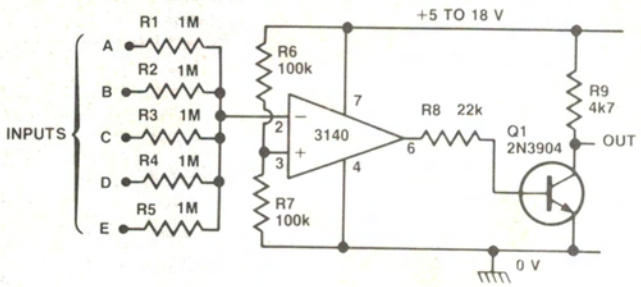


Figure 32. Compound five-input op-amp majority-logic gate.

taking the output of one element to one of the inputs of the following element.

The 4530B is actually a fairly hard to find IC. Fortunately, however, majority logic can easily be created by using a CA3140 op-amp in the configuration shown in Figure 31, which shows a five-input circuit. Here, the op-amp functions as a voltage comparator, with potential divider R6-R7 applying half-supply volts to pin 2 of the op-amp, and the five input resistors (which are each connected to either ground or the supply rail) form a potential divider that applies a fraction of the supply voltage to pin 3.

Suppose that two input resistors are connected to logic 0 and three resistors go to logic 1. The three logic 1 resistors have a combined (paralleled) impedance of 333k, and the two logic 0 resistors have a combined impedance of 500k, so the resulting potential-divider voltage on pin 3 is greater than half-supply volts, causing the output of the op-amp comparator to switch high. If, on the other hand, only two of the five inputs are taken to logic 1, the resulting pin 3 voltage is below half-supply value and the op-amp output is switched low. The circuit thus gives 'majority-logic' action.

When 5% resistors are used the Figure 31 circuit can be given any number of inputs up to a maximum of eleven by simply adding one more 1M resistor for each new input. The output of the circuit switches fully to zero volts when the output is low, but only rises to within a couple of volts of the supply rail value when the output is high.

In most applications this defect is of little importance; it does, however, mean that elements cannot be cascaded to increase the effective total number of inputs. This defect can be overcome by using the alternative 'compound' configuration of Figure 32, in which the output is inverted and level-shifted by Q1 and the inputs to the op-amp are transposed. The output of this circuit switches to within 50 mV of either supply rail, enabling units to be cascaded without limit. ●