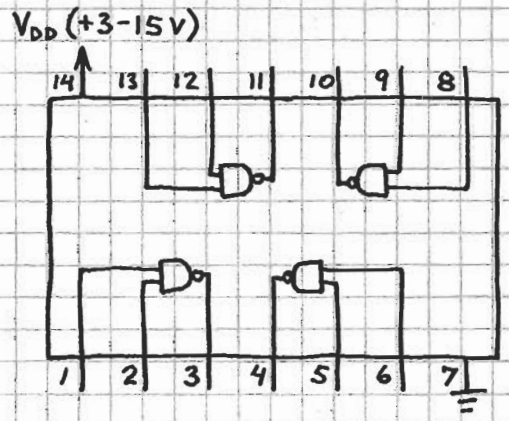
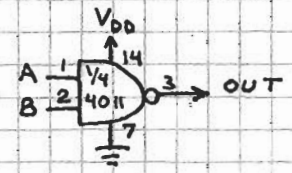
QUAD NAND GATE
4011

THE BASIC CMOS BUILDING BLOCK CHIP. MORE APPLICATIONS THAN TTL 7400/74LS00 QUAD NAND GATE.



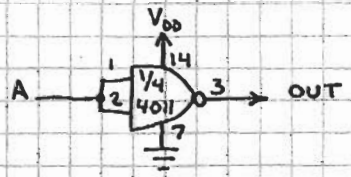
IMPORTANT: CONNECT ALL UNUSED INPUTS TO PIN 7 OR 14!

CONTROL GATE



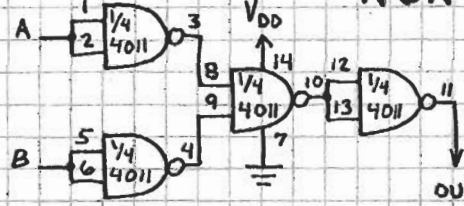
A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

INVERTER



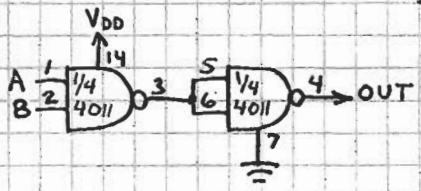
A	OUT
L	H
H	L

NOR GATE



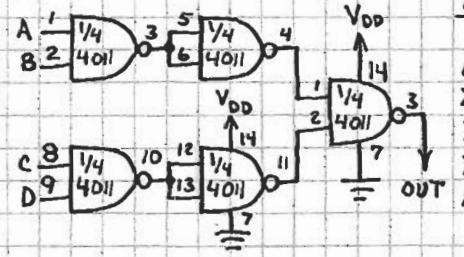
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

AND GATE



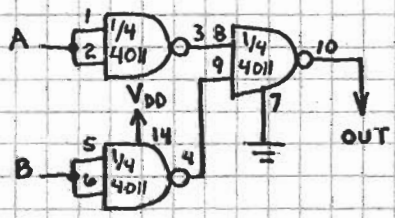
A	B	OUT
L	L	L
L	H	L
H	L	L
H	H	H

4-INPUT NAND GATE



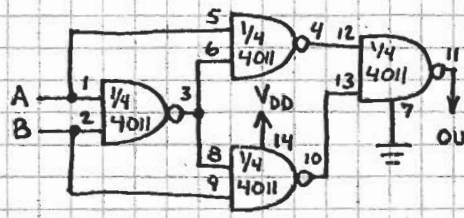
A	B	C	D	OUT
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

OR GATE



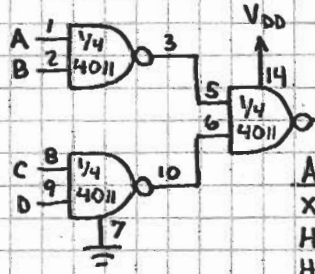
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	H

EXCLUSIVE-OR GATE



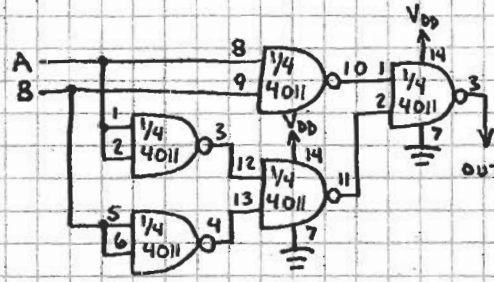
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	L

AND-OR GATE



A	B	C	D	OUT
X	X	H	H	H
H	H	X	X	H
H	H	H	H	H

EXCLUSIVE-NOR GATE



A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	H

Engineer's newsletter

Lossy chokes could sap gate speed

On this page on June 22, Iklil Kayihan suggested that vhf noise on TTL power supply lines could be damped using lossy chokes. But D. S. Walton of Icthus Instruments Ltd., Gateshead, Tyne and Wear, England, disagrees. He says that noise voltages on a system's supply lines are caused by changes in a gate's output, causing rapid changes in current demand—**on the order of 50 mA in as little as 1 ns.** This demand must be met rapidly, or else the gate speed and thus system speed will suffer.

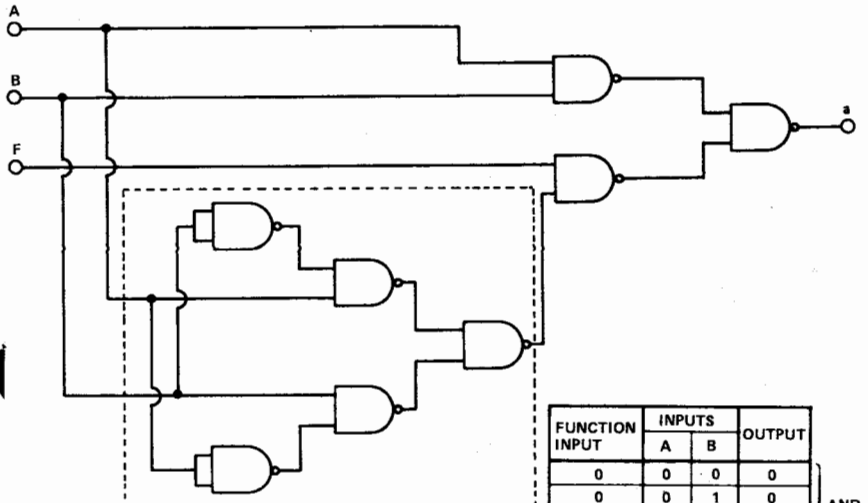
Walton notes that any inductance inserted between the gate package and the decoupling capacitor opposes any rapid change in current demand and so actually does slow down the gate. Rather than add more inductance, his recipe for low-noise power distribution more or less follows the conventional approach—use a large enough decoupling capacitor (1 μF or so per package) to meet the transient current demand without introducing a significant voltage drop. The stray inductance between capacitor and package should also be held to a minimum.

Programmable Gate

P. Mead

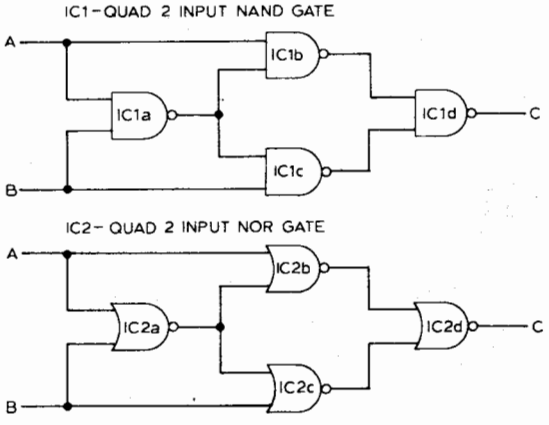
The Programmable Gate is a gate which converts an AND gate to an OR gate by applying a logic '1' on the function input.

The logic design uses 8 x 2 input NAND gates. The number of gates may be reduced by replacing the 5 NAND gates enclosed by the dotted line, with a 2 input exclusive OR, such as the TTL 7486.



FUNCTION INPUT	INPUTS A	INPUTS B	OUTPUT	
0	0	0	0	AND FUNCTION
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	OR FUNCTION
1	0	1	1	
1	1	0	1	
1	1	1	1	

Exclusive OR and NOR gates D. S. Smith



TRUTH TABLE

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

When constructing logic circuits which need either an exclusive OR gate or exclusive NOR gate, and one is not available, the following arrangement of NAND or NOR gates can produce the required results. The circuits can be constructed using standard TTL or CMOS gates.