wireless world circard

Set 11: Basic logic gates

The *W.W.* article introducing this subject must have been of limited value for newcomers to logic as a result of a few typographical errors that crept in. These are corrected of course, the main errors being in lines 29 & 30 of Table 1 and in Table 6. The article forms a good introduction to Boolean algebra rules, truth tables and logic symbology (but for details of the Karnaugh map technique see article on page 60). The cards detail the different realizations of logic gates, card 4 being especially useful in summarizing the different kinds of NAND gate (standard, low power, high speed and Schottky). Card 8 is arguably the most useful giving circuits for interfacing between different kinds of logic circuits. Interfacing with analogue circuitry to form shunt or series choppers, as used in multiplexers, is covered in card 11. Three cards deal with newer kinds of logic systems. Card 9 describes the nomenclature used in threshold logic—a generalized approach of which the simple gates form special cases. Optical logic gates, three-state logic and majority gates are covered on cards 10 & 12. Set 16 card 4, and set 18 card 2 give logic circuits using current differencing amplifiers.

Basic logic gates

Logical or arithmetic processes are extensively used in systems such as industrial control, computers, electronic instrumentation and automatic telephone exchanges. These processes often involve complex functions of several variables, the desired functions being realized by switching operations in a logical manner. Although much of the design of these systems now deals with the interconnection of complex functional blocks, successful results also depend on a knowledge of the basic elements that constitute the complex functional blocks.

The basic elements of such systems are logic gates, which may perform combinational operations on their inputs. These inputs will normally be in one of two allowed states that could be, for example, two different voltages, two different currents or two different resistance values such as the limiting cases of open circuit and short circuit. Whatever form the allowed states take, a logic gate is concerned with whether certain statements about its inputs, at a given instant, are true or false. If these statements are made using normal language they become unmanageable as the number of quantities involved increases, making some form of symbolic statement highly desirable.

If a certain statement is true it is assigned the value 1 and if it is false it is given the value 0. For example, if one of the inputs to a logic gate is called A and it can be either at 5 V or 0 V then the statement "input A is at 5 V" may be true or false. If it is true than A = 1 and if it is false then A = 0. If this gate has three inputs and its output, D, is only at 5 V (D = 1) when two of its inputs, A and B, are at 5 V and its other input, C, is at 0 V, then D = 1 when A = 1 AND B = 1 AND C = 0.

Now C = 0 implies that C is NOT 1 i.e. $\bar{C}$ = 1, where the bar indicates NOT or negation, so the above statement could be simply written as D = A AND B AND C. Using the multiplication sign of normal algebra (× or .) to represent the AND operation this statement becomes D = A × B × $\bar{C}$, or D = A.B.$\bar{C}$, or even D = AB$\bar{C}$ where the "multiplication" (AND) signs are implied. This type of algebra, based on logical statements that are true or false, is called Boolean algebra and it is a very useful tool in the development of logical thinking and in the design of digital circuits and systems.

TABLE 1. Properties of Boolean algebra.

1	0+0	=0	11	$\bar{A}$.A	=0	21	A. (B+C)	=A.B+A.C
2	0.0	=0	12	$\bar{A}$+A	=1	22	A+A.B	=A
3	1+1	=1	13	0+A	=A	23	A+$\bar{A}$.B	=A+B
4	1.1	=1	14	0.A	=0	24	A.(A+B)	=A
5	0.1	=0	15	1+A	=1	25	(A+B).(A+C)	=A+B.C
6	0+1	=1	16	1.A	=A	26	$\overline{A+B}$	=$\bar{A}$.$\bar{B}$
7	$\bar{0}$	=1	17	A+B	=B+A	27	$\overline{A.B}$	=$\bar{A}$+$\bar{B}$
8	$\bar{1}$	=0	18	A.B	=B.A	28	$\bar{\bar{A}}$	=A
9	A+A	=A	19	(A+B)+C	=A+(B+C)	29	$\overline{\bar{A}+\bar{B}}$	=A.B
10	A.A	=A	20	(A.B).C	=A.(B.C)	30	$\overline{\bar{A}.\bar{B}}$	=A+B

Table 2. Boolean theorems in terms of relay contacts.

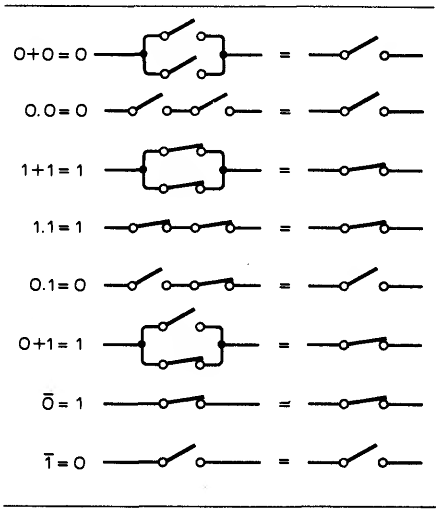
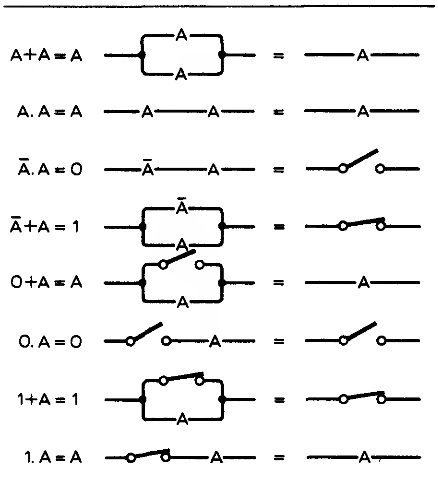


Table 3. Boolean theorems in one variable.



As well as the AND and NOT operations it is necessary to postulate the OR operation which is represented by the (+) symbol of normal algebra. For example, if a logic gate has two inputs A and B, and its output D is in the logic 1 state when either A or B is in the logic 1 state this statement can be written as D = A OR B which is represented by D = A + B.

A logic gate is an example of a basic logical circuit, called a combinational circuit, the output of which at a given instant is determined by the state of its inputs. Irrespective of its complexity, certain relationships, laws and simplification rules of Boolean algebra can be used to represent or investigate the behaviour of a combinational circuit. Using up to three variables, Table 1 shows some of the properties of this algebra some of which are the same as ordinary algebra. In Boolean algebra division and subtraction have no meaning and the variables can only have the values 0 or 1. Table 2 shows the Boolean algebra theorems relating the values 0 and 1 in terms of relay contacts that are either open (logic 0) or closed (logic 1). Table 3 illustrates the Boolean algebra theorems in one variable A in similar terms, where A can have either of the states 0 (A-contact open) or 1(A-contact closed). In Table 1 relations 26 & 27 together are known as De Morgan's theorem and 29 & 30 are identical with 26 & 27 except that the variables have been negated (or inverted or complemented).

Combinational logic circuits may take many different forms, one of which employs relay contacts which is useful for illustrating some of the simple Boolean relations. For example, in Figs 1 & 2, A, B and C are contacts operated by relay

*All with Paisley College of Technology.

coils (not shown) to complete a path between input and output. Thus, we are concerned with the statement "the connection between input and output is complete".

When this statement is true D = 1 and when it is false D = 0. In Fig 1, D = 1 only when contacts A AND B AND C are closed simultaneously so the Boolean representation is D = A.B.C. Hence, series-connected contacts of the same type provide the AND operation. In Fig. 2, D = 1 when contacts A OR B or C are closed so the situation may be represented by D = A + B + C. If more than one contact is closed the above statement is still true, i.e. D = 1. Thus, parallel-connected contacts of the same type provide the OR (or "inclusive" OR) operation and the order in which they are wired or considered does not affect the truth of the statement.

The validity of a Boolean statement representing the behaviours of a combinational logic gate can be checked by means of a truth table. which is a tabular listing of all possible logic combinations of the variables and the resulting output logic. Tables 4 & 5 are the truth tables for Figs 1 & 2 respectively and they show that a complete truth table requires 2^n rows to represent a gate having n variables. Table 6 is a listing of the truth tables for the commonly-used combinational logic operations and shows the names given to the logic gates used to realize these operations. The NOR (NOT OR) gate performs the complement of the OR function and the NAND (NOT AND) gate the complement of the AND function.

TABLE 4. Truth table for Fig. 1

A	*B*	*C*	*D*
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

TABLE 5. Truth table for Fig. 2

A	B	C	D
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

Unlike the OR gate, the "exclusive" OR gate only makes D = 1 when either A = 1 OR B = 1 but not when A = B = 1. The exclusive OR operation is used so frequently that it is given the symbol $\oplus$. Thus, $D = A\bar{B} + \bar{A}B = A \oplus B$.

Examples have been given of basic logical operations realized by means of relay contacts but this technique can become unwieldly. A more general diagrammatic representation of logic gates is desirable as the logic diagram should be independent of the circuit techniques employed in their realization. Unfortunately, there is no universally accepted symbol* to represent a particular logic gate, some of the different types of symbols that have been used being shown in Fig. 3.

While the operation indicated by a logic gate symbol is independent of the circuitry used, it should be realized that as there are two allowed states the user must decide which state is to represent the logical 1 condition. For example, if the two states are represented by voltage levels, one may be positive and the other 0 V, one may be negative and the other 0 V, one may be positive and the other negative, both may be positive or both negative. Irrespective of the values of these voltage levels, the system is said to use positive logic if the logical 1 state is represented by the more positive level and is said to use negative logic if the logical 1 state is represented by the more negative voltage level.

Although all the combinational logic gates appearing in Table 6 are available in various forms of hardware, it is possible to build complete logic systems with either only NOR gates or only NAND gates. Fig. 4 shows how the AND, OR, NOR and exclusive-OR operations may be realized using only NAND gates and Fig. 5 shows the sole use of NOR gates to

*Following a majority decision of the I.E.C., the B.S.I. have opted for the rectangular logic gate symbols (not shown in Fig. 3). BS3939 section 21 is currently being amended. — Ed.

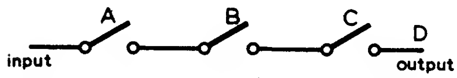


Fig. 1: D = 1 when contacts A AND B AND C are closed, represented by D = A.B.C.

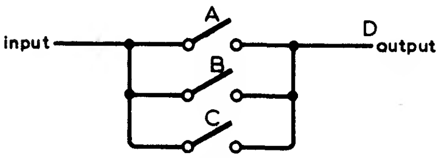


Fig. 2. D = 1 when A OR B OR C are closed, represented by D = A + B + C.

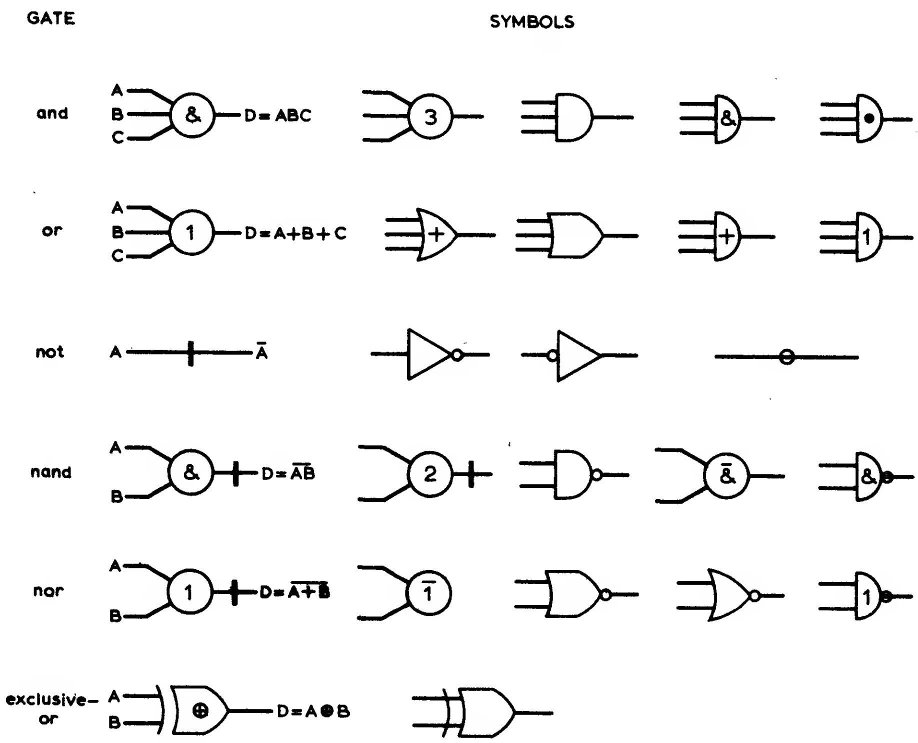


Fig. 3. Some of the symbols used for logic gates.

TABLE 6. Truth tables for common combinational logic operations.

INPUTS		OUTPUT D =				
A	B	A.B	A+B	$\overline{A+B}$	$\overline{A.B}$	$A \oplus B$
0	0	0	0	1	1	0
1	0	0	1	0	1	1
0	1	0	1	0	1	1
1	1	1	1	0	0	0
NAME OF GATE		AND	OR	NOR	NAND	EXCLUSIVE — OR

realize the AND, OR, NAND and exclusive-OR operations. These illustrations also show the application of some of the relations given in Table 1. Figs 4(a) & 4(b) use relations 28 & 30 respectively on the output function and relation 30 is also used on the output from the three-input NAND gate in Fig. 4(c). In Fig. 4(d), relations 27, 21 & 11 are used in turn on both inputs to the final gate and relation 30 used on its output function. Figs 5(a) & 5(b) use relations 29 & 28 respectively on the output function, relation 29 also being used on the output of the three-input NOR gate in Fig. 5(c). In Fig. 5(d) relation 29 is used on the input to the final gate and relations 27, 26, 21 & 11 used in turn on its output function.

These examples show that more gates of a given type are required to realize any other particular simple logic function. Although this point has been illustrated by simple Boolean expressions, in the design of more complicated systems the algebra may be cumbersome and other techniques such as Karnaugh mapping would be used to obtain a minimal solution. To synthesize a complex system it may be advisable to use gates of one type because of their availability and cost.

Many different types of solid-state electronic logic-gate realizations are available such as resistor-transistor logic (r.t.l.), diode-transistor logic (d.t.l.), direct-coupled transistor logic (d.c.t.l.), transistor-transistor logic (t.t.l.), emitter-coupled logic (e.c.l.) and complementary metal oxide transistor logic (c.m.o.s.). These families of gates have different characteristics and one family may prove to be more suitable than another in a particular application. For example, the prime consideration may be highest possible speed of operation or lowest power consumption or greatest immunity to external noise or the simplicity of interfacing the gates with other circuitry. The successful design of a digital system therefore requires a working knowledge of the capabilities of the various types of electronic gates available.

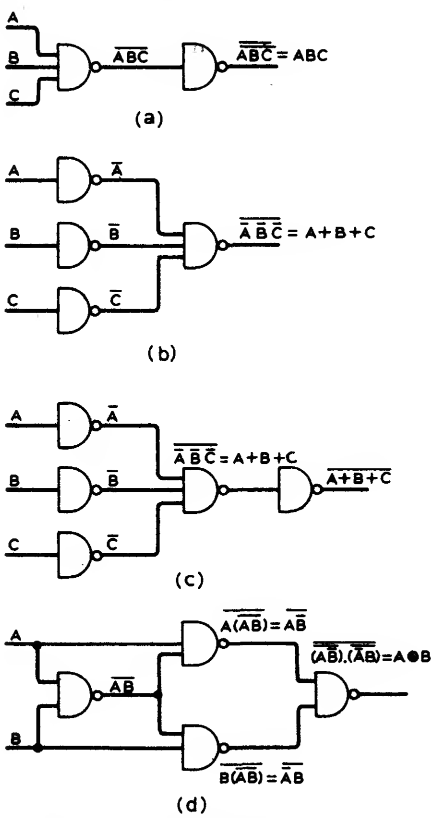


Fig. 4. Logic operations of AND (a), OR (b), NOR (c) and exclusive OR (d), can be realized using only NAND gates.

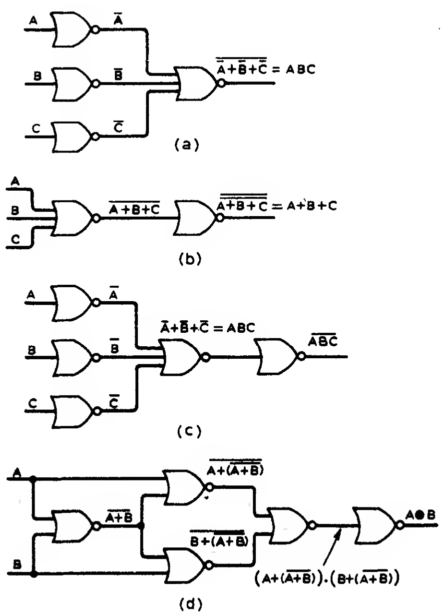
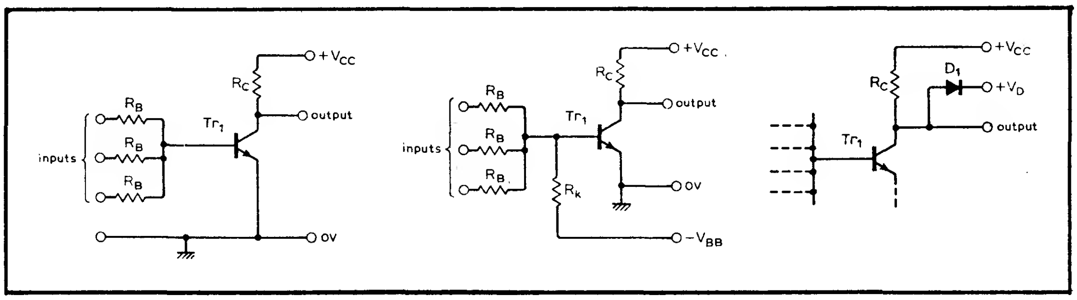


Fig. 5. NOR gates can realize the logic operations of AND (a), OR (b), NAND (c) and exclusive OR (d).

Resistor-transistor and direct-coupled gates



Typical r.t.l. parameters
$+V_{CCmin}$ 20V
$+V_{CCmax}$ 28V (4mA)
$-V_{BB}$ 0V (with silicon transistors)
R_B 82kΩ, R_K 30kΩ, R_C 7.5kΩ
logical 0 level 300mV max
logical 1 level 14V min
Fan-in 4
Fan-out 6
Maximum frequency 10kHz

Simple r.t.l.
The simplest resistor-transistor logic (r.t.l.) gate, which performs the positive logic NOR function, is shown left. A positive voltage applied to any input turns Tr_1 on, causing V_{out} to fall from V_{cc} to a value that depends on the base drive. If sufficient base drive is applied, Tr_1 saturates making V_{out}= V_{CEsat}, representing the logical 0 state. Positive voltages applied to the other inputs increases the degree of saturation and only change V_{out} by a small amount. If logical 0 voltages (V_{CEsat}) are supplied to all inputs the base-emitter juction of Tr_1 will be only slightly forward biased ($V_{CEsat} \approx 0.1$ to 0.4V) and $V_{out} \approx +V_{CC}$. For useful logic functions the gate must feed some load, causing an additional current I_L to flow in R_C and hence reducing the logical 1 value of V_{out} below V_{CC}. The gate is also a negative-logic NAND gate.

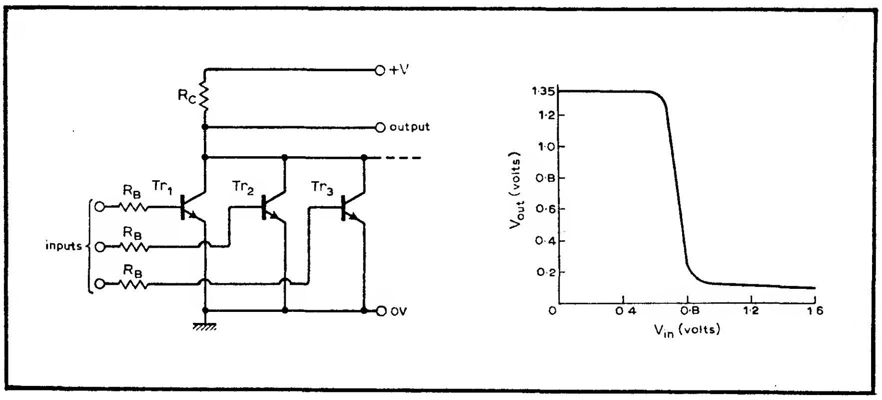
Improved r.t.l.
Inclusion of a base bias resistor, R_K in the middle circuit, returned to a negative supply ensures that Tr_1 is definitely turned off when all inputs are below the input logical 1 threshold and reduces the transistors turn-off time. Speed-up capacitors can be placed in parallel with each input R_B to produce resistor-capacitor-transistor logic. However, if all inputs are at logical 1 voltages and one of them rapidly switches to the 0-state, its speed-up capacitor couples the negative-going transition to the base-emitter junction of Tr_1 which can cause the transistor to temporarily switch off. For this reason r.t.l. gates are normally only used at fairly low switching speeds.
A clamping diode D_1, shown right, can be connected to a supply $+V_D < +V_{CC}$ to make the logical 1 output voltage less dependent on the load current, provided that the drop across R_C does not cause D_1 to become reverse-biased.

Direct-coupled logic
Direct-coupled-transistor logic is also referred to as direct-coupled logic and collector-coupled-transistor logic, but it is strictly incorrect to refer to it as resistor-transistor logic as is done by some manufacturers since the input resistors have no logic function. The base resistors bottom serve only to divide the current between transistors when their inputs are paralleled. The gate is a positive-logic NOR gate which uses the transistorsas summing elements. The transistors also provide input- output isolation and restoration of the logic levels in each gate in a cascade. A positive voltage at any input turns on its associated transistor causing V_{out} to fall to V_{CEsat}, the logical 0 level. With all inputs at logical 0 the transistors are virtually cut off causing V_{out} to rise towards $+V$ until the transistors in the following gates turn on.
For correct operation R_C and R_B values must be chosen to ensure that driven transistors turn on when the driving gate transistors turn off. Also, when the driving gate is on the driven transistors must be off, hence the threshold value of V_{BE} must exceed V_{CEsat}. The difference between these two values influences the gate's noise immunity. Discrete-circuit versions allow individual trimming of the base resistors to compensate for unequal V_{BE} values. Integrated circuit versions have closely-matched V_{BE} and V_{CEsat} values due to simultaneous manufacture on the same substrate.
Fan-in capability is limited by collector leakage currents which, for several transistors off simultaneously, could cause V_{out} to fall below the level required to ensure that the following transistors are turned on. This is particularly so in low-power versions of the gate. A typical transfer characteristic is shown below.

Further reading
Dokter, F., & Steinhauer, J. Digital Electronics, chapters 4 & 5, Macmillan, 1973.
Harris, J. N. *et al* Digital Transistor Circuits, chapters 6 & 7, Wiley, 1966.

Typical d.c.t.l. parameters

Parameter	normal	low-power
+V	3.6V	3.6V
R_C	640Ω	3600Ω
R_B	450Ω	1500Ω
Fan-out	5	5
Gate dissipation	12mW	2.5mW
Propagation delay	24ns	45ns
logical 1 level	1.2V	1.2V
logical 0 level	200mV	200mV
Noise margin, min ("1")	400mV	400mV
Noise margin, min ("0")	350mV	350mV



Diode-transistor gates

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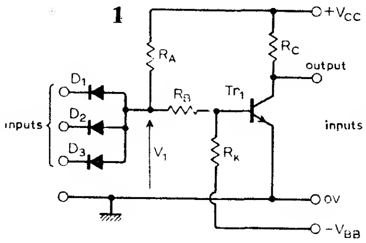

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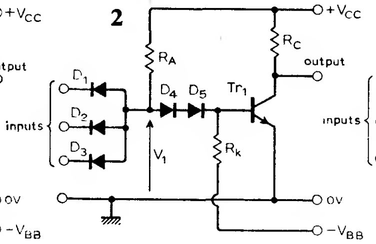

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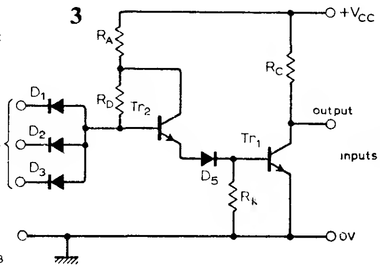

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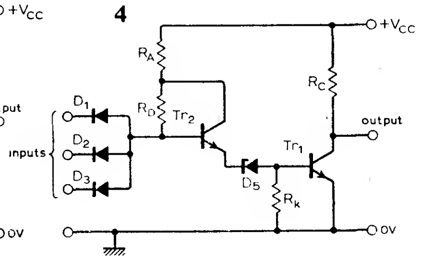

Fig. 1 shows a diode-transistor logic (d.t.l.) NAND gate, using discrete components, which is effectively a diode-logic AND gate followed by an inverting transistor. Resistors R_A, R_B and R_C act as a level-shifting potential divider designed to provide enough base drive to allow Tr_1 to saturate, making $V_{out}=V_{CEsat}$ (logical 0), when all input diodes conduct due to logical 1 levels being present at all inputs. If any input is at logical 0 V_{CEsat}, its associated diode conducts, causing V_1 to fall to the forward voltage of the diode. The transistor is then held in the cut-off state by the reverse bias obtained by potential division of V_{BB} between R_K and R_B and the output goes to the 1-level as its collector rises towards $+V_{CC}$. The turn-off of Tr_1 is assisted by the negative base voltage and the turn-on time may be reduced by shunting R_B with a speed-up capacitor. The fan-in is that of a diode logic gate and the fan-out depends on the current-sinking ability of Tr_1. Preservation of logic levels may be improved by including a collector clamp diode—see card 1.

Another version of the d.t.l. NAND gate, sometimes called low-level logic, is shown in Fig. 2 where R_B and its speed-up capacitor are replaced by the input-offset diodes D_4 and D_5, which are more suitable for monolithic integrated fabrication techniques. Only a relatively small voltage swing is required at the base of Tr_1 to switch it on or off, but in Fig. 1 a relatively large swing in V_1 is required to achieve this due to the large part of V_1 lost across R_B. The use of D_4 and D_5 in Fig. 2 leads to a much smaller required swing in V_1 to achieve the desired base voltage swing. Hence the signal levels may be lowered to reduce gate dissipation which also falls due to the removal of R_B.

Other diodes may be placed in series with D_4 and D_5 to improve noise immunity. While the input diodes should have a very short reverse recovery time, the level-shifting diodes D_4 and D_5 should be slow recovery types to ensure that they do not return to their high-impedance, reverse-biased state until Tr_1 has cut off.

Elimination of the V_{BB} supply can simplify circuitry in many instances, a popular modified form of the d.t.l. NAND gate using a single supply being shown in Fig. 3. In comparison with Fig. 2, the offset diode D_4 is replaced by Tr_2 and R_D. This transistor provides amplification

Typical d.t.l. parameters

Parameter	Fig. 2	Fig. 3	Fig. 4	Fig. 5
$+V_{CC}$	4V	5V	15V	15V
$-V_{BB}$	2V	—	—	—
R_A	2kΩ	1.6kΩ	3kΩ	3kΩ
R_C	2kΩ	6kΩ	15kΩ	15kΩ
R_D	—	2.15kΩ	12kΩ	12kΩ
R_E	—	—	—	1.5kΩ
R_K	20kΩ	5kΩ	5kΩ	5kΩ
Fan-out	5	8	10	10
Gate dissipation	10mW	10mW	28mW	28mW
Propagation delay	30ns	30ns	125ns	110ns
Noise margin ("1")	0.4V min	0.4V min	5V	5V
Noise margin ("0")	0.35V min	0.35V min	5V	5V

that allows a higher level of base drive to be fed to Tr_1, achieving a higher fan-out capability, and also permits a reduction in the value of R_K compared with Fig. 2.

Gates used in industrial logic systems often require high noise immunity, rather than high speed and low power dissipation, as large transients can be produced in supply lines or picked up at inputs due to switching of relays, etc. Fig. 4 shows a modified form of Fig. 3 that exhibits higher noise margins largely due to D_5 being changed from a forward-biased diode to a reverse-biased diode exhibiting a zener-type characteristic when the p.d. across it reaches about 6.7V. Thus the input threshold voltage is increased by an amount equivalent to the p.d. that would occur across a further four forward-biased diodes connected in series with D_5 in Fig. 3, but is achieved by using only one such diode operating on its reverse characteristic. A higher supply voltage is required in Fig. 4 but to prevent large increases in currents, and hence gate dissipation, all resistor values are also increased. Fig. 6 shows typical transfer characteristics for the circuits of Figs. 3 & 4. Fig. 5 shows the high noise-immunity gate of Fig. 4 with an active pull-up transistor Tr_3. When Tr_1 is off R_C supplies base drive to Tr_3 which supplies load current via R_E. With the output in the 0-state Tr_3 is off and Tr_1 sinks load current through D_6 which causes the low logic level to exceed V_{CEsat} of Tr_1. The table shows a comparison of some typical parameters for integrated circuit versions of Figs. 2 to 5.

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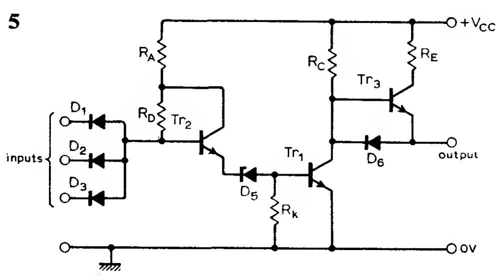

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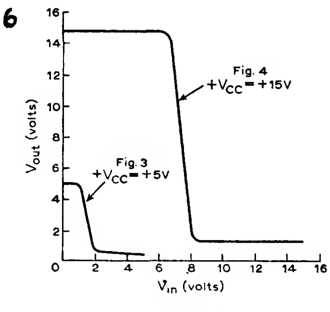
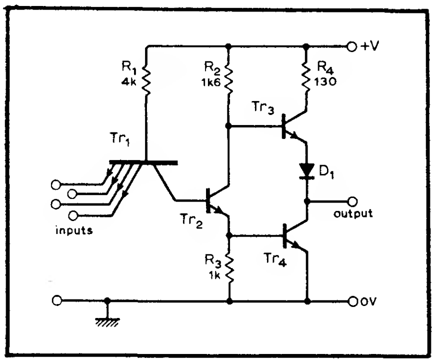


Further reading

Dokter, F. & Steinhauer, J. Digital Electronics, chapters 4, 5 and 6, Macmillan, 1973.

Meindl, J. D. Micropower Circuits, chapter 11, Wiley, 1969.

Basic t.t.l. gate



Typical parameters
Temperature range: 0 to 70°C
+V min 4.5V, +V max 5.5V
"0" supply current 22mA max
"1" supply current 8mA max
Fan out 10 t.t.l. loads
Inputs:
"0" level 800mV max
"1" level 2V min
"0" level 1.6mA max at +V max
"1" level 40μA max with V_{IN}=2.4V

Outputs:
"0" level 400mV max at +V min
"1" level 2.4V min at +V min
"0" level 16mA
Short-circuit output current: 18 to 55mA at +V max
Propagation delay* from "1" to "0" 15ns max
Propagation delay* from "0" to "1" 22ns max
"1" noise margin 400mV min
"0" noise margin 350mV min
Gate dissipation 10mW
*With output loaded by 400Ω//15pF.

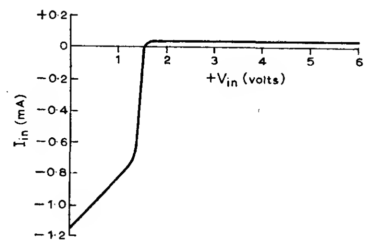
Circuit description
Circuit shows the form of the basic transistor-transistor logic gate which performs the positive logic NAND function and which may normally have up to eight inputs. If all the inputs are at a high level (logical 1), base drive is provided to Tr_2 through R_1 and the base-collector junction of Tr_1. If any one or more input is at a low level (logical 0), the current in R_1 flows through the base-emitter junction of Tr_1 to ground. The base will then be only V_{BE1} above V_{IN} and Tr_2 cut off due to lack of base drive. Transistor Tr_1 thus performs the AND function as its collector is only high if all its inputs are high. Transistor Tr_2 acts as a phase splitter that saturates with only a moderate current gain—note the small ratio of R_1/R_2 with $R_2 \approx R_3$. When Tr_2 is cut off its collector and emitter are approximately at +V and 0V respectively. When Tr_1 drives Tr_2 on, its emitter rises to V_{BE4} and its collector falls to ($V_{BE4}+V_{CE2sat}$). In this state Tr_4 will be saturated so that the output will be at V_{CE4sat} (logical 0) when all inputs are in the high state. In this condition the gate can sink current through Tr_4 from a number of loads, normally a maximum of 10, in the 0-state, without causing V_{CE4sat} to rise above the acceptable 0-threshold.
If any of the gate inputs is in the low state, Tr_4 will be off as Tr_2 is cut off. Transistor Tr_3 will be on to an extent determined by the emitter current demanded at the output. This current will be small when the gate feeds a number of similar t.t.l. gates and its base current will be smaller still. Hence the p.d. across R_2 due to Tr_3 base drive will be negligible and the output will be in the high state with V_{out} at approximately $+V-(V_{D1}+V_{BE3})$.

Switching action
When switching the output from the 0- to the 1-state, all inputs are initially high (logical 1). As the potential of one or more input falls, nothing happens until it reaches about 1.4V, when the source current via Tr_1 base-emitter junction prevents base current flowing to Tr_2 via the base-collector junction of Tr_1, which rapidly removes the stored charge from Tr_2 base and switches it off. The collector potential of Tr_2 starts to rise as this transistor turns off, but stops rising as Tr_3 begins to conduct heavily. This conduction occurs because Tr_4 has not yet switched off, as the charge stored in its base decays only relatively slowly through R_3. Therefore, a large current spike of short duration and limited in amplitude by R_4 occurs in the supply line during the switch-off action due to Tr_3 and Tr_4 being simultaneously on. This conduction in Tr_4 removes some of the stored base charge, allowing the output voltage and Tr_2 collector potential to rise. The rise continues until Tr_3 becomes cut off and the output settles to the 1-level. Typical input, output and transfer characteristics are shown in Figs. 2, 3 & 4 respectively. Width and amplitude of the current spike are virtually unaffected by the rate at which the gate is switched on and off. Hence a side effect of the current spike is an increase in power consumption as the switching frequency increases.

Unused inputs
Inputs that are unused in a particular application should be connected in parallel with used inputs for fastest switching speed. Unused inputs can be left open circuit, but excessive pick-up noise may result unless the open circuit is made at the integrated circuit package connection. If unused inputs are connected to the positive supply rail, it is advisable to do so via a resistor of around 1kΩ to prevent the gate being damaged by a supply line transient that exceeds the maximum rating.

Further reading
Scarlett, J. A. Transistor-Transistor Logic and its Interconnections, chapters 1 to 6, Van Nostrand, 1972.

2



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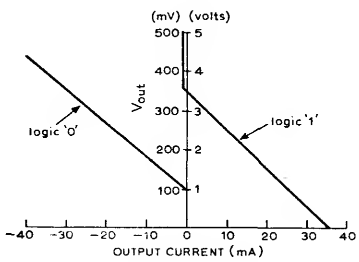

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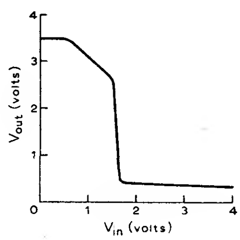
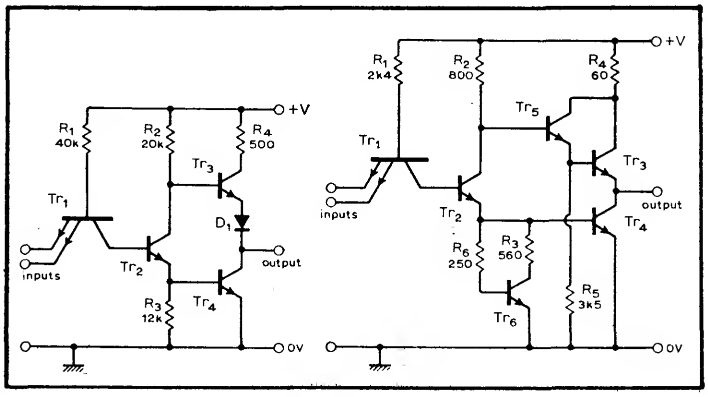


NAND gate variations in t.t.l.



In the basic, or standard t.t.l. NAND gate (card 3), the resistance values affect performance. Resistor R_1 influences the rate of rise of voltage at Tr_2 base and turn-on time. Gate dissipation, when the output is in the 0-state is affected by the value of R_2. Stored base charge in Tr_4 is removed via R_3 when the output state changes from logical 0 to 1. Turn-off time of the gate when feeding a capacitive load is influenced by the value of R_4 which provides short-circuit protection.

Low-power t.t.l.
For low-power operation the resistor values must be increased to reduce the charging-discharging currents. But larger resistors imply slower switching speeds unless transistor size is reduced to lower their capacitances. This can be done due to the lower current levels and by reducing the degree of gold doping the transistors achieve higher current gains to better-utilize the smaller currents. The resulting gate, top left, has a power dissipation only one-tenth of that in a standard gate with a speed reduction penalty of only three times.

High-speed t.t.l.
To obtain higher switching speeds than are obtainable with standard t.t.l., the charge-discharge rates of the integrated and external capacitances must be increased. This implies larger transistor currents and hence lower resistor values. The higher currents require larger transistors having increased capacitances that tend to offset the speed increase due to higher currents. A distinct speed improvement is obtainable, the high-speed NAND gate shown above having about double the speed and slightly more than twice the dissipation of the standard gate.
The Darlington-connected pull-up transistors Tr_5 and Tr_3 provide higher active-region gain which reduces the output resistance and increases the ability to drive capacitive loads. Resistor R_5 is sometimes returned to the output point, rather than to the 0-V rail, to reduce the gate dissipation. Sometimes a by-pass transistor, Tr_6, is added to the pull-down transistor, Tr_4, as shown right. Resistance of the discharge path for stored base charge in Tr_4 is reduced, improving the turn-off time. Transistor Tr_2 cannot conduct through R_3 until its emitter voltage exceeds the turn-on V_{BE} of Tr_6 which is approximately the same as that of Tr_4. Hence, the output remains in the 1 state until V_{IN} rises to a level sufficient to turn on Tr_4, which removes the low-slope region from the transfer characteristic improving noise immunity.

Schottky-clamped t.t.l.
Excess base drive is shunted through the diode, which clamps the collector-base junction with a p.d. of 400mV which is insufficient to produce any significant forward conduction. The elimination of gold-doping provides higher-gain, physically-smaller transistors with very little charge storage and hence much higher switching speeds without the penalty of further increased power dissipation. Use of Schottky-clamped transistors increases the output 1-level improving its noise immunity. Transistor Tr_4 below has very little stored base charge, improving the turn-off time and reducing the supply current spike. As this transistor's V_{CEon} determines the output 0-level, the level will be raised by about 100mV compared with the standard gate but its value will be far less temperature dependent. The table shows a comparison of some typical parameters of different t.t.l. NAND gates.

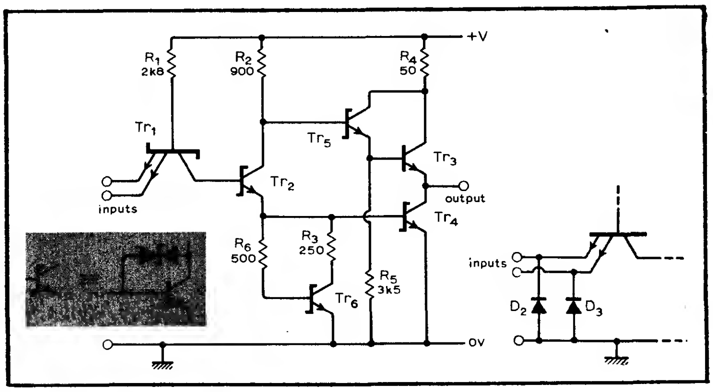
Input clamping diodes
Most t.t.l. gates have input clamping diodes to ground, as shown on right to reduce the negative excursions of input signals due to ringing caused by reflection of pulses along the interconnection transmission lines.

Further reading

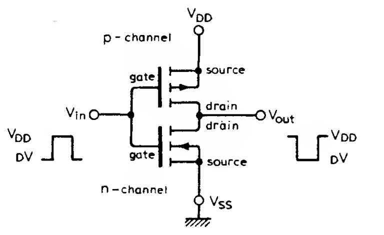
Priel, U. Take a look inside the t.t.l. i.c. *Electron*, pp. 24, 26 & 30, 19 April 1973.
Murphy, R. H. Performance and reliability aspects of current trends in t.t.l., *New Electronics*, pp. 30, 33 & 34, 20 April 1971.
Clifford, C. Guide to low-power t.t.l., *New Electronics*, pp. 24, 27 & 28, 4 May 1971.
Scarlett, J. A. Transistor-Transistor Logic and its Interconnections, chapters 3, 4 & 9, Van Nostrand, 1972.

Cross references
Set 11, card 3; set 10, card 11.

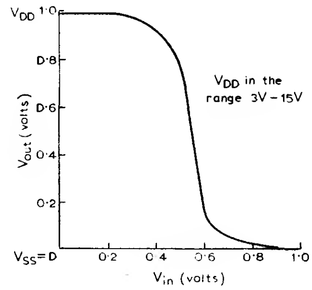
Parameter	standard	low-power	high-speed	schottky
+V	5V	5V	5V	5V
"0" current	5.5mA	0.46mA	10mA	9mA
"1" current	1.3mA	0.18mA	4.2mA	4.25mA
Fan out	10	10	10	10
Gate dissipation	10mW	1mW	22mW	20mW
Output delay "1" to "0"	8ns	30ns	6ns	3ns
Output delay "0" to "1"	12ns	30ns	6ns	3ns
Noise margin "1"	400mV	400mV	400mV	700mV
Noise margin "0"	400mV	400mV	400mV	300mV
V_{INmax} "0"	800mV	700mV	800mV	800mV
V_{INmin} "1"	2V	2V	2V	2V
V_{OUT} "0"	400mV	300mV	400mV	500mV
V_{OUTmin} "1"	2.4V	2.4V	2.4V	2.7V
I_{IN} "0"	1.6mA	0.18mA	2.0mA	2.0mA
I_{IN} "1"	40μA	10μA	50μA	100μA
I_{OUT} "0"	16mA	2mA	20mA	20mA



Complementary m.o.s. gates—1



Typical data
IC $\frac{1}{3}$ (CD4007AE)
Working voltage range (V_{DD} $-V_{SS}$) 3 to 15V
Temperature range −40 to +85°C
Input capacitance 5pF
Input resistance $>10^9\Omega$
Output voltage (high) 9.99V (V_{DD} =10V, V_{SS}=0V)
Output voltage (low) 0.01V (V_{DD}=10V, V_{SS}=0V)
Fan-out d.c. >1000
a.c. typically 20

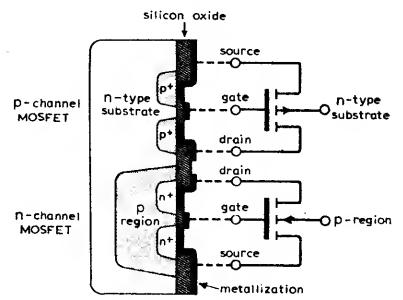


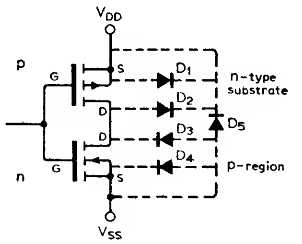
Description
The circuit shows the basic complementary-symmetry isolated-gate inverter stage, which uses both an n-channel and a p-channel enhancement-mode m.o.s.f.e.t. in a series-pair configuration. Such circuits can be directly coupled as either transistor will be in its non-conducting or off-state if its gate-source voltage is zero. Individual gates are tied together to form a single signal input gate, and the drains are commoned at the output. Assume that the input signal excursion is from $+V_{DD}$ to ground potential i.e. $V_{SS}=0V$. When the input is $+V_{DD}$, the n-channel f.e.t. is biased to a high conducting state because V_{GS} is a high positive value. Simultaneously, the effective gate-source voltage of the p-channel f.e.t. is zero, and hence this transistor will be off, and the output will be at ground potential. When the input goes to zero volts (the low or 0-state for positive logic), the n-channel f.e.t. is biased off, but the p-channel transistor has now a large negative voltage between gate and source and is therefore biased into conduction, and the level then approaches $+V_{DD}$ (the high or 1-state). In either logic state, one transistor is conducting and the other is cut-off. It follows that the quiescent power dissipation is exceedingly low—the transistor that is off will only conduct leakage current, typically 1nA.

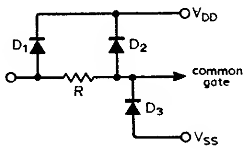
More significant power dissipation occurs during the switching from one level to the other, due to both a current spike which occurs when the inverter is in its linear region and to the charging and discharging of load capacitance. This depends on the frequency, the value of the capacitance and the square of the supply voltage.
If the p-channel source is connected to ground, the n-channel source should be connected to $-V_{DD}$ and the drive signal excursion should be from $-V_{DD}$ to 0V.

Construction
A cross-section depicting the formation of n-channel and p-channel transistors on the same chip is shown below, with associated symbols. The p-channel one is formed directly on an n-type substrate, but the n-channel device is formed in a p-region diffused into the substrate. This process creates parasitic diodes, and their relationship to the inverter terminals is shown centre. As V_{DD} is normally more positive than V_{SS}, these diodes are in a reverse-biased state, and their leakage current contributes to quiescent power dissipation. It should be noted that if the voltage level at the output terminal is subjected to any transient condition, it is unable to go more positive than V_{DD} or more negative than V_{SS}, by more than the forward conducting voltage of these parasitic diodes.

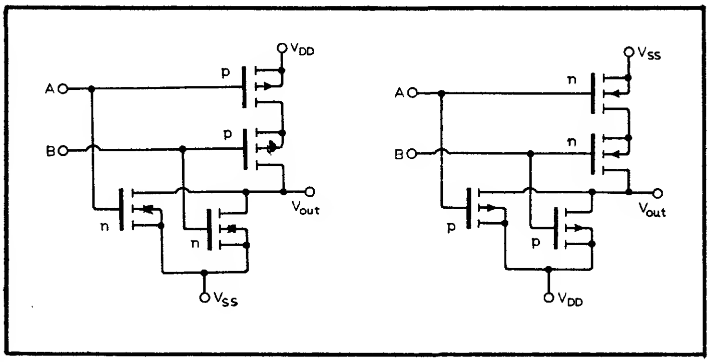
Input protection
Because the input resistance of the device is so high, static charges may be sufficient to charge the input capacitance of the gate oxide to a high enough voltage to cause breakdown (~100V). The diode protection network, below right is one type designed into some gates. If the gate terminal voltage is greater than V_{DD}, diodes D_1 and D_2 can conduct, and if less than V_{SS}, D_3 may conduct—the current magnitude should be limited to around 10mA (R may be around 2kΩ). For conditions where the diodes are either forward or reverse biased, the voltage across the oxide layer is limited to approximately 1 or 25V respectively.







Complementary m.o.s. gates—2



Typical data
$V_{DD} = +10V$, $V_{SS} = 0V$, T_{amb} 25°C.

Gate	drive p(source) (mA)	V_{out} (V)	drive n(sink) (mA)	V_{out} (V)	quiescent power (μW)	delay (ns)
Nor	1.0	9.5	2.5	0.5	0.05	25
Nand	1.2	9.5	0.6	0.5	0.05	25
Inverter-pair	2.5	9.5	2.5	0.5	0.05	20
Buffer	2.5	9.5	16.0	0.5	0.5	10 to 25

Basic gate structure
NOR and NAND functions are formed by series and parallel combinations of p and n pairs. For the NOR gate, the n-type f.e.ts are in parallel and the p-type in series as shown left. The circuit configuration of the NAND is similar but the p-types are in parallel, the n-types are in series, and the supply connections are changed over, see diagram right. The NOR logic action is described assuming V_{DD} is a positive voltage and V_{SS} is at 0V. Input excursions at A and B will be within the range 0V to V_{DD}. If either A or B is positive, then one of the p-types will be off and one of the n-types on, thus connecting V_{out} to 0V via the on-resistance of the conducting transistor. If both A and B are positive, again the output will be at 0V. If A and B are at 0V, then both p-types will be biased on, due to the negative voltage at their gates, and both n-types will be off, and hence V_{out} will be at $+V_{DD}$.

General notes
Noise immunity. Typically the input may change by up to $0.45V_{DD}$ before the output begins to alter. Over the full range of $V_{DD} - V_{SS}$ (3 to 15V), a noise immunity of $0.3V_{DD}$ is guaranteed.

Unused inputs. NOR gates: Connect input terminals together or to the lower voltage terminal V_{SS}. NAND gates: Connect input terminals together or to the voltage terminal V_{DD}.

Parallel gates. Gate outputs may be connected in parallel allowing greater output currents at the expense of increased power dissipation—current hogging need not be considered.

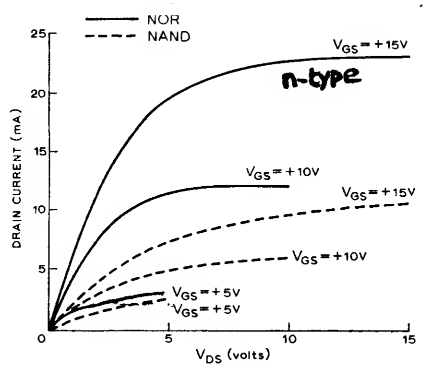
Pulse drive. Rise and fall times should be less than 5μs typically to prevent the device spending too long in the linear region during switching and thus increasing power dissipation.

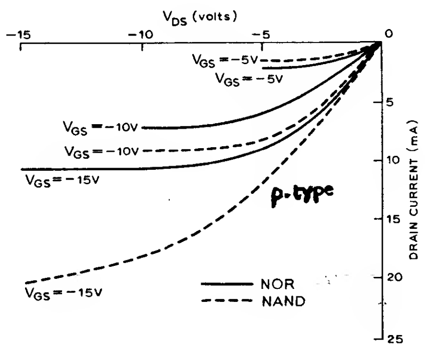
Output characteristics
The two graphs shown left illustrate typical n-device and p-device drain current characteristics for the NAND and NOR gate. Drain currents for the n-type in the NOR gate are much higher than those available in the NAND gate for the same gate-source voltage.

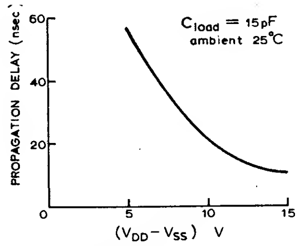
Propagation delay
Delay periods are usually defined between 50% points on the input and output level transitions, and this will depend to a great extent on the capacitive loading at the output, as this itself affects the transition time. Third graphs show that typical propagation delays depend on supply voltage, though in the 10 to 15V region the delay spread is of the order of 10ns.
As the capacitive loading is increased (each c.m.o.s. gate is an effective 5pF load), it is fairly easy to slow down.the circuits with external capacitance (right). The propagation delay is also temperature-dependent, increasing as the temperature increases due to fall-off in the g_m of the transistors.

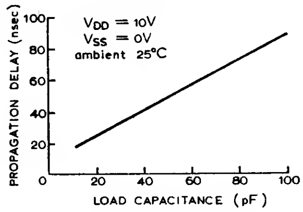
Development
Devices have been produced which operate with V_{DD} values (V_{SS}=0V) in the range 1.1 to 1.6V, and recently 0.7V. Another technology known as dielectric isolation, applicable to both types of c.m.o.s., promises devices with propagation delays as low as 10ns.

Further reading
Harrison, L., CMOS—Tolerant logic, *Electron,* 3 May 1973.
Ankrum, P. D., Semiconductor Electronics, Prentice-Hall.
Bishop, R. A. Complementary m.o.s. offers many advantages to the digital-systems designer, *Electronic Engineering,* Nov. 1972, pp. 67–70.
Funk, R. E. & Bishop, A. C.o.s.m.o.s. simplifies equipment design, *New Electronics,* 1 May 1973, pp. 24–8.

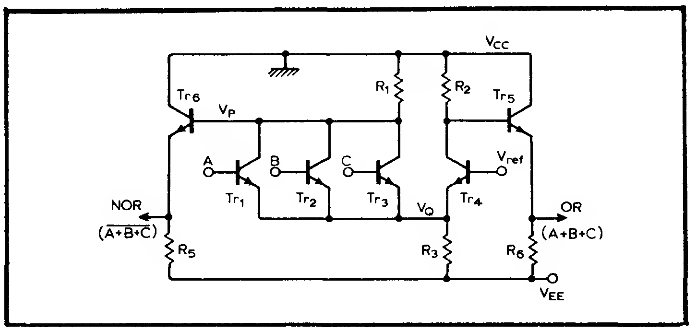




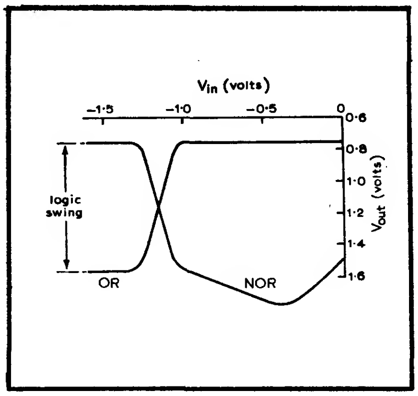




Emitter-coupled logic

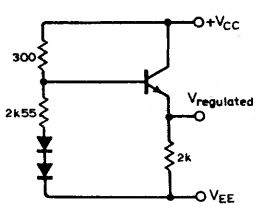


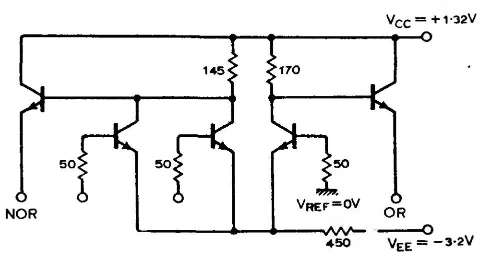
Typical operating data
R_1 270Ω, R_2 300Ω
R_3 1.2kΩ R_5, R_6 1.5 to 2kΩ
V_{CC} 0V, V_{ref} −1.15V,
V_{EE} −5V
Logic 1 output −0.75V
Logic 0 output −1.5V
Propagation delay 5 to 11ns
Max a.c. fan-out 15
Output resistance <0.1Ω
Output current 1.5 to 2mA to maintain logic levels within 3%
Temperature range 0 to 75°C.
Gate dissipation ≈ 35mW
Worst noise margin 250mV

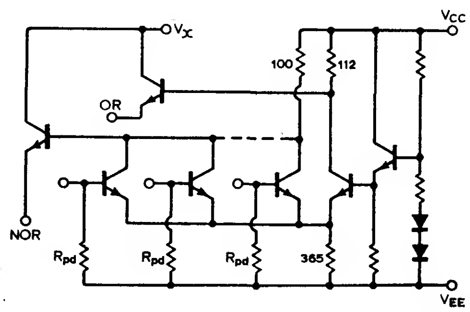


Circuit description
"Emitter-coupled logic" (e.c.l.) describes integrated logic circuits in which the switching transistors do not saturate as in other forms of bipolar transistor logic. Delays due to charge-storage effects in the saturated mode are avoided, leading to faster switching.
The above diagram is one form of a three-input basic e.c.l. gate, whose outputs provide an OR and the complementary NOR logic functions. The reference voltage must be well regulated, and of a level midway between the logic swings. For nominal logic high and low output of −0.75V and −1.55V respectively, this indicates $V_{ref} = -1.15$V. The following evaluation is for guidance only. If inputs A,B,C, are at the low logic level, Tr_1, Tr_2 and Tr_3 are cut off, Tr_4 is conducting and hence the potential at Q with respect to ground, assuming 0.75V drop across all emitter-base junctions, will be −1.9V, and the voltage across R_3 is $V_{EE} - V_Q$. Assume V_{EE} is −5V, then I=2.6mA. This means that the drop across R_2 is 0.78V and therefore the OR output will be −1.53V. As there is no current through R_1, V_P is 0V, and the NOR output is thus −0.75V due to the base-emitter junction drop.
When a logical 1 (−0.75V) is applied to, say, terminal A transistor Tr_1 will conduct harder than Tr_4, and the current in R_3 is then supplied via R_1, i.e. the current has been diverted from Tr_4 because the input voltage to Tr_1 is half a logic level more than that of V_{ref}, and the resultant reduction of the base-emitter drops of Tr_4 is sufficient to decrease its emitter's current to almost zero. Hence the base of Tr_5 is now at 0V and the OR output will be logical 1 at −0.75V. The related NOR is determined from the new V_Q value of −1.5V, and hence the p.d. across R_3 is −3.5V and thus I=2.9mA. Therefore the p.d. across R_1 will be −0.78V and hence the NOR output is −1.53V.
● A temperature-compensated regulator package of the form shown left is available as the reference voltage, also frequently on the same chip as the gate structure. This minimizes variation of noise margin with temperature.

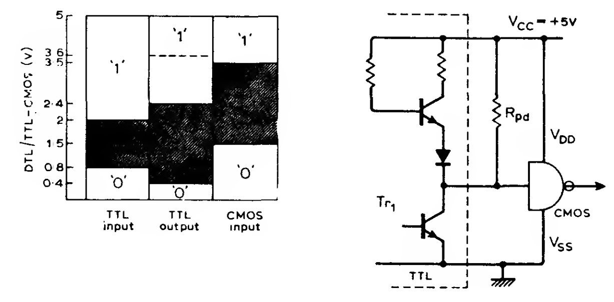
Faster circuits
● Centre circuit shows a type of e.c.l. gate where the reference is at ground potential. With the supplies shown, logic levels nominally −400mV for logical 0 and +400mV for logical 1. Suitable for driving into 50Ω loads, and up to 25mA d.c. when terminated in 50- and 270-Ω pull-down resistor to −3.2V.
Fan-out: 12 (a.c.)
Propagation delay 2 to 3ns
Input level (high) 0.15 to 0.72V
Input level (low) −1.5 to −0.15V
Unused inputs: connect to −1V±50%.
Noise margin: ±200mV.
● Other e.c.l. gates with a basic configuration similar to the first provide multi-input, multi-emitter follower OR/NOR outputs, with optional pull-down resistors.
V_{CC}=0V, V_{EE}= −5.2V±20%
Output (source) current: up to 2.5mA.
Operating temperature range −55 to 125°C
Propagations delay (rising) 3.5 to 5ns
Fall-time propagation delays up to 15ns due to emitter-follower output resistance and capacitance loading.
Three outputs tied together (wired OR) gives output impedance of about 2.5Ω.
Suitable for driving 50-Ω loads (two pull-down resistors only for faster fall times).
Noise margin 175mV
To maintain high speed, limit interconnection length to <25cm
Fan-in: 20; fan-out: 15 (a.c.)
● Basic form of ECL circuit capable of propagation delay <1ns is shown right. A separate supply terminal V_x is used for the output emitter-followers.
V_{EE}: −5.2V. Pull-down resistors of 50 or 2kΩ provide a path for leakage currents (unused inputs can be open-circuit) and act as loads for driving gates. Power dissipation ≈55mW.
Fan-out=70 for R_{pd}=50kΩ.
Fan-out=7 for R_{pd}=2kΩ.
Propagation delay:
0.9ns for 510-Ω load.
1.1ns for 50-Ω load.
Interconnections should be 50-Ω microstrip transmission lines and termination connected to −2V supply.
Temperature range 0 to 75°C.
Logic swing typically −0.9V ("1") to −1.75V ("0").



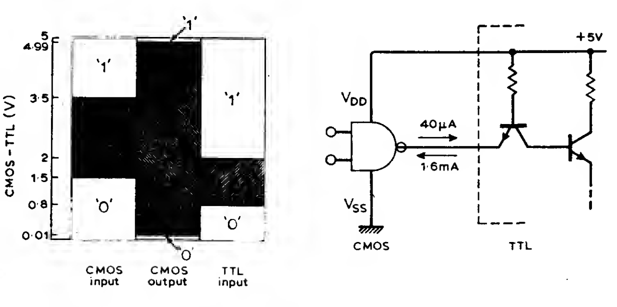




Interfacing

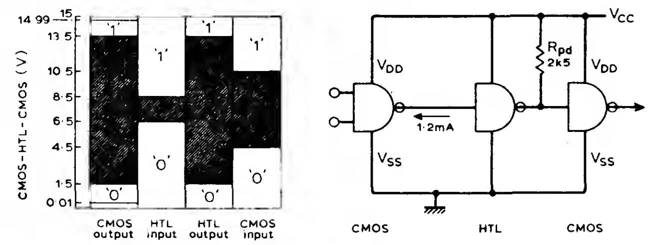


d.t.l./t.t.l.-c.m.o.s.
The minimum t.t.l. 2.4V 1-level output is normally for a load current of 400μA, but as the c.m.o.s. gate input current is approximately 10pA, the more likely 1-output is 3.6V. This is an inadequate noise margin (0.1V) and an active pull-up resistor typically 1 to 10kΩ depending on whether high speed or low power is required) is connected from the t.t.l. output to the positive supply rail of +5V. Hence when Tr_1 is off the c.m.o.s. input will be at +5V giving a 1.4V noise margin. The threshold values of switching for the c.m.o.s. gate is typically 30% and 70% of the supply voltage, i.e. 1.5V and 3.5V respectively.
Note. Unshaded areas represent the 1- and 0-regions, the borders being the minimum 1-level and the maximum 0-level for minimum and maximum t.t.l. supply voltages.

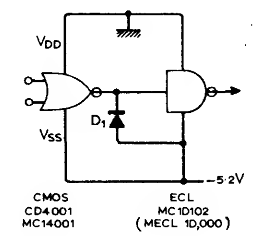


c.m.o.s.-t.t.l.
The c.m.o.s. gate must sink 1.6mA and source 40μA for the 0- and 1-state of the bipolar input respectively. Not all c.m.o.s. devices can cope with one t.t.l. load (1.6mA) but gates on the same package may be paralleled to increase their current sinking capability, or preferably buffers such as CD4009, CD4041, CD4049 should be used. These devices can sink two t.t.l. load currents and still have an output of 0.4V, thus retaining a 0.4V noise margin.

Low-power t.t.l.-c.m.o.s.
Most c.m.o.s. devices can drive low-power t.t.l. directly as the logic zero-level sink-current is 0.18mA. Again for driving c.m.o.s., the t.t.l. output should have a pull-up resistor for adequate noise margin.

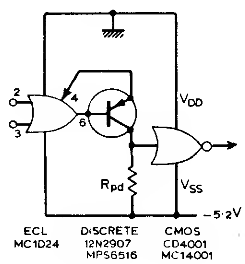


c.m.o.s.-h.t.l.-c.m.o.s.
Most high-threshold logic gates operate from a V_{CC} supply of 15 ±1V. Hence direct connection with c.m.o.s. gates is possible. Noise immunity is high, of the order of 3V for high and low h.t.l. outputs, though this may be improved using a pull-up resistor as shown (in some i.cs this may be internal) which also improves the output rise-time. Rise and fall times of around 1μs should be the aim for the h.t.l.-c.m.o.s. interface.



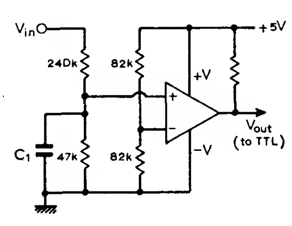
	logic '0'	logic '1'
CMOS output	−5·8V	−0·88V
ECL input	−1·475V	−1·105V

c.m.o.s.-e.c.l.
Both may be operated from −5V ±20%, but speed is restricted to 1MHz. Speed is increased if Vss is taken to a separate supply between −5 and −15V. The clamp diode D_1 keeps e.c.l. drive to a minimum of about −5.8V. Above typical figures indicate a high level noise margin of 225mV, and a low level of 4.3V.



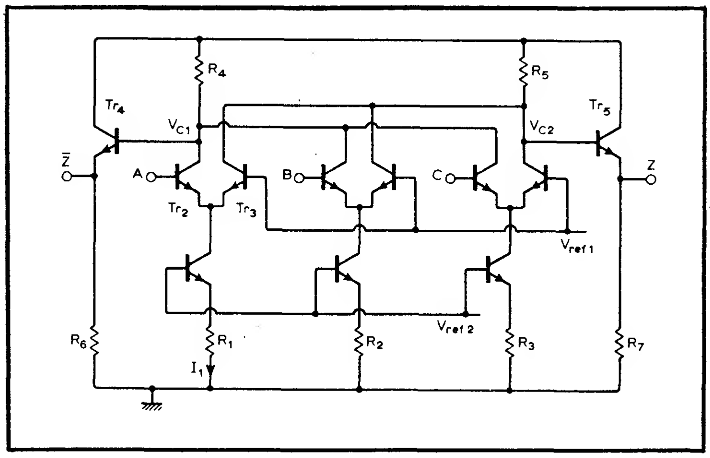
	logic '0'	logic '1'
transistor output	−5·2V	−0·9V
CMOS input	−3·60V	−1·56V

e.c.l.-c.m.o.s.
Output swing of e.c.l. (typically −1.55 to −0.75V) is inadequate to drive c.m.o.s. directly, i.e. switching levels are 30% and 70% of −5.2V. One technique is to use a two-input expandable gate driving a p-n-p transistor, with a pull-down resistor (≈3kΩ) to the negative supply. This provides noise margins amplitudes of 1.56 and 0.66V.



h.t.l.-t.t.l.
Circuit shows a technique for interfacing high level logic to t.t.l. This uses a linear voltage comparator LM311, the component values used allowing an input level range of 0 to 30V. Capacitor C_1 may be added to decrease the effects of fast noise spikes.

Threshold logic



Circuit data

Supply 6V. R_1, R_2, R_3 1.5kΩ. R_4, R_5 560Ω. R_6, R_7 3.3kΩ. V_{ref1} 4.9V, A=B=C=V_{ref1}+100mV. V_{ref2} 1.8V. Sequentially applying A, B & C, Z changes in 0.4V steps from 3.9 to 5.1V. "1"=5.1V (V_{ref1}+200mV), "0"=4.7V or less (V_{ref1}−200mV).

V_{ref1} can be reduced towards V_{ref2} but cannot be increased much beyond 4.90V. R_4 and R_5 can be varied but are generally tied to the values for R_1, R_2 and R_3 (ref. 1) and to the voltage swing required.

Circuit description

Threshold logic gates are much more powerful and flexible than are the normal AND, OR gates. Majority, minority, AND, and OR gates are simply particular cases of threshold logic. A threshold gate has inputs A, B, C .... with weights a, b, c ... associated with the respective inputs. The output Z from such a gate is then:

Z=1 if $<a\mathrm{A}+b\mathrm{B}+c\mathrm{C}+\ldots> \geqslant$ some value T_1, the upper threshold, and Z=0 if $<a\mathrm{A}+b\mathrm{B}+c\mathrm{C}+\ldots> \leqslant$ some value T_2, the lower threshold. $T_1>T_2$ and normal arithmetic addition is involved in the above brackets. The output is more precisely written as:

$Z=<a\mathrm{A}+b\mathrm{B}+c\mathrm{C}+\ldots>_{T1:T2}$

T_1-T_2 is the threshold gap and is that inadmissible sum which will give an ambiguous output. Generally A, B, C, ... are binary (1 or 0); a, b, c ... need not be, but generally are, integers in which case the weighed sum can only take on integral values. The threshold performance is then quoted by those to integers between which switching takes place. We then obtain:

$Z=<a\mathrm{A}+b\mathrm{B}+c\mathrm{C}+\ldots>_{t1:t2}$

where t_1 and t_2 are integers, $t_1-t_2=1$, and $t_1-t_2>T_1-T_2$.

The symbol used is shown (left).

Circuit shows a three-input threshold gate with identical weighting on each input. Basically it comprises three long-tailed pairs with a constant-current source (e.g., Tr_1 and R_1) in each tail. When A exceeds V_{ref1} by 100mV or more the tail current flows through Tr_2 and R_4 and when A is less than V_{ref}, by more than 100mV the current flows through Tr_3 and R_5. Resistors R_4 and R_5 act as summing resistors, summing the currents from the long-tailed pairs. Transistors Tr_4 and Tr_5 act as emitter-follower output stages for V_{C1} and V_{C2} so that $Z=V_{C2}-V_{be}$ and $\bar{Z}=V_{C1}-V_{be}$.

When Z is in the high state it must exceed V_{ref1} by 100mV or more so that a succeeding stage will recognize it as logical 1. Likewise in the low state Z must be less than V_{ref} by 100mV or more.

The following formulae apply to the circuit.

● $I_1=\dfrac{V_{ref2}-V_{BE}}{R_1}$; I_2 and I_3 are obtainable similarly.

● When I_1 is switched from R_5 to R_4 on application of logical 1 at A, then the change in $V_{C2}=I_1R_5$. This change should be around 200mV or more to obtain decisive switching.

● Max $Z=V_{CC}-V_{BE}$ and occurs when no current flows in R_5.

● Min $Z=V_{CC}-V_{BE}-3I_1R_5$. This assumes that all the tail currents are identical and flowing in R_5.

As shown, all three inputs must be applied before Z goes to logical 1. Hence:

$Z=<\mathrm{A}+\mathrm{B}+\mathrm{C}>_{3:2}\equiv Z=$ A.B.C(Boolean). Clearly if any of the inputs is permanently tied to logical 1 we obtain a two-input AND gate. Moreover, if V_{ref1} is dropped to 4.5V only two of the inputs are required to be high for Z to be 1 and hence:

$Z=<\mathrm{A}+\mathrm{B}+\mathrm{C}>_{2:1}\equiv$simple majority gate.

If now C (say) is permanently tied to logical 0 we require the two remaining inputs to be high and we have obtained a two-input AND gate. On the other hand, if C is permanently tied to logical 1 only, one of the remaining inputs requires to be logical 1 for Z to be logical 1 and hence we have obtained a two-input OR gate.

Alteration of R_4 and R_5 is more generally used to alter the threshold[1].

If R_4 and R_5 are different then the outputs from Tr_4 and Tr_5 will not be the logic complement of one another. Any other threshold logic function that one wants can be obtained within the restriction that the weightings will remain the same. Furthermore if, say, R_5 is comprised of a string of series resistors then one can obtain a large number of different functions as well as the basic one[2].

Reference 3 shows how one can improve the tolerance of the circuit to large input voltages which otherwise can cause saturation and incorrect current summation.

Further reading

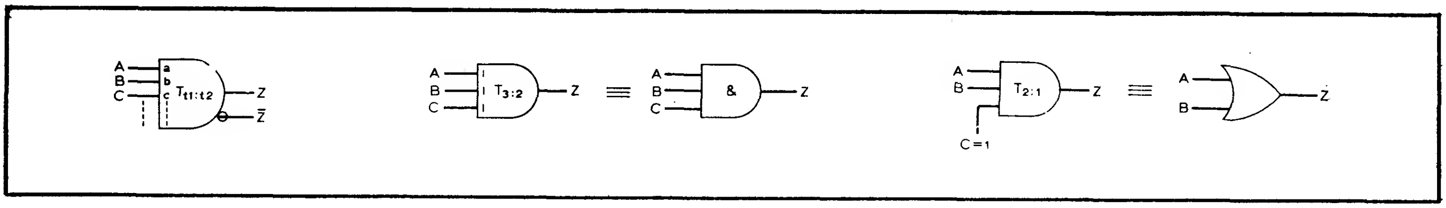
Hurst, S. L. Introduction to threshold logic, *Radio and Electronic Engineer*, 1969, pp. 339–51.

1. Hampel, D. & Winder, R. O. Threshold logic, *IEEE Spectrum*, May 1971, pp. 32–9.

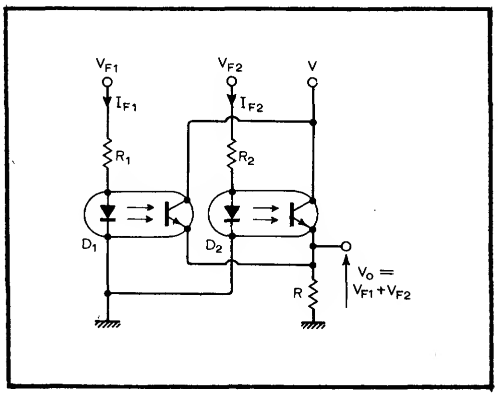
2. Hampel, D. Multifunction threshold gates, *IEEE Trans. on Computers*, vol. C-22, Feb. 1973, pp. 197–203.

3. Hurst, S. L. Improvements in circuit realisation of threshold logic gates, *Electronic Letters*, vol. 9, 1973, p. 123.

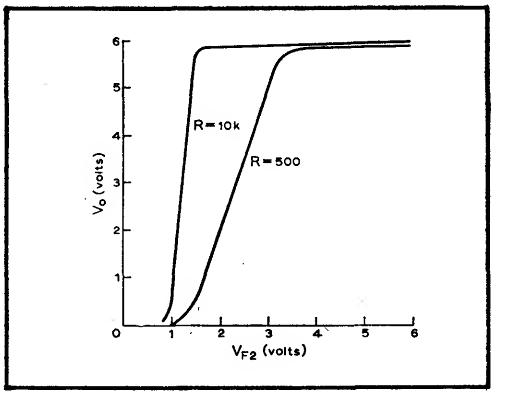
See also card 12.



Optical logic



Performance data
R_1, R_2 100Ω
R 10kΩ and 500Ω
V 6V
V_{F1}=0 and
V_{F2}=0→6V giving
I_{F1}=0 and
I_{F2}=0→50mA
optocouplers TIL112
These figures resulted in graph (right)



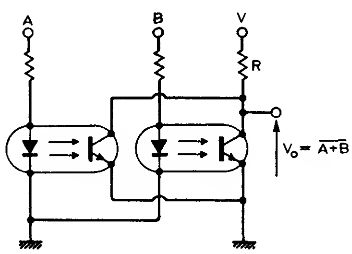
Circuit description
All the simple logic functions can be performed using optical couplers. Fan-out or speed difficulties preclude the use of these gates in complete logic system but in systems where simple logic is required and/or the input is in optical form, they can be very useful and show the usual advantages of optical coupling (cross ref. 1). Circuit shows an OR gate using optical couplers. If V_{F1} is large enough (>1.2V) to make D_1 conduct then Tr_1 conducts and V is applied to R. Similarly V is applied to R if V_{F2} is high and if both V_{F1} and V_{F2} are high. Hence, in Boolean terms, $V_o = V_{F1} + V_{F2}$. The transfer characteristic shown right for two different values of R indicates the static performance and shows noise immunities superior to that of t.t.l. For these two values of R with the given V the photo-transistors are being operated in their saturated mode (cross ref. 1) which permits a maximum current through each transistor of approximately 15mA. The normal parallel type of fan-out is, therefore, only one since the required I_F of succeeding stages is in the range 10 to 50mA. However, serial connection of succeeding stages could yield a fan-out of two or three if the appropriate resistance were chosen. This fan out could be increased if V were increased or, if speed was not essential, by using opto-couplers with Darlington output stages. The fan-in can easily be increased. Note that basically the drive signal is the diode current rather than the applied voltage so that current driving can easily be employed. Moreover V_{F1} and V_{F2} need not be the same, nor indeed do the two diode currents. All that is necessary is that each transistor be driven into saturation. With the quoted data pulse repetition frequencies of 40kHz can be handled. Higher frequencies but with lower current handling capacity can be obtained using photo-diodes and lower frequencies with greater current handling capacity with photo-darlingtons (cross ref. 2).

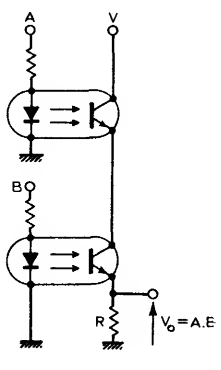
Component changes
V can be increased to 30V.
V_{F1} and R_1 can be varied so long as I_{F1} is in the range 10–50mA. Similarly for V_{F2} and R_2
Optocouplers: ISO-LIT12, MCT26.

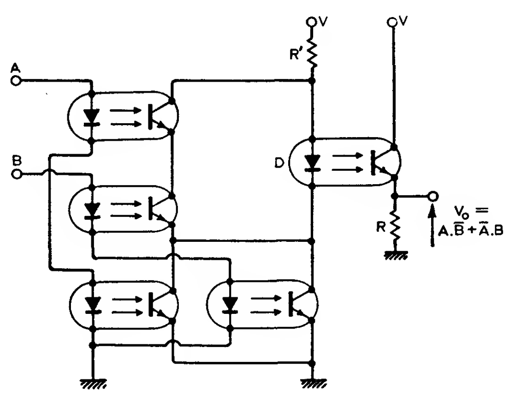
Modifications
- A NOR gate can be constructed as shown left, in which the load R is placed in the positive supply rail.
- An AND gate can be constructed as shown centre. In this case V_o when in the 1-state will be the supply volts minus the sum of the two saturated collector-emitter voltages.
- A NAND gate can be constructed by placing the load R in positive supply line.
- An exclusive-OR gate can be constructed as shown right. Current flows through D and hence in R only when A or B, but not both, are "1". R′ serves to limit the current drawn from the supply when both A and B are "1".
- Negative supply voltages can be used if p-n-p opto-transistors are used.

Cross references
Set 9, cards 8 & 9.

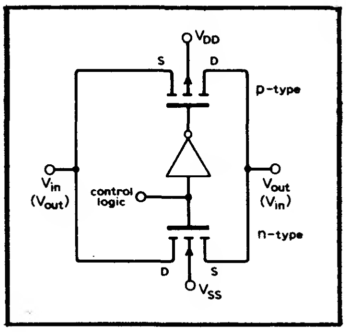
Circuit modifications



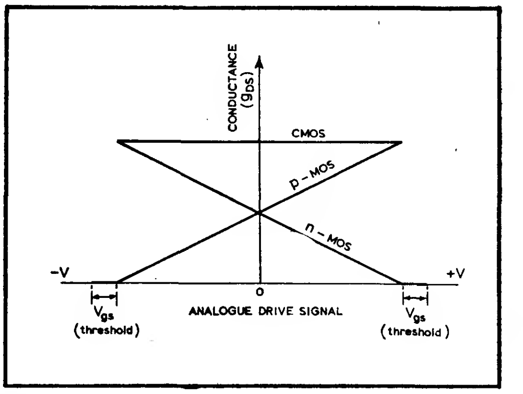




Analogue gates



Typical data
IC: ¼(CD4016AE), ¼(MC14016CL)
Supplies (max): $V_{DD}=+7.5V$, $V_{SS}=-7.5V$
or $V_{DD}=+15V$, $V_{SS}=0$
Input analogue signal range: $\pm 7.5V$ or 15V peak
'on' resistance: 300 to 1kΩ (typical)
'off' resistance: 1000MΩ (typical)
Feedthrough capacitance: 0.2pF
Transfer function linearity: <0.5% distortion into 10kΩ load and $(V_{DD}-V_{SS}) > 10V$
Frequency range: up to 10MHz

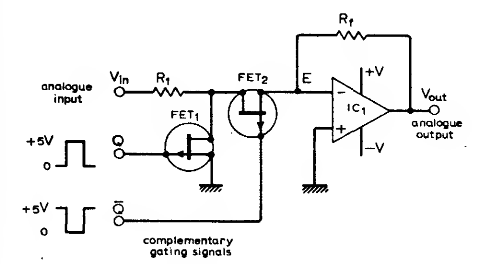


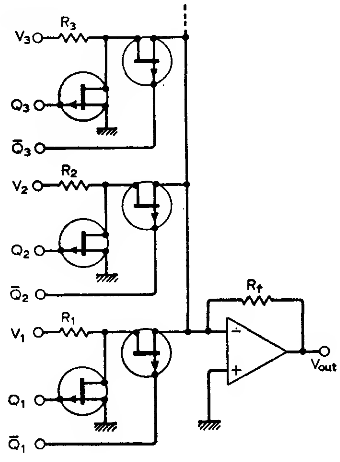
Circuit description
An analogue gate may be considered as an electronic switch which serially connects an analogue signal to a specific input point on the occurrence of a logic or control signal. This is the basis of many multi-channel multiplexers.
One gate that is particularly useful is the c.m.o.s. transmission gate. This comprises a series-pair inverter and two complementary transistors connected in parallel as shown, which allow bi-directional current flow when a control or logic signal is applied to the inverter. High and low signals are applied to the separate gates, and hence both transistors are either on or off simultaneously. The sources and drains of the parallel transistors are tied together, and either terminal may be driven by analogue or digital signals, and the excursion must be within the range of the supply, V_{SS} to V_{DD}.
If the control level is lowered to the V_{SS} rail both transistors are off. This is because the gate-source voltage of the p-type transistor will be zero or positive, and the n-type transistor gate-source voltage either zero or negative for a drive-signal swing limited to $V_{DD}-V_{SS}$. When the control signal is at V_{DD}, both transistors tend to be in the on-state. When the drive signal rises towards V_{DD}, the p-type f.e.t. will conduct harder because its gate-source voltage will increase negatively. At the same time the n-type f.e.t. conductance will begin to fall, as its positive gate-source voltage is decreasing. The resultant effect is for the parallel arrangement to exhibit a fairly constant conductance and hence constant resistance. The graph is an idealized characteristic and assumes first-order linearity of n-m.o.s. and p-m.o.s. device conductance g_{DS} against input voltage, to give a constant g_{DS} for the parallel connection. The actual characteristics exhibit some non-linearity, but the effect on the output-input voltage transfer function is most evident only at low supply voltages (e.g., $V_{DD}=V_{SS}=-2.5V$).

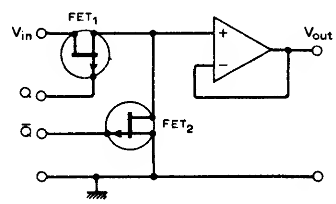
Circuit modifications
● Circuit left is a shunt-series chopper circuit using p-channel junction f.e.ts to gate the analogue signal. The f.e.ts must be fed in antiphase and can be driven from t.t.l. logic provided the f.e.t. pinch-off voltage is less than 4V. When Q is high ($\bar{Q}$ low), Tr_2 is conducting and Tr_1 is off. As Tr_2 is connected to a virtual earth point E, then the signal level at this f.e.t. input is minimum and hence the gate voltage exceeds the sum of the signal voltage and the f.e.t. pinch-off value, a necessary condition for switching. When $\bar{Q}$ is high, Tr_2 is off, and the signal is grounded via the on resistance of Tr_1. The analogue swing is limited by the maximum signal swing of the i.c. amplifier, and the speed of switching will depend on the slew rate of the amplifier.
Tr_1 & Tr_2 2N5461, IC 741 or LM301A, $R_1=R_f=10$ to 33kΩ
The junction f.e.ts may be replaced by p-m.o.s. depletion types with similar pinch-off.
● Further, similar, chopper circuits may be connected to the virtual earth point to provide a signal multiplexer (middle). Signals V_1, V_2 and V_3 can be gated in turn by applying complementary control signals to the $\bar{Q}$, Q terminals in sequence, say from a ring-counter.
● The arrangement right, a series-shunt chopper, is best suited to voltage sources as neither the op-amp or Tr_2 draws significant current when Tr_1 is on, or when Tr_1 is off. The current from the source is negligible. Hence the input signal is gated to the op-amp with almost zero attenuation.

Further reading
CD4016A Data Sheet, RCA Solid State Databook Series SSD 203A.
Johnson, P. A. Complementary m.o.s. integrated circuits, *Wireless World*, vol. 79, August 1973, pp. 395–400.
Givens, S. FETs as analog switches, *Electronic Components*, 26 January, 1973.
Honey, F. J. DTL/TTL controls large signals in commutator, *Electronics*, March 1970, p. 90.
Jenkins, J. O. M. Interface circuits drive high-level switches from low-level inputs, *Electronic Engineering*, May 1971.

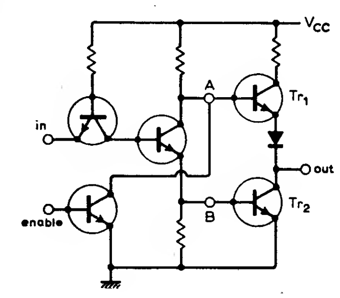
Circuit modifications







Three-state and majority logic



IN	ENABLE	OUT	
0	0	1	on states
1	0	0	
0	1	Hi-Z	off states
1	1	Hi-Z	

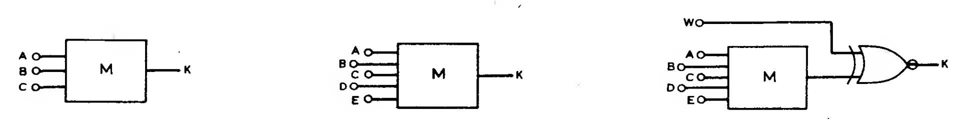
Three-state gates
Three-state logic (t.s.l.) is now available from at least three companies: National Semiconductor, Texas Instruments and Signetics. Flip-flops, multiplexers, demultiplexers, line drivers, counters and r.o.ms are among the devices available in this form. The three states are normal 1 and 0 levels plus an off state which represents a high impedance condition in which the gate can neither sink nor source current—effectively an open circuit. Referring to the diagram, if the enable signal is logical 0 then normal logic inversion of the input signal is performed. However, if the enable signal is logical 1, then the input signals are overridden and the device goes into its hi-Z or off state as point A and with it point B are grounded. Hence, both Tr_1 and Tr_2 are switched off and present a high impedance to the load. This means, for example, that a large number of gates can be connected by means of a bus to a single load, only one gate at a time being connected to the load, all others being in the hi-Z state. If the number of gates connected to the bus is high then the leakage current (typically 40μA) of the off devices must be taken into account as the single on-device is supplying the load plus the leakage of all the off-devices. For this reason t.s.l. gates normally have a Darlington-connected upper output stage and this increases the source current capability by an order of magnitude over that for normal t.t.l. This in itself is an advantage of t.s.l. which in addition has the usual advantages of t.t.l. with respect to other logic families. The increased source current capability also carries with it a much reduced one-level output impedance which gives a one-level noise immunity an order of magnitude better than that for t.t.l.
To ensure in a bus-organized system that no two devices are ever on at the same time, all t.s.l. devices are arranged such that the time delay from on to off is less than that from off to on. Nevertheless, overlaps can occur and although no damage is done to the devices transients resulting from this or any other source can be longer than in a t.t.l. system, principally because more gates will probably be connected to the output of a t.s.l. device and this gives rise to increased load capacitance. Note that all t.s.l. devices are fully t.t.l. compatible and that three-state buffer gates are available to convert any d.t.l. or t.t.l. device into a t.s.l. element.

Further reading
Calebotta, S. *Electronic Design*, vol. 20, no. 14, 6 July 1972, pp. 70–2.
National Semiconductor, Digital Integrated Circuits Data Book.

Majority logic gates
A majority logic gate is a form of threshold logic gate where the numerical "weight" assigned to each of its inputs is unity. Majority logic uses combinational gates that provide an output in the 1-state (true) only when more than half of the inputs are in the 1-state. To realize this requirement when the number of inputs in the 1-state exceeds the number of inputs in the 0-state by only one (an input majority of one), majority gates normally have an odd number of inputs.
It has only recently become possible to design systems based on standard integrated-circuit packages employing majority logic. These packages are of the 16-pin dual-in-line type and contain two identical majority logic gates, each having five inputs and using c.m.o.s. technology. Such majority logic gates allow the design of certain functions, such as those required for communication in the presence of noise and correlation methods, that are difficult to implement with other types of gate.
The flexibility of the majority gate can be seen by comparison with the normal AND, OR, NAND and NOR gates which select one input combination from a possible 2^n combinations of n inputs, whereas the majority gate can select 2^{n-1} of the 2^n inputs. A majority gate with only three inputs is possible, as shown left, having an output function $K=AB+AC+BC$ and, on inversion, this can produce the NOR majority function $K=\overline{AB+AC+BC}$.
The output function of the 5-input majority gate, shown centre, is more complex and is: $K=ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE$.
By feeding this function to an exclusive-NOR gate together with another function, that may be at logical 0 or logical 1, further flexibility is introduced. When the W-input is at logical 1 (right) K provides the above 5-input majority logic function, $K=M5$ (say), and when $W=0$ inversion occurs making $K=\overline{M5}$. With $D=1$ and $E=0$, K provides the majority of the three inputs A, B and C when $W=1$ ($K=M3$) and the NOT majority function $K=\overline{M3}$ when $W=0$. With $D=E=1$, K provides the three-input OR function when $W=1$ and the three-input NOR function when $W=0$. With $D=E=0$, the three-input AND function is realized when $W=1$ and this becomes the three-input NAND function when $W=0$.

Further reading
Garrett, L., C-MOS may help majority logic with designers' vote. *Electronics*, vol. 46, no. 15, 19 July 1973, pp. 107–12.

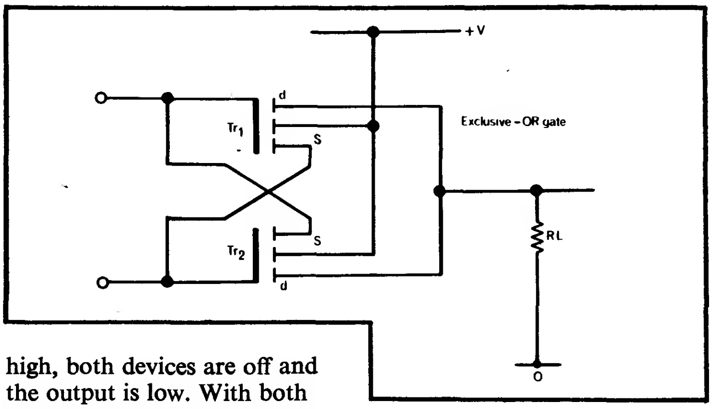
Cross references
Set 11, cards 5, 6 & 9.



wireless world circard

Set 11: Basic Logic Gates Up-date

1. A novel form of logic gate has been proposed recently that allows relatively complex logic functions to be constructed using a small number of components. They are compatible with existing i.c. processes and can be implemented using devices from standard i.cs. No power gain is available as the active devices are used as series switches, i.e. cascaded gates suffer from loss of signal level as with earlier diode gating systems. In the example shown, two p.m.o.s. enhancement-mode transistors are used. With both inputs



high, both devices are off and the output is low. With both inputs low, the devices are off because again each device has $V_{gs}=0$. Only if one input is high and the other low is one device put into a conducting state is the output taken high. The symmetrical nature of the circuit shows that it does not matter which is taken high, e.g. if A is high and B low, then Tr_2 conducts raising the output close to A (the difference depending on the on-resistance of Tr_2 compared with R_L). The circuit thus implements the exclusive-OR function, and the reference describes other arrangements both m.o.s. and bipolar for producing logic functions with fewer-than-normal components.

Reference

Edwards, C. R. Some novel exclusive-or/NOR circuits, *Electronics Letters*, 1975, 11, pp. 3/4.

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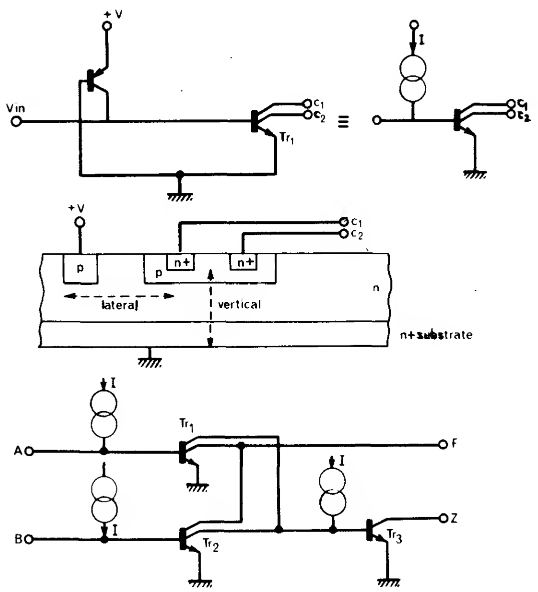
2. Integrated injection logic I^2L has the lowest speed-power product of presently available gates (1975), and a much higher packing density. The structure is such that the n-p-n transistor Tr_1 is vertical and the lateral p-n-p transistor serves as both a current source and as an active load. Tr_1 has multiple collectors c_1 and c_2. With the input of the I^2L gate high (or floating, corresponding to the previous gates being off), then Tr_1 is biased on by the p-n-p current source. Then its outputs are capable of sinking the currents from the current sources at the inputs of the gates to which they are connected.



If V_{in} <700mV, the injected current will be diverted through the low output of the driving gate; hence no base current to p-n-p transistor and the collectors will depend on potential to which they are connected. The OR/NOR gate shown provides $F=\overline{(A+B)}$ and $Z=(A+B)$. If either input A or B is high, Tr_1 or Tr_2 conducts and F is low. Also, as then the wired-OR connection to the base of Tr_3 is low, Tr_3 is off, and Z tends to be high. Note that I^2L input/output connections are not connected directly to the package pins, but via appropriate buffer networks.

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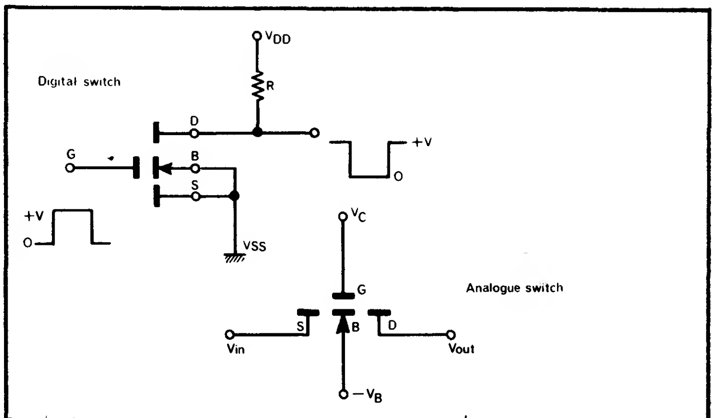
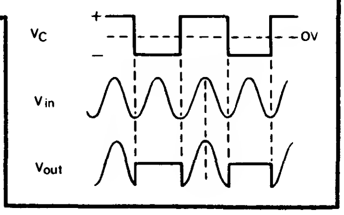
3. D.m.o.s. transistors are double-diffused metal-oxide devices, in which the channel length L of this n-type enhancement type can be controlled very accurately during production. Since R_{on} on-resistance, and input capacitance are proportional to L, while g_m and cut-off frequency are proportional to $1/L$ and $1/L^2$ respectively, then these devices provide better performance than conventional n-type f.e.ts. Digital and analogue switch configuration are shown.

For the digital switch, $(V_{DD} - V_{SS})$ can go up to +30V. With an input signal at V_{in},

$$V_{out}=\left(\frac{R_{on}}{R+R_{on}}\right)V_{DD}$$





This is the low level of V_{out} and is controllable by varying R. The following table shows the rise-time, and delay between input and output in nanoseconds.

V_{DD}	$R(k\Omega)$	t_r	t_d
5	0.68	0.7	0.6
10	0.68	0.8	0.7
15	1.0	1.0	0.9

The threshold voltage at which the transistor turns on is dependent on V_B when source and substrate are not connected as in the analogue switch application, and may have to be accounted for to avoid shift in operating point. The input signal is transmitted through the analogue switch when V_C > (most positive peak of V_{in}) and is disconnected when V_C < (most negative peak of V_{in}).

Reference

Theory and applications of DMOS, *Electronic Industry*, December 1975.