Lab Notes

Walking rings . . . and other miracles

A common task facing the electronics designer is that of producing simple digital counter/divider networks which produce an output frequency or count rate that is some fixed fraction of an input frequency or count rate. Here's how to do it.

Ray Marston

DIGITAL DIVISION, or counting, is a fairly straightforward task – providing you know how (!), chiefly involving the manipulation of circuit 'blocks' to economically or conveniently do the task required. But, as the old saying goes, there's more than one way to skin a cat . . .*

4013 and 4027 flip-flops

The two most basic counter/divider ICs in the CMOS range are the 4013 dual D-type flip-flop and the 4027 dual J-K flip-flop. Figure 1 shows the outlines and pin notations of these two devices, which each contain two independent flip-flop stages sharing common supply connections. Each of these packages can be used to give division ratios or 2, 3 or 4.

A single 4013 'D' stage can be made to act as a divide-by-two counter by grounding its SET and RESET pins and coupling its DATA pin to its $\overline{Q}$ output, as shown in Figure 2a. A single 4027 J-K stage can be made to act as a divide-by-two counter by grounding its SET and RESET pins and connecting its J and K pins to the positive supply rail, as shown in Figure 2b. Both of these circuits change state on the positive-going transition of the input clock signal, which must have rise and fall times of less than 5 us. The 4013 is very fussy about the shape of its input clock signals and tends to be rather temperamental in operation. The 4027 is not too fussy about its clock signals and is very easy to work with.

Ripple counters

Figure 3 shows how two divide-by-two 'D' or J-K flip-flop stages can be wired in series to give an overall division ratio of four (2^2). Figure 4 shows how three

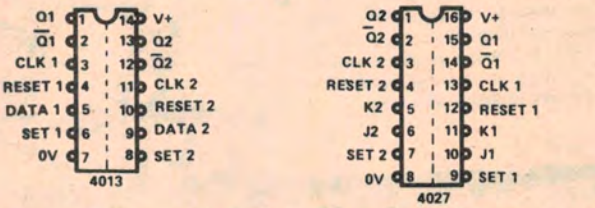


Figure 1. **Outlines and pin notations for the versatile 4013 dual-D and 4027 dual J-K CMOS flip-flop ICs.**

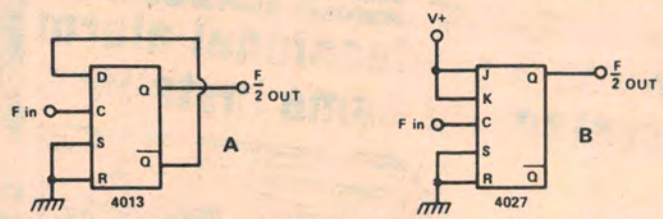
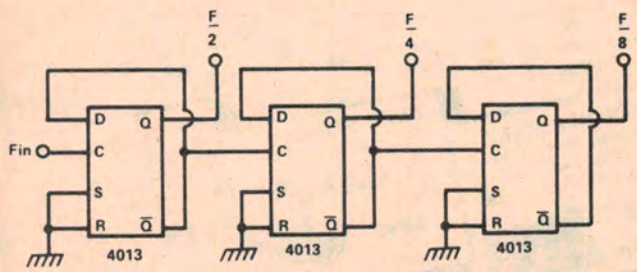


Figure 2. **Divide-by-two counters made from D-type (left) and J-K (right) flip-flops.**



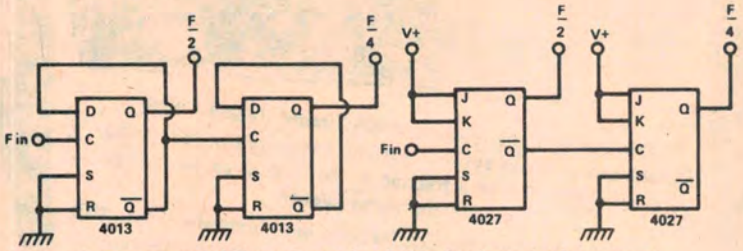


Figure 3. **D-type and J-K versions of a divide- by-four ripple counter**

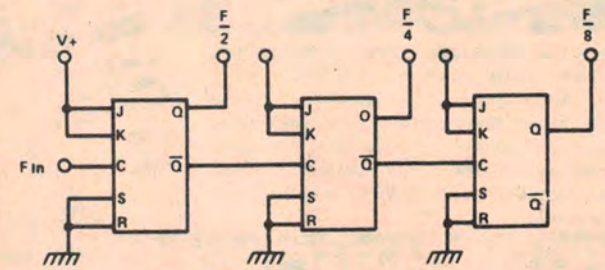


Figure 4. **Two versions of a divide-by-eight ripple counter using D-type (top) and J-K (bottom) flip-flops.**

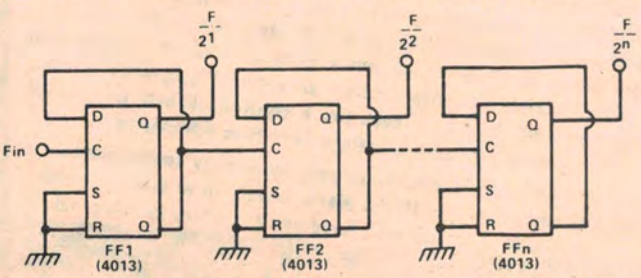


Figure 5. **How a chain of D-type flip-flops can be linked to provide a divide-by-2 ripple counter.**

*(Uh, sorry . . . no offence to cat lovers)

An occasional series in which we discuss interesting circuit techniques, circuits we have tried in our own laboratory but not developed as a project, practical notes on projects, measurement techniques for hobbyists etc.

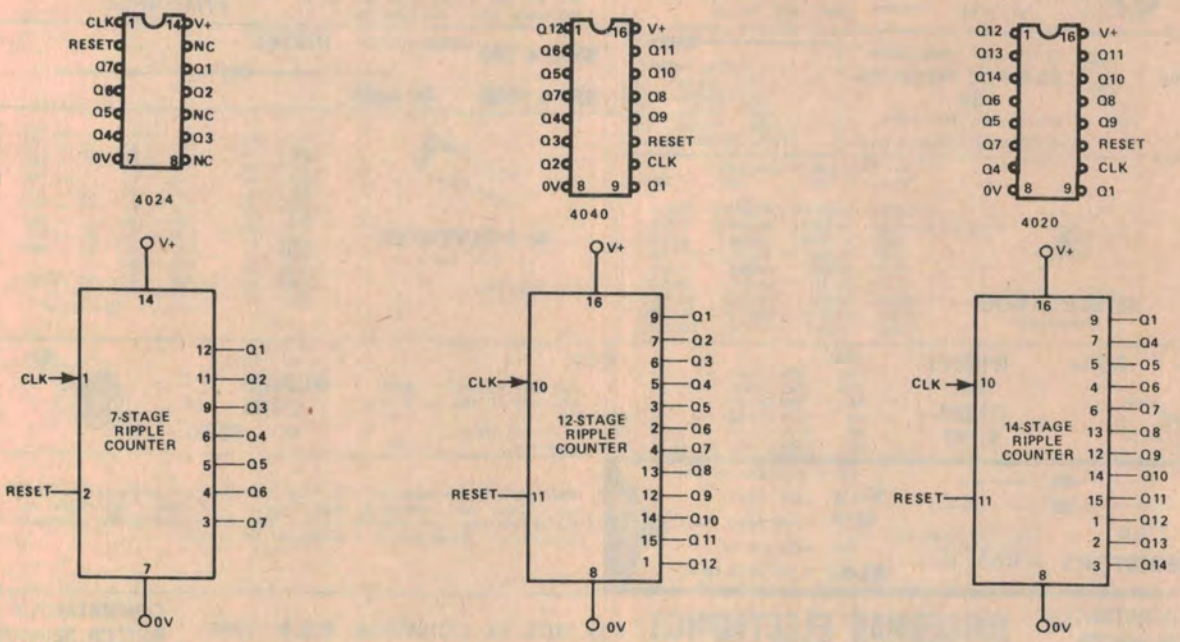


Figure 6. **Outlines (above) and functional diagrams (below) of three popular CMOS multi-stage ripple counter ICs.**

such stages can be wired in series to give a division ratio of eight (2^3). Note that each counter stage is clocked at precisely half the rate (an octave below) of the preceeding stage, so that the clock signal seems to 'ripple' through the counter chain. Also note that, as is made clear in Figure 5, the final division ratio is equal to 2^n where 'n' is the number of counter stages. Thus, four stages give a ratio of $2^4 = 16$, five stages give $2^5 = 32$, six give $2^6 = 64$, seven = 128 and so on.

A detail not made clear in the above diagram is that, since the counters of a 'ripple' circuit are effectively wired in series, the propogation delays of the individual stages in the counting chain add together to give a fairly long total delay at the end of the chain. If each stage has a delay or 100 ns and there are ten stages, the total propagation delay is 1 us. Consequently, the first output signal will not change state until 1 us after the arrival of the original input clock signal that initiates that change of state. The counter states of the 'ripple' type of counter are thus not in perfect synchrony with the original clock signal and this type of circuit is consequently known as an asynchronous counter.

The 4013 and 4027 counters can be cascaded to give any desired number of ripple stages. When more than two stages are required it is usually economic, however, to use a special-purpose MSI ripple-carry binary counter/divider IC. Figure 6 shows the outlines and functional diagrams of three popular ICs of this type.

The 4024 is a seven-stage ripple unit with all seven outputs externally accessible. It gives a maximum division ratio of 4096. The 4020 is a fourteen-stage unit with all outputs except 2 and 3 externally accessible; and it gives a maximum division ratio of 16 384.

Figure 7 shows the outline and functional diagram of a special-purpose ripple-carry unit, the 4060. This is another fourteen-stage unit, but does not have outputs 1, 2, 3 or 11 externally accessible. The special feature of the 4060 is that it incorporates a built-in clock oscillator circuit. The diagram shows the connections for using the internal circuit as either a crystal or an RC oscillator.

The 4020, 4024, 4040 and 4060 ICs ▶

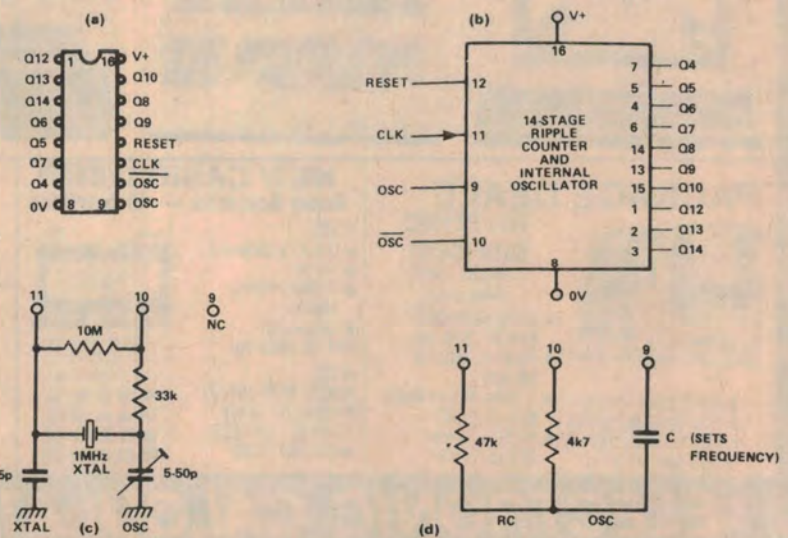


Figure 7. **Outline (a), functional diagram (b) and alternative oscillator connections (c and d) for the 4060 fourteen-stage ripple counter.**

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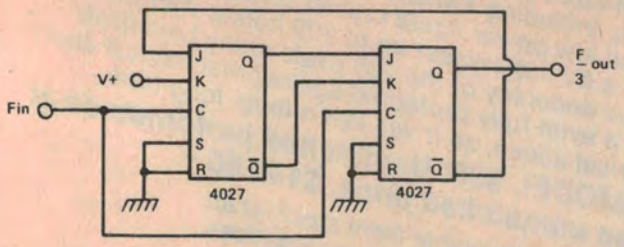

Figure 8. **A divide-by-three 'walking ring' or 'Johnson' counter using J-K flip-flops.**

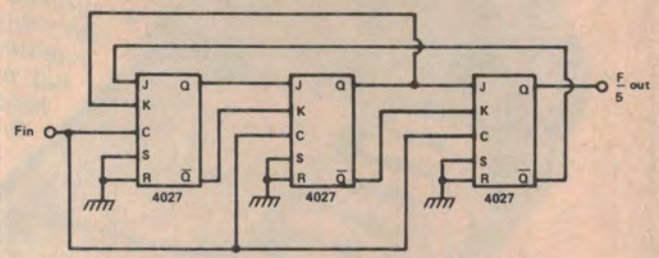

Figure 9. **A divide-by-five Johnson counter using J-K blocks.**

are all provided with Schmitt trigger action on their input terminals and trigger on the negative transition of each input pulse. All counters can be set to zero by applying a high level on the RESET line.

'Walking ring' or 'Johnson' counters

An alternative to the ripple type of counter is the so-called 'walking ring' or 'Johnson' counter. In these counters, all stages are clocked in parallel and the stages are cross-coupled so that the response of one stage to a clock pulse depends on the states of the other stages.

Figure 8 shows the connections for making a divide-by-three counter from two J-K stages and Figure 9 shows the connections for making a divide-by-five counter.

A major advantage of the 'walking ring' or 'Johnson' counter is that, since all stages are clocked in parallel, the outputs of the completed counter are subjected to only a single stage or propagation delay. Consequently, the system gives synchronous operation and outputs give glitch-free decoding.

4018 divide-by-n counter

When count numbers greater than four are required, it is economic to use MSI ICs such as the 4018, rather than the 4013 or 4027. The 4018 is a five-stage 'Johnson' counter that can be made to divide by 2, 3, 4, 5, 6, 7, 8, 9 or 10 by merely cross-coupling its terminals in suitable ways. The IC features a Schmitt trigger on its clock input line and clocks on the positive transition of the input signal.

Figure 10 shows the outline and functional diagram of the 4018. Figure 11 gives methods of cross-coupling the IC to give division ratios from two to ten. On even division ratios, no additional components are needed. On odd ratios, a two-input AND gate is required in the feedback network. This gate can be a single 4081 AND stage, or can be made from two 4011 NAND stages.

Greater-than-10 division

Even division ratios greater than ten can usually be obtained by simply cascading suitably scaled counter stages, as shown in Figure 12. Thus, a divide-by-two and a divide-by-six stage give a ratio of twelve, a divide-by-six and a divide-by-six give a ratio of 36 and so on.

Non-standard and uneven division ratios are obtained by using standard counters, such as the 4018, and decoding their outputs to generate suitable counter-reset pulses on completion of the desired count. ●

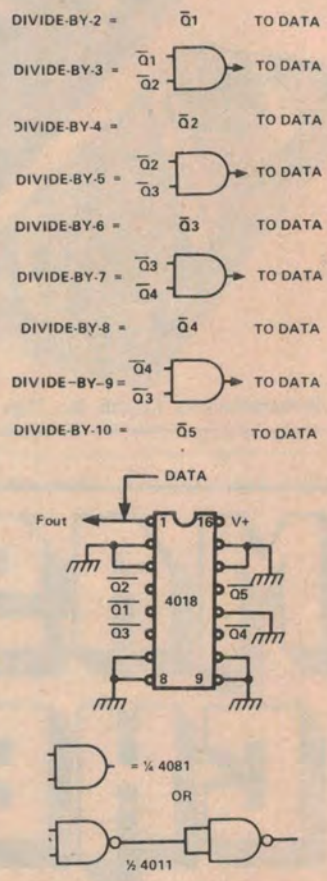

Figure 11. **Methods of connecting the 4018 for divide-by-two to divide-by-ten operation.**

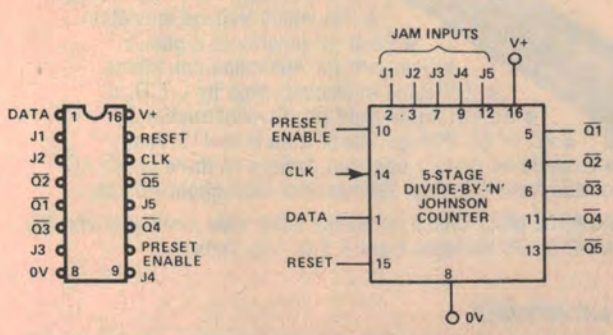

Figure 10. **Outline and functional diagram of the 4018 presettable divide-by-n counter.**

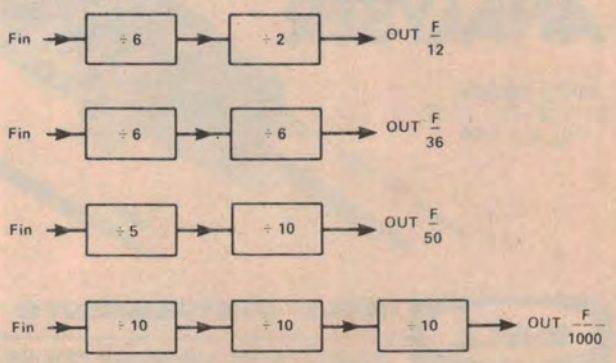

Figure 12. **Typical examples of division by numbers greater than ten.**