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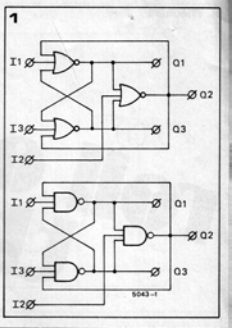
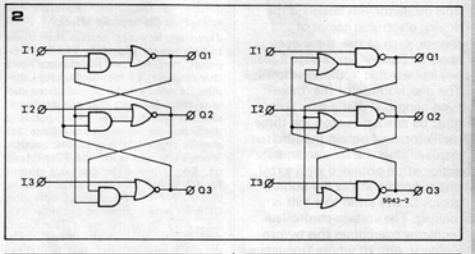
tri-stable



It is possible to use two NAND or NOR gates to make up a flipflop - a circuit with two stable conditions. The process can be extended to obtain circuits with three or even more stable states.



The arrangements shown in figure 1 both have 3 stable states. The state taken up by the outputs will depend on the input conditions applied. These circuits have the objection that correct operation is only guaranteed when drive is applied to two of the inputs at once (see table 1).

It is however possible to modify the circuits so that a single input drive will produce the desired output state. The circuit as a whole becomes more extensive; but it becomes easier to use. Figure 2 shows the modified arrangement. The operation of this circuit can be followed from table 2.

Figure 3 shows a master-slave shift register. If C is at logic '1', then the OR-gate outputs will also be '1', so that the state of Q_1-Q_2-Q_3 does not change. If C becomes '0', the AND-gate outputs will also be '0', so that the state of Q_4-Q_5-Q_6 is held.

Suppose for example that C is logic '0', with I_1 = '0', I_2 = '0' and I_3 = '1'. We find that Q_1 = '1', Q_2 = '1' and Q_3 = '0'. Since C is '0' the state of Q_4-Q_5-Q_6 is maintained. If C now goes to '1', the outputs Q_1, Q_2 and Q_3 will not change.

This state is also the state at the inputs I_4, I_5 and I_6. Q_4 therefore becomes '0', Q_5 also '0' and Q_6 '1'. This shows that the input information '0'-'0'-'1' appears, after one clock pulse, at the output.

NOR gates

I_1	I_2	I_3	Q_1	Q_2	Q_3
0	0	0	x	x	x
1	1	0	0	0	1
1	0	1	0	1	0
0	1	1	1	0	0
1	1	1	0	0	0

NAND gates

I_1	I_2	I_3	Q_1	Q_2	Q_3
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
1	0	0	0	1	1
1	1	1	x	x	x

Table 1

NOR gates

I_1	I_2	I_3	Q_1	Q_2	Q_3
0	0	0	x	x	x
1	0	0	0	1	1
0	1	0	1	0	1
0	0	1	1	1	0
1	1	1	0	0	0

NAND gates

I_1	I_2	I_3	Q_1	Q_2	Q_3
0	0	0	1	1	1
0	1	1	1	0	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	x	x	x

Table 2