Engineer's notebook

Back-and-forth scanner overcomes slewing-rate limits

by James A. Blackburn
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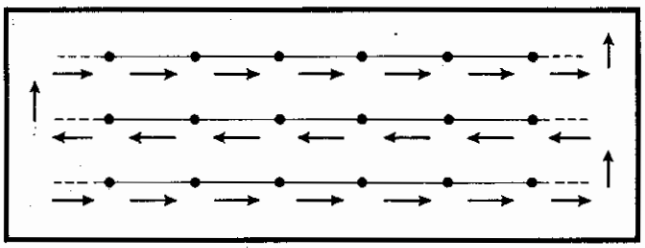
An incremental plotter or line printer that can store entire lines in a buffer memory can be made to print the lines alternately forwards—from left to right—and backwards—from right to left. This refinement will significantly increase its speed because it will no longer need the carriage return function with its all-too-finite slewing rate. In fact, only the minimum character-to-character print rate will then be affected by the mechanical inertia of the print-head assembly (or, in the case of an all-electronic display system, by the finite settling time of the amplifiers).



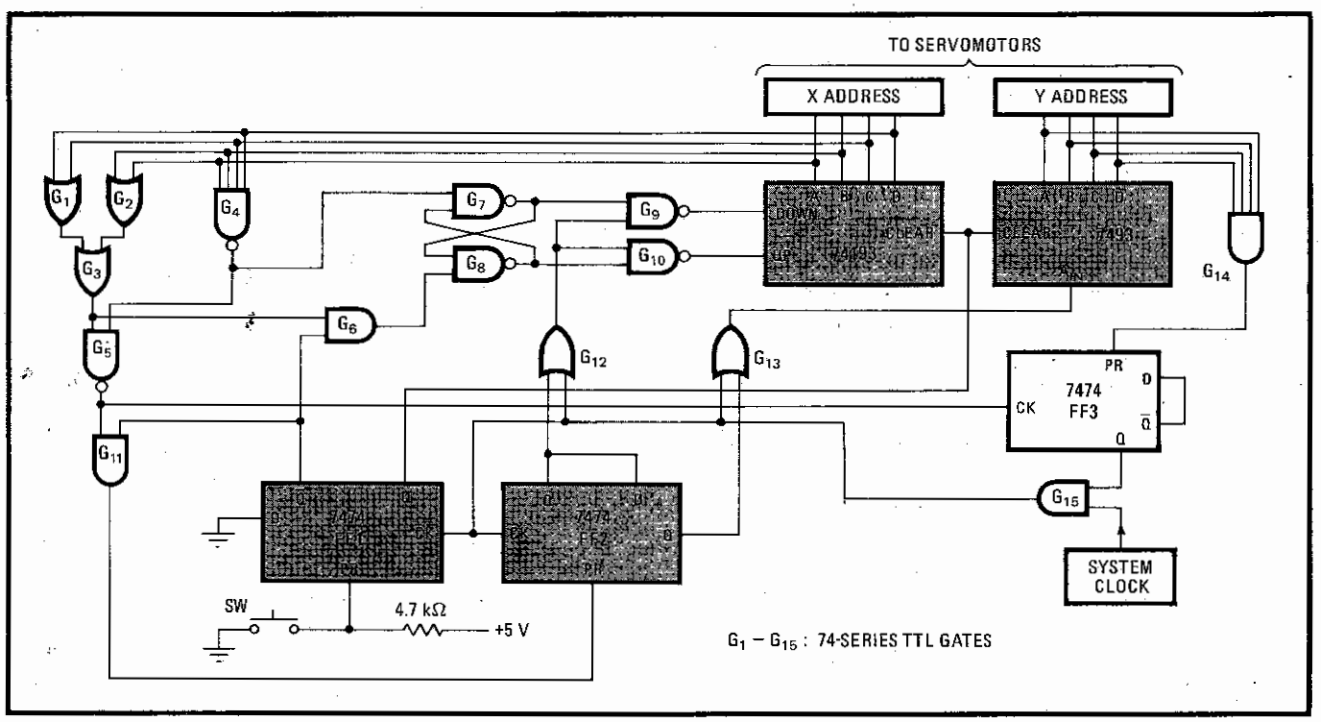
1. Zig-zag scan. Two-dimensional scan in minimum time is achieved by reversing scan direction on alternate rows, as indicated here. Initial address (0,0) is at lower left, and scan halts at (15,15).

The technique is applicable to all two-dimensional scanning that must be performed incrementally. However, it is particularly efficient when each horizontal line contains many points, because in such cases the dead time during carriage return is proportionately large.

The circuit described here generates the required address sequences. It was designed as part of a rapid-film-scanning densitometer. The X and Y addresses can be sent via digital-to-analog converters to a servo system for incrementally moving the film holder past a photodetector. Alternatively, the vertical and horizontal count pulses may be used directly to drive stepping motors. If an appropriate clock frequency is chosen, the film may be scanned in the minimum time compatible with motor torque, sample stage inertia, and step size. A digitized replica of the image on the film may then be obtained by logging the densitometer output at each selected address.

The circuit shown in Fig. 2 performs an alternating-direction scan with TTL integrated circuits exclusively and is thus capable of high-speed performance. The clock frequency would normally be selected so that it is optimum for incremental motion in the X direction. In the example presented here a 16-by-16-address grid is employed. Other choices would be relatively easy to implement by cascading counters and/or changing the max-min address testing.

Briefly, the circuit functions as follows. Switch SW is



2. Scan-control logic. Logic circuit for alternating-direction incremental scanner uses 74-series TTL gates, flip-flops, and counters. Flip-flops are triggered by rising pulse edges, and counters by falling edges. Count pulses could drive stepping-motor controllers directly.

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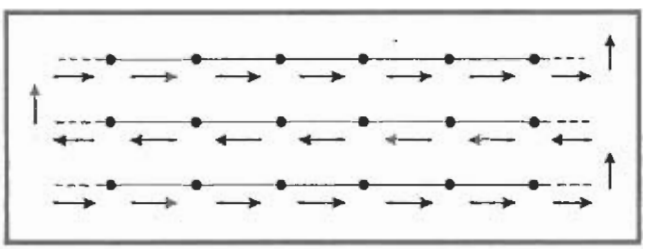

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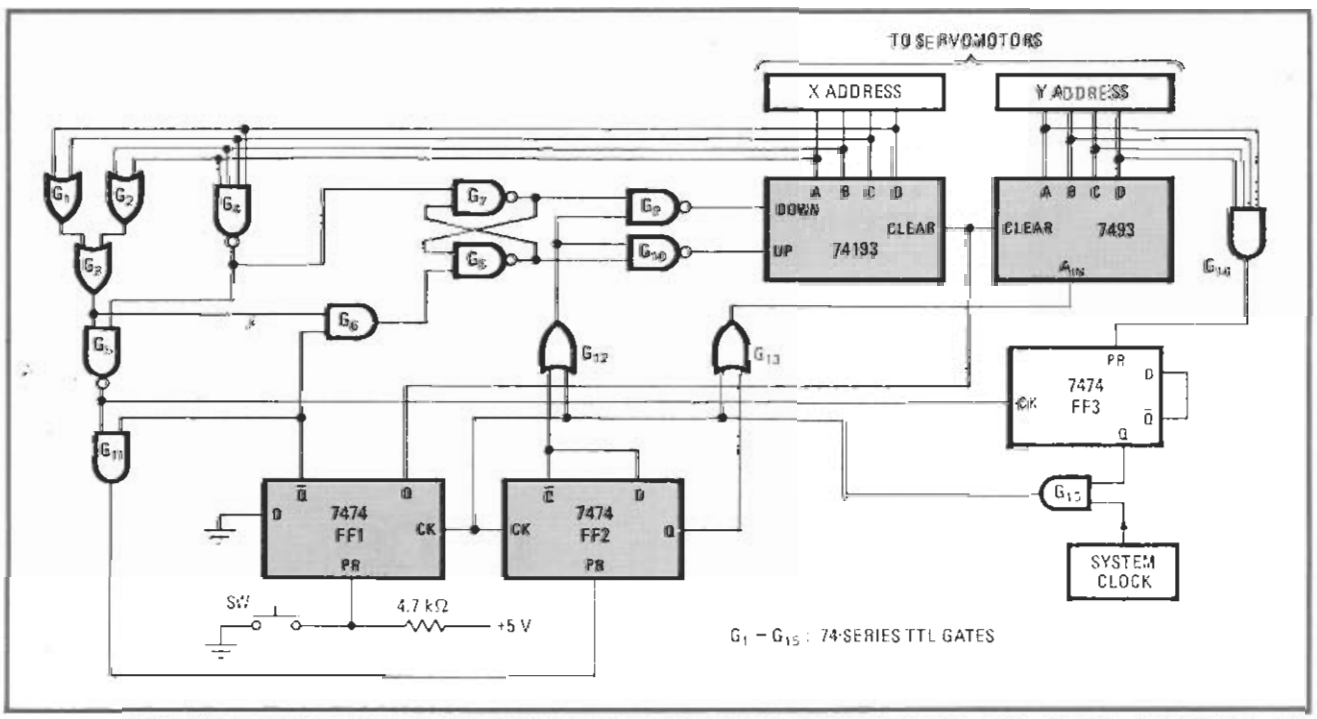

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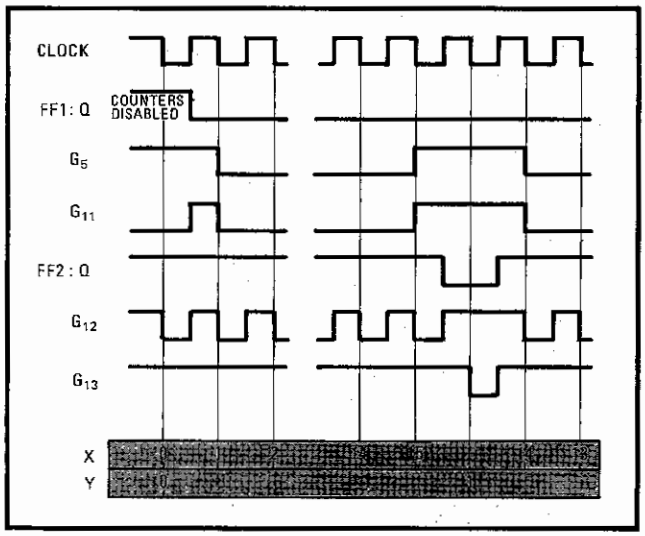
depressed. This sets all counters to zero, presets the three D-type positive-edge-triggered flip-flops (7474), and initializes the R-S flip-flop composed of gates G_7 and G_8. Note that the output of G_{14} is low; therefore clock pulses are passed freely through G_{15}. The first rising edge on the clock stream to occur after SW is released triggers flip-flop FF_1, thus enabling the X and Y counters and G_6. Gate G_{11} is now irreversibly enabled so that the end-of-line test performed by gates G_1–G_4 directly controls the PRESET function of FF_2.

As can be seen in the timing diagram (Fig. 3), the output of G_{11} rises for a half cycle because G_5 is initially high. However, the clock pulse has preceded this event by an interval equal to the propagation delay of FF_1. Therefore FF_2 does not toggle, and its Q output remains at logic 1.

Subsequent negative clock edges are passed through G_{12} and G_{10}, causing the X address to increment steadily. The timing diagram indicates the sequence of events as the end of the first line is reached. A final negative clock edge causes a count of 15 to be achieved. The output of G_4 immediately goes low, toggling G_7/G_8. As a result G_9 is enabled and G_{10} disabled, while the outputs of G_5 and G_{11} rise, enabling FF_2. A half cycle later, the rising clock-edge toggles FF_2, enabling G_{13} and disabling G_{12}. The next falling edge increments the Y address without affecting the X counter. Following this a positive edge again toggles FF_2, this time closing G_{13} but opening G_{12}. The X address now will decrement steadily until a zero count is reached, when a similar logical sequence will route a clock pulse to Y and prepare G_7/G_8 for upcounting. (Note that FF_2 can be toggled by the clock pulses only when the output of G_5 is high—that is, when either a minimum or maximum X address is obtained.)



3. Pulse sequences. Timing diagram shows output states of selected gates and flip-flops in circuit that produces back-and-forth scanning, and the X and Y addresses that control servomotors.

When the fifteenth Y increment occurs, G_{14} goes high and enables FF_3. From the timing diagram it can be seen that G_5 will already be high at this moment. FF_3 does not change state until the next rising edge is applied to its clock input, at the completion of the last horizontal scan. A final falling clock edge causes G_5 to go high, toggling FF_3 and disabling G_{15} so that no further clock pulses reach the rest of the circuit. The X and Y addresses are thus frozen at this terminal count.

Once SW is released, the entire scan proceeds automatically and halts at the final address. Logging an entire image therefore requires no attention from the operator. □