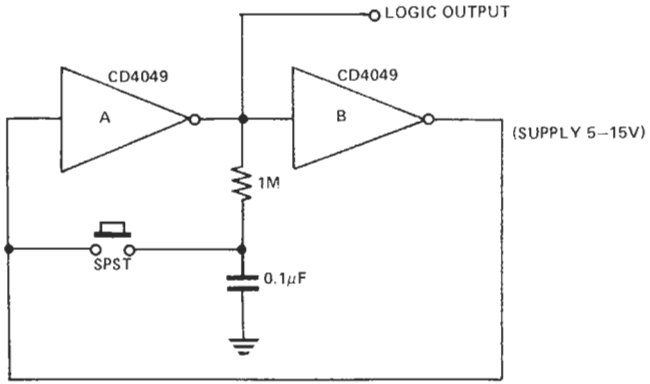
SPST SWITCH FLIP FLOP

The circuit gives latching on-off action with a single SPST switch, utilizing the high input impedance property of CMOS logic.

It can be seen that C will go to the logic state opposite to that existing at the input to inverter A. On closing the contact, the input to inverter A is taken to the opposite logic state momentarily and the latch flips.

The RC time constant of about 100 milliseconds provides sufficient protection from switch bounce yet gives quick recovery for the next operation. The output may drive other logic gates or external loads through buffer circuits.



65

positive-triggered set-reset flip-flop using inverters

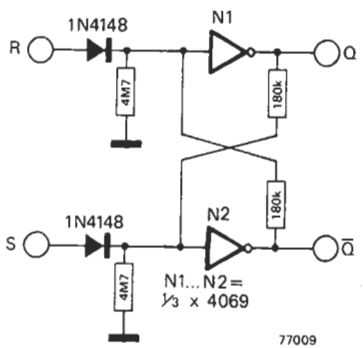
elektor july/august 1977

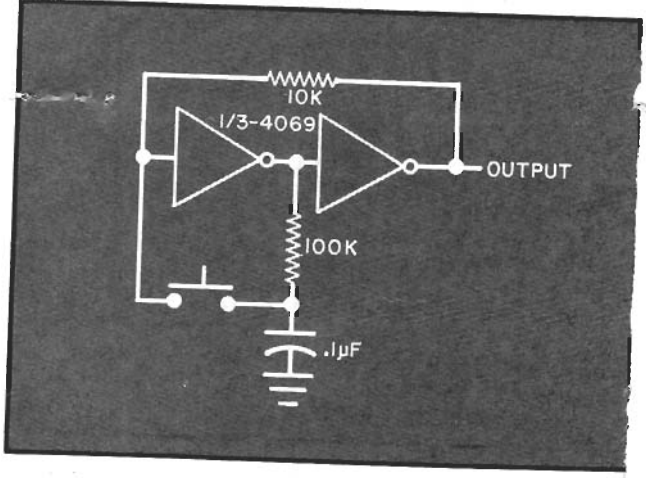
The standard set-reset flip-flop circuit consists of two cross-coupled NAND gates and is set and reset by applying a logic '0' level to the appropriate input. The circuit shown in the figure is triggered by a logic '1' and uses inverters.

Assume that initially both inputs are low and the $\overline{Q}$ output is high. The input of N1 is also pulled high via the 180 k resistor, so the Q output is low, which holds the input of N2 low. If a logic '1' is applied to the S input the $\overline{Q}$ output will go low, pulling the input of N1 low, and the Q output will go high, thus holding the input of N2 high even if the S input subsequently goes low. Applying a logic '1' to the R input will reverse the procedure and reset the flip-flop.

The circuits feeding the inputs of the flip-flop should be capable of providing a logic '1' level into a 180 k load, which normal CMOS circuits are capable of doing.

Reference: RCA Application Notes.





POPULAR ELECTRONICS

Alternate Action Pushbutton

4

Each time the pushbutton switch is operated, the circuit shown here changes its output state. On one depression, the output is high; and on the next depression, the output is low. Operation is reliable and the pushbutton is fully debounced.

Despite its apparent simplicity, this is a full-fledged master-slave flip-flop with the RC network being the "master" that remembers where the output is to go. The two inverters form the "slave" latch.

Three-function RS latch

A standard RS latch as shown in (a) responds to an input at both SET and RESET by bringing both outputs low. An alternative latch, shown in (b), can be used in cases where non-complement outputs are undesirable. When RS is 00, latch 1 and hence latch 2 will not change. When RS is 01, latch 1 resets which sets latch 2. By symmetry, RS at 10 causes latch 2 to reset. With RS at 11, both outputs of latch 1 are forced low. However, two low inputs at latch 2 will not alter the output. A similar latch may be constructed using cross-coupled NAND gates.

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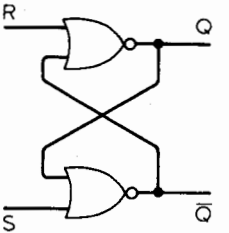
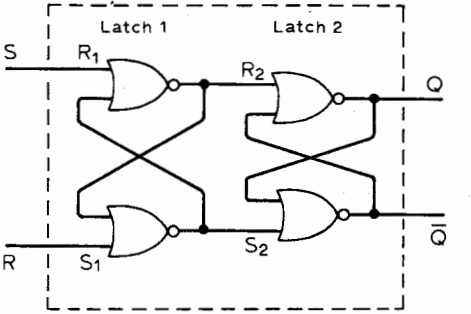


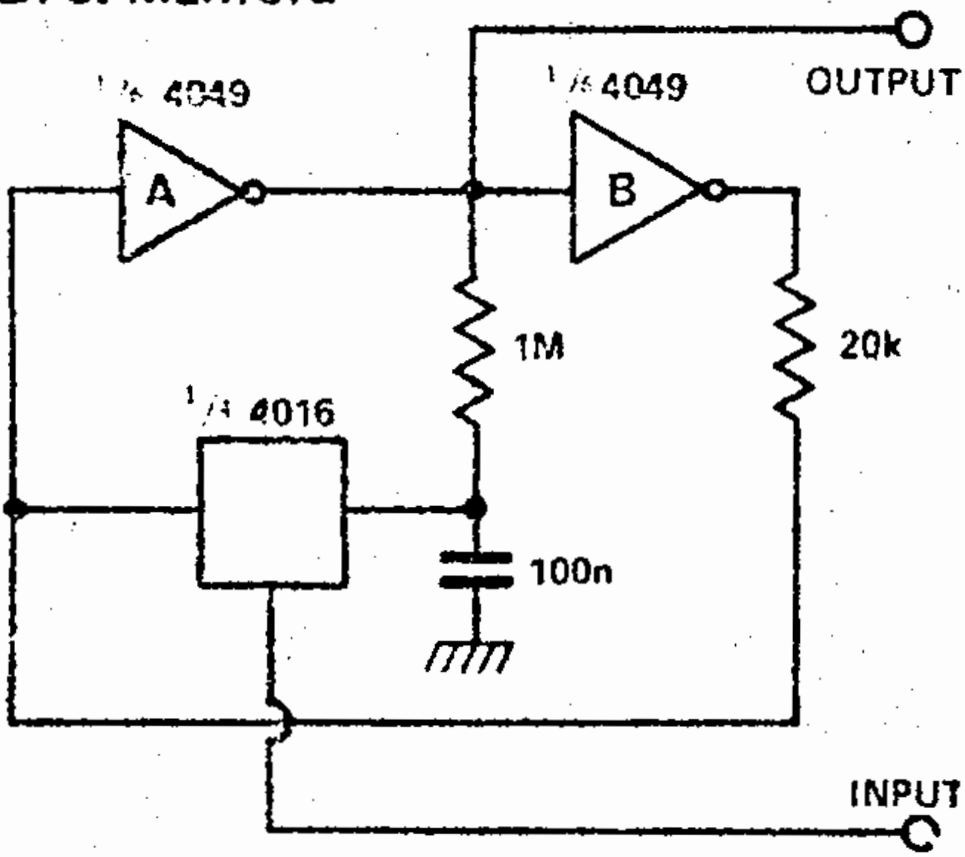
(a)



(b)

Improved SPST Switch Flip-flop

D. J. Manford



This circuit was developed from the SPST switch flip-flop shown in last November'"Tech-Tips", and has the advantage that it can be driven by an input refered to earth— logic outputs or push-buttons.

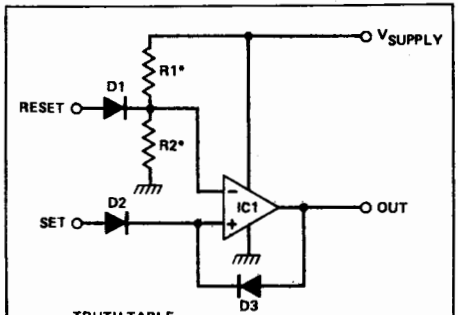
When the input to the 4016 goes high it connects together the input to A, and C. This 'flips' the latch.

The 20k resistor between the output of invertor B and the input of A is needed as the 4016 cannot pull the output of inverter B down directly.

Analogue Set-Reset Latch

T.P. West

Although CMOS gates are commonly used to provide analogue amplifiers, the operational amplifier is often overlooked for use in digital applications. Often, a circuit design calls for a set-reset latch within an analogue circuit: this normally requires digital circuitry to be included in the design. By the use of this circuit, spare op-amps in a package may be utilized to provide the set-reset function. The op-amp used may be of any type with the low and high voltages at the output being only a function of the op-amp's internal output drive circuitry. The resistors R1 and R2 should be chosen so that R2 = 2.4R1 and R2 < $V_{supply}/0.05$. Although the circuit is shown for a single supply rail, it will work on a dual supply but produces a low of around the negative supply voltage. All changes in state occur on the low-to-high transition.



TRUTH TABLE

SET	RESET	OUT
0	0	NC
0	1	0
1	0	1
1	1	1

NC = NO CHANGE

*SEE TEXT

NOTE:
IC1 IS ANY OP-AMP
D1-3 ARE 1N4148

ETI

Another way to build a two-gate flip-flop

by Donald P. Martin
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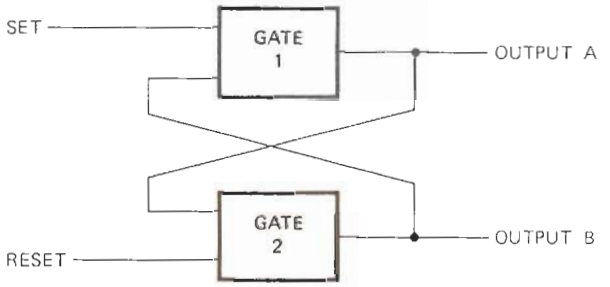
Most logic designers know that a flip-flop may be built with two NAND gates or two NOR gates, but few seem to realize that one AND gate plus one OR gate may often do just as well. This simple substitution can be helpful in minimizing the IC package count for a complex design.

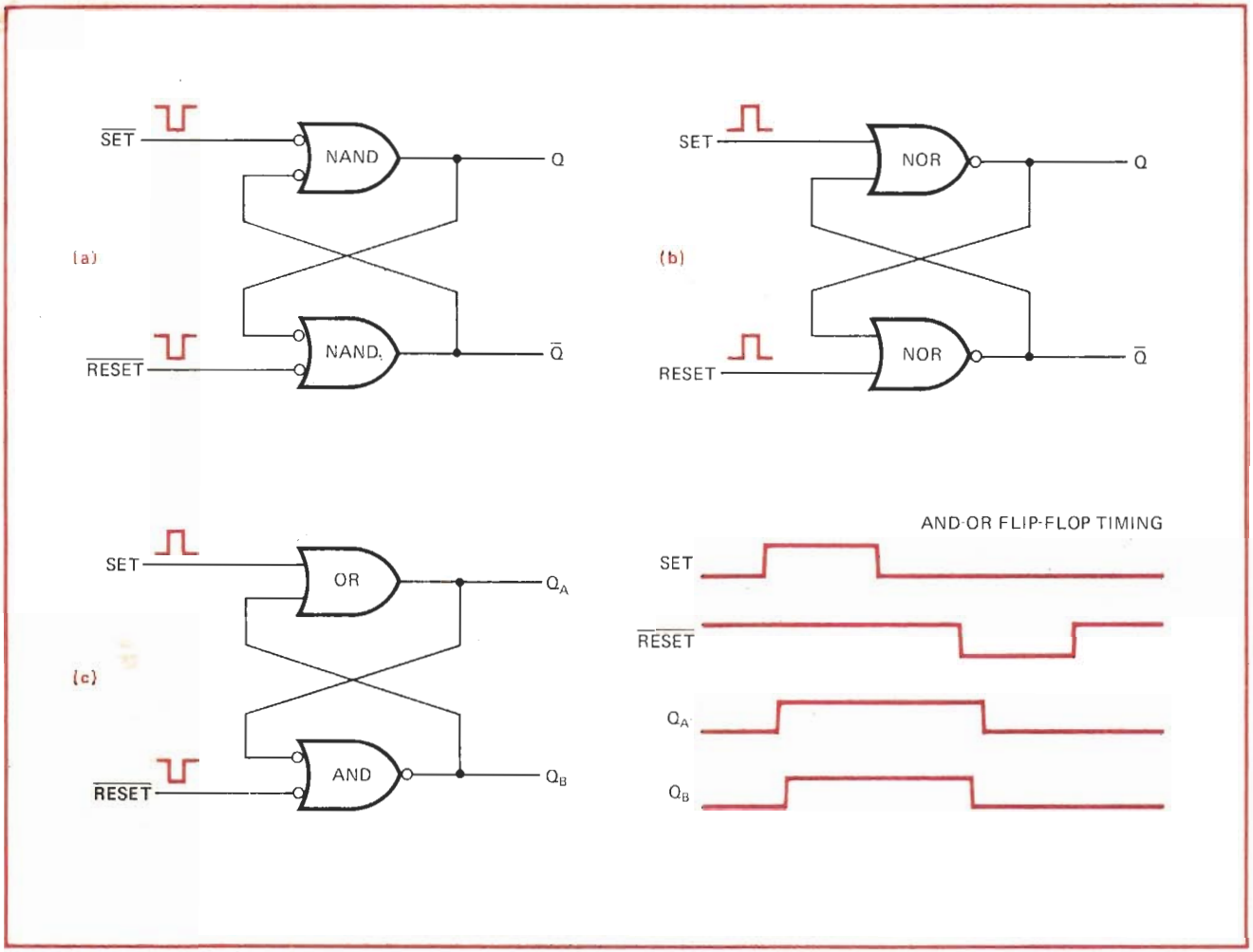
In general, a flip-flop is constructed by taking two two-input gates and connecting one of the inputs of each gate to the output of the other gate (Fig. 1). For proper flip-flop operation, each gate's exceptional input state must be the complement of the other gate's exceptional output state. (A gate's exceptional output state is the logic state that occurs with only one combination of inputs; the exceptional input state is the logic state at both inputs that creates the exceptional output state.)

Figure 2 illustrates the three ways to build a flip-flop—with NAND gates (2a), with NOR gates (2b), or with



GATE	EXCEPTIONAL INPUT STATE	EXCEPTIONAL OUTPUT STATE
NAND	1	0
NOR	0	1
AND	1	1
OR	0	0

1. By definition. For the two-gate flip-flop, one gate's exceptional input state must be the complement of the other gate's exceptional output state. A gate's exceptional output state is that logic state produced by only a certain combination of (exceptional) inputs.



2. Three choices. A flip-flop can be made from two NAND gates, as in (a), or from two NOR gates, as in (b). A third alternative—one that is particularly handy if you're trying to use leftover gates—is to wire up an AND gate and an OR gate. The resulting flip-flop does not have complementary outputs, nor same-polarity set and reset inputs, but it can help avoid undesirable race-prone situations.

AND and OR gates (2c). (The AND gate is drawn here as an equivalent negative NOR gate so that the operation of the AND-OR flip-flop will be clearer.)

The NAND flip-flop requires negative set and reset inputs, while the NOR flip-flop needs positive set and reset inputs. Each of these flip-flops provides complementary (Q and $\overline{Q}$)outputs. Needless to say, the designer who is trying to use leftover gates can employ an AND gate, followed by an inverter to get a NAND gate, or he can put together an OR gate and an inverter for a NOR gate.

Unlike in the NAND and NOR flip-flops, the set and reset inputs of the AND-OR device have opposite polarities—often very conveniently—and the outputs of this flip-flop are not complementary—sometimes quite inconveniently. Of course, an inverter can be added at one of the outputs to change its polarity.

It should be noted that the AND-OR flip-flop can be particularly useful in race-prone applications. During the set pulse of this flip-flop, the Q_A output rises to logic 1 before the Q_B output even starts to rise. □