# Modular switch array includes priority encoder

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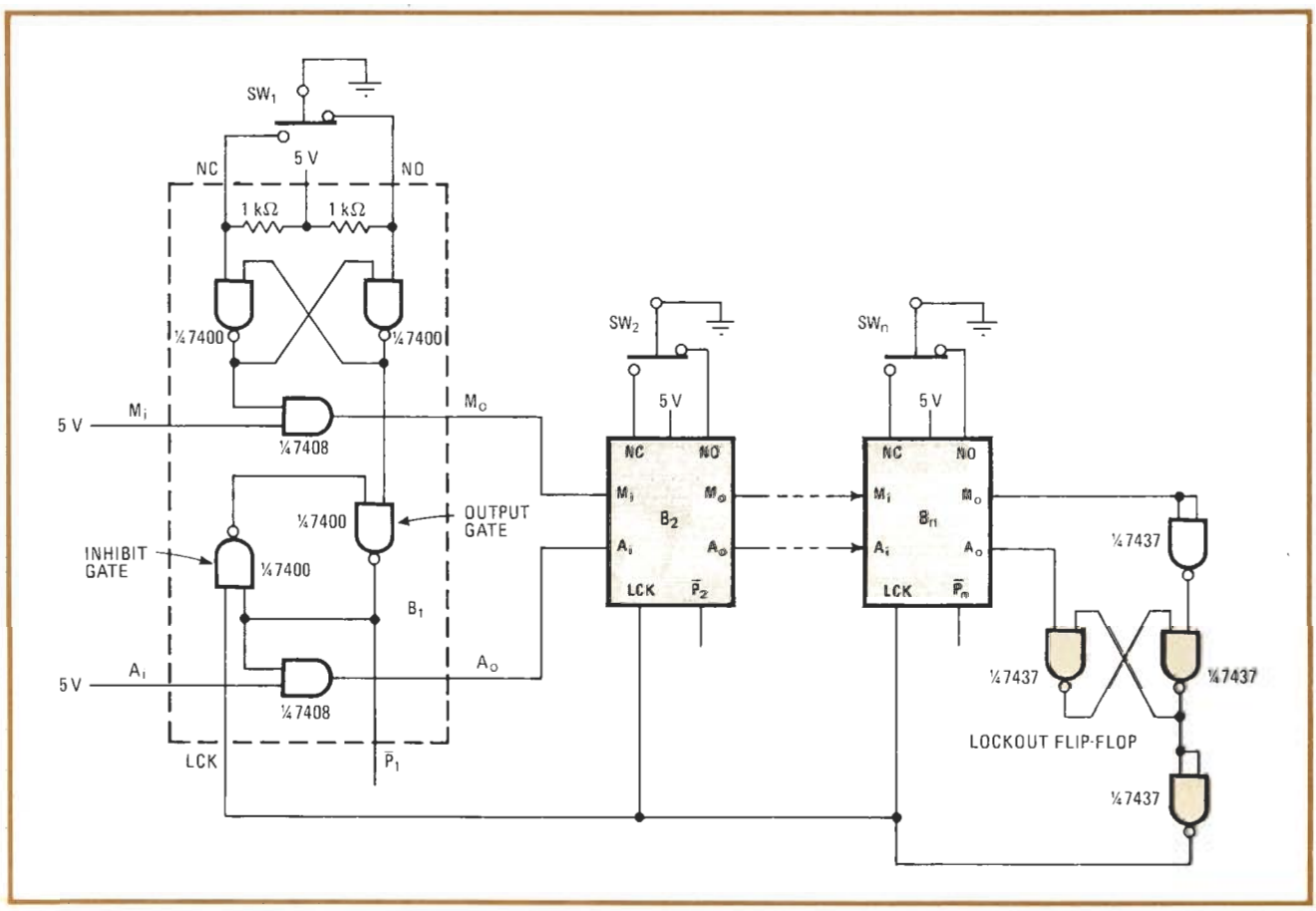
The output ports of this momentary-contact switch array respond to the first command received, and the circuit locks out all subsequent commands, providing a time-sequence priority scheme often needed in industrial systems. The low-cost circuit prevents simultaneous switch depressions from spoiling system operation, and the modularized design technique employed makes it fairly simple to implement.

The structure for this switch array is shown in the figure. A number of single-pole, double-throw switches ($SW_n$) are individually interfaced through the same number of switch buffer modules ($B_n$) to a single set-reset flip-flop at the output of the last module. This flip-flop generates a lock-out signal to ensure that only one module at any given time can be in the active state.

Each module contains its own SR flip-flop, a gated output driver with inhibit circuitry, and two AND gates. The flip-flop is configured to circumvent switch contact bounce and has its inputs connected to the normally open (NO) and normally closed (NC) contacts of each switch. The inverting output is combined with the $M_i$ input signal through an AND gate to derive the $M_o$ output. The noninverting output of the flip-flop is applied to the gated output driver. Each module is cascaded by connecting the $M_o$ and $A_o$ ports to the $M_i$ and $A_i$ ports of the next buffer.

Depressing any switch drives the $\overline{P}_i$ output of its associated module low. The $M_o$ and $A_o$ ports of the last buffer module in the chain move low at this time, permitting generation of the LCK signal.

The inhibit gate in each module will prevent the output gate from going low, irrespective of the state of the input flip-flop, if the buffer module output, $\overline{P}_i$, is inactive. If the buffer module is active, the inhibit gate will be inactive, independently of the state of the LCK




**Priority encoding.** First switch to close captures its output buffer. Circuit disables all other buffer output lines by generating a lockout (LCK) signal. Release of switch or switches automatically resets circuit. The truth table of the switch array is illustrated.

TRUTH TABLE FOR SWITCH ARRAY BUFFER

| Time | $SW_1$ | $SW_2$ . . . | $SW_i$ . . . | $SW_R$ . . . | $SW_{n-1}$ | $SW_n$ | $\overline{P}_1$ | $\overline{P}_2$ . . . | $\overline{P}_i$ . . . | $\overline{P}_k$ . . . | $\overline{P}_{n-1}$ | $\overline{P}_n$ | $M_{o_n}$ | $A_{o_n}$ | LCK |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_0$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| $t_1$ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| $t_2$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| $t_3$ | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| $t_4$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| $t_5$ | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| $t_6$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

output. The lockout flip-flop is not reset until the $M_o$ signal at the last flip-flop moves high again. This occurs when the switch is released.

Once the switch first depressed is released, all module outputs become inactive, even if other switches were activated after a particular module had been set. Only after all switches are released can one of the buffers become active again. The operation of the switch array is shown in the illustration.

This design can accommodate up to 30 switches. This limit on their number is set by the driving capability of the inverter driver of the lockout flip-flop. □