Continued from page 80

Symmetrical divide-by-three
Gary Brunkhorst

This circuit takes an input (symmetrical) square wave at CMOS levels and divides it by a factor of three, producing a symmetrical output. Figure 1 shows input and output waveforms.

At first glance, this may seem a simple task, but note that the output waveform first changes state on a negative-going transition of the input waveform, then on a positive-going transition, etc. The circuit of Figure 2 neatly overcomes the problem of nonsymmetrical divided output by inverting the input waveform periodically, using an exclusive-OR gate.

The waveforms involved are show in Figure 3. The prototype circuit used a 74C73 for flipflop 1 and 2, but almost any type of edge-triggered flipflop could be used. The same method could be used to obtain a divide-by-5, 7 or 9.

(Ed. note: this circuit may not work at high speeds owing to gate delays in flipflops 1 and 2, but is nonetheless a good idea, despite the limitations.)

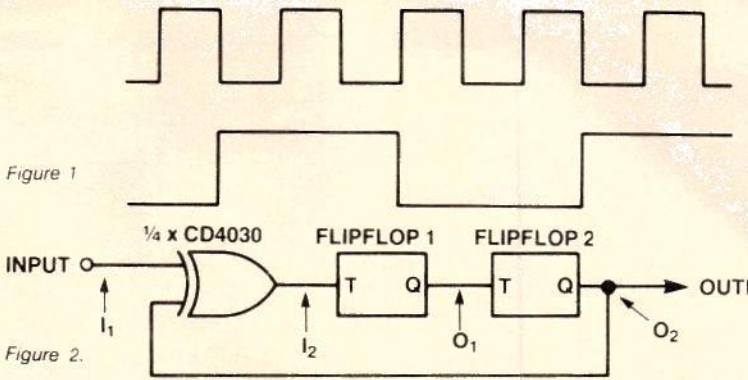

Figure 2.

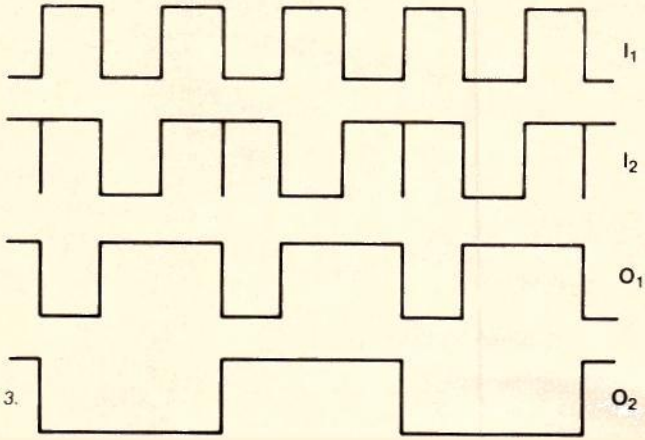

Figure 3.