Square-root counter calculates digitally

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A square-root counter has many uses, notably the measurement of the root-mean-square output voltage of a transducer that has a square-law response. This counter finds the square root digitally, rounded off to the nearest bit, of any analog voltage that has been converted into a digital train of N pulses by a voltage-to-frequency converter. In other words, the circuit finds the square root of N.

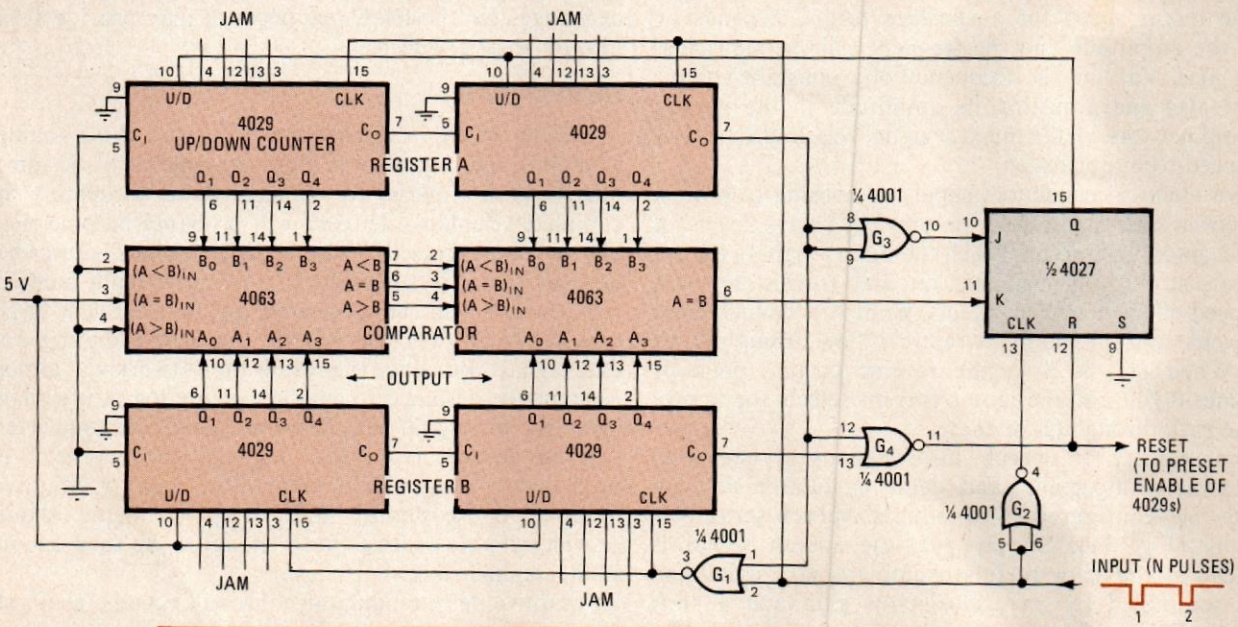
Of course, square-root circuits that generate an analog-voltage output already exist, but they usually require accurate square-law diodes and scaling components like resistor voltage dividers. This circuit, being all-digital, eliminates those shortcomings and in addition is much simpler than the digital square-root detectors now available.

Two registers and a comparator do most of the work. Four 4029 complementary-metal-oxide-semiconductor up/down counters, operating in the binary-coded-decimal mode, form the two synchronously clocked registers, A and B, as shown in the figure. Register A clocks up or down, depending on the state of the C-MOS 4027 flip-flop. Register B advances by one count any time an input clock pulse is received and the carry-out signal ($\overline{C}_o$) of register A is active, or low. The negative-going transitions of the input signal clocks both the flip-flop and B, while positive transitions clock A.

Initially, the flip-flop is reset and both registers are cleared by means of the JAM lines. After the clock pulse (N = 1), register B advances to state 1 and the flip flop is set, placing register A in the count-up mode. Register A then advances to 1 and $\overline{C}_o$ moves high, setting the J input of the flip-flop low.

The C-MOS 4063 comparator detects that the contents of registers A and B are now equal (as they were before, at initialization, and it brings the K input of the flip-flop high.

During the next pulse (N = 2), G_1 inhibits the clock input to register B, and the flip-flop is reset, placing A in the count-down mode. Register A returns to zero, again setting $\overline{C}_o$ low and J high. Then, when N = 3, register B is incremented to 2, while register A counts to 1. On the arrival of a pulse (N = 4), counter A increments to 2, and because the contents of B do not change, an A = B pulse is generated by the comparator. The entire cycle is then repeated, as shown in the table.



CONTENTS OF REGISTERS AFTER N PULSES

N	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18 ...
REGISTER A	0	1	0	1	2	1	0	1	2	3	2	1	0	1	2	3	4	3	2 ...
REGISTER B	0	1	1	2	2	2	2	3	3	3	3	3	3	4	4	4	4	4	4 ...

$N^{1/2}$. Register B in the circuit yields the square root of N, rounded off to the nearest bit, where N is the number of input pulses received after the circuit has been reset to zero. Digital circuit eliminates shortcomings of detectors that measure analog voltages directly.

Thus, register A starts an up count one cycle after it has reached 0, and initiates a down count one cycle after it has determined its contents are equal to B. As a result, the output of register $B = N^{1/2}$.

The reset line is activated by G_4 whenever both registers overflow, and this sets both registers to their initial values. It can also be activated regularly by an appropriate timebase for time-averaging measurements. For special applications, the registers may be preset to a nonzero number via their JAM lines. The registers may also operate in the binary mode without their square-root counting function being affected, while the counters may easily be extended beyond their 8-bit capacity, simply by being cascaded. □