Nonsequential counter design makes use of Karnaugh maps

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The design of a nonsequential binary counter—one that does not count in a 0-1-2-3-4-5-6-7 sequence—can be considerably simplified by the use of Karnaugh mapping techniques. Such a counter is sometimes needed in digital systems where certain functions must be controlled in a nonbinary sequence.

To illustrate the technique, we will design a three-bit counter for a 0-2-4-5-3-7-1-6 sequence. After listing the desired counter states in their proper sequence, as done in (a), the present-state and next-state conditions can be compiled, as shown in (b). Next, three Karnaugh maps, the ones labeled NSM_A, NSM_B, and NSM_C in (c), are used to represent the next-state conditions.

The minterm locations on the next-state maps are determined by the present-state variables. The value for that location is obtained from the next-state table. Since three bits are involved, three J-K flip-flops will be needed to implement the counter.

Six other maps are now constructed—three are to determine the logic functions required at the J inputs of the flip-flops, while three are for the K inputs of the flip-flops. These maps, which are drawn in (d), are labeled J_A, J_B, J_C, K_A, K_B, and K_C, where J_A and K_A represent the inputs of flip-flop FF_A, J_B and K_B the inputs of flip-flop FF_B, and J_C and K_C the inputs of flip-flop FF_C. (TTL flip-flops will be used.)

The locations of the variables that are true are noted on the J-input maps by Xs, indicating that the state of the variable can be either logic 0 or logic 1. (This permits maximum reduction of circuitry.) For example, on the J_A map , the true locations of variable A are marked with an X wherever variable A is logic 1 on its next-state map, NSM_A. These locations are 110, 100, 111, and 101.

The remaining locations on the J-input maps are filled in with the remaining values on the appropriate next-state map. The leftmost four locations on the J_A map, for instance, are identical to the leftmost four locations on the NSM_A map.

Similarly, the appropriate logic functions can be determined for the K inputs. For these however, the locations of the variables that are false are filled in with Xs to mark the "don't care" (can be either logic 0 or logic 1) positions. And the remaining locations are filled in with the proper inverted data from the next-state map. The K_A map, for example, contains Xs whenever variable A is logic 0 on the NSM_A map, and inverted data from NSM_A in the remaining locations.

The logic functions represented by these J-input and K-input maps can be reduced by grouping through Karnaugh mapping techniques. These groups are noted on the map by the colored enclosures. The variables within these groups establish the logic function needed at a particular flip-flop input.

The J_A input requires a signal of $B+C$, which means that the Q output of flip-flop FF_B must be ORed with the Q output of flip-flop FF_C and the output of that OR gate applied to the J input of flip-flop FF_A. Likewise, input J_B requires an OR gate ($\bar{A}+C$), input J_C an AND gate ($A\bar{B}$), input K_A an OR gate ($B+C$), input K_B an OR gate ($A+\bar{C}$), and input K_C an AND gate ($\bar{A}\bar{B}$). The negated variables, of course, are taken from the $\bar{Q}$ outputs of the flip-flops.

Now the nonsequential binary counter design is complete. The circuit of (e) shows what the final configuration looks like. The states of its three output lines agree with the truth table in (b) and proceed in the nonbinary sequence of (a). □

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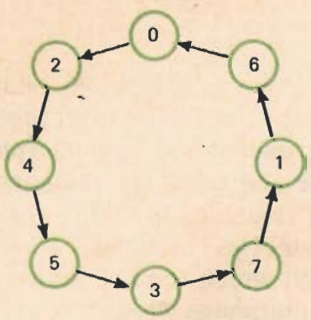
(a)



(b)

TRUTH TABLE			
PRESENT STATE		NEXT STATE	
	A B C		A B C
0	0 0 0	2	0 1 0
2	0 1 0	4	1 0 0
4	1 0 0	5	1 0 1
5	1 0 1	3	0 1 1
3	0 1 1	7	1 1 1
7	1 1 1	1	0 0 1
1	0 0 1	6	1 1 0
6	1 1 0	0	0 0 0

(c)

NSM_A

AB \ C	00	01	11	10
0	0	1	0	1
1	1	1	0	0

NSM_B

AB \ C	00	01	11	10
0	1	0	0	0
1	1	1	0	1

NSM_C

AB \ C	00	01	11	10
0	0	0	0	1
1	0	1	1	1

(d)

J_A

AB \ C	00	01	11	10
0	0	1	X	X
1	1	1	X	X

B, C → B+C

J_B

AB \ C	00	01	11	10
0	1	X	X	0
1	1	X	X	1

$\bar{A}$, C → $\bar{A}$+C

J_C

AB \ C	00	01	11	10
0	0	0	0	1
1	X	X	X	X

A, $\bar{B}$ → A$\bar{B}$

K_A

AB \ C	00	01	11	10
0	X	X	1	0
1	X	X	1	1

B, C → B+C

K_B

AB \ C	00	01	11	10
0	X	1	1	X
1	X	0	1	X

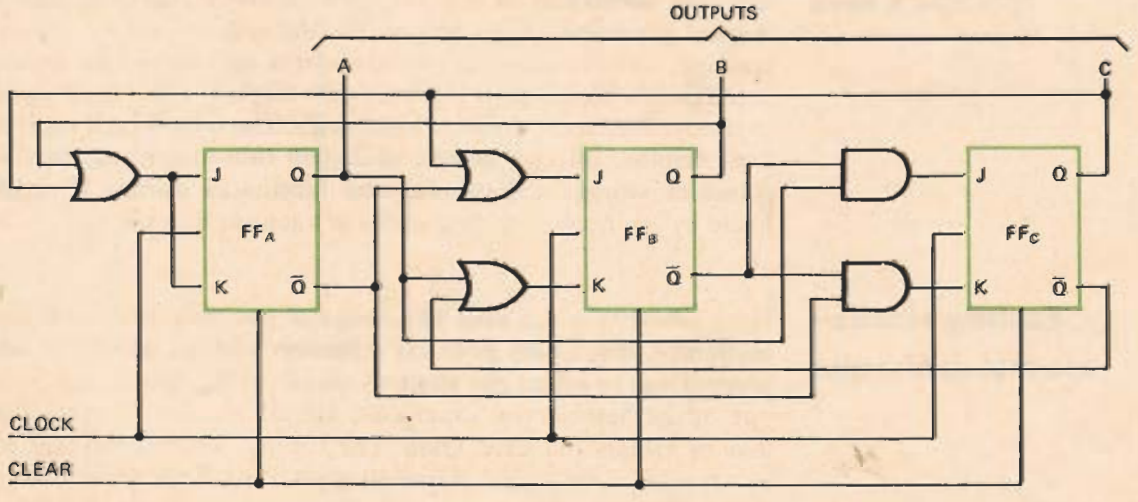
A, $\bar{C}$ → A+$\bar{C}$

K_C

AB \ C	00	01	11	10
0	X	X	X	X
1	1	0	0	0

$\bar{A}$, $\bar{B}$ → $\bar{A}\bar{B}$

(e)



Designing a counter. Karnaugh mapping, a design procedure that is normally applied only to binary designs, can also be used for synthesizing a nonsequential counter. The three-bit binary counter designed here has a 0-2-4-5-3-7-1-6 sequence (a). From the truth table (b) of this counter's next-state outputs, the next-state map (c) can be drawn for each of its three output lines. The next group of maps (d) establish the logic function required at each input of the three J-K flip-flops needed to build the counter. The final circuit is shown in (e).